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Design and Implementation of Low Power D flip flop for Embedded Application

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Abstract - *Optimizing the power consumption of flip-flops (FFs) can greatly lower the power consumption of digital systems. An energy-efficient retentive true single-phase-clocked (TSPC) FF is proposed . The proposed TSPC FF precharges only when necessary by using input-aware precharge strategy. Floating node analysis and transistor level optimization are also used to assure the FF's great energy efficiency without considerably expanding its size. By using 22-nm CMOS technology, the suggested FF consumes 30.37 percent less power than a standard transmission-gate flip-flop (TGFF) at 10% data activity at a supply voltage of 0.95 V. As the data activity decreases to 0%, the reduction rate increases to 98.53 percent.*

Key Words: Flip flop, low voltage operation, low power, redundant-precharge-free, true single phase clocked(TSPC).

1 .INTRODUCTION

As the process has advanced, digital systems' performance has significantly improved, and power consumption has turned into a severe limitation. Additionally, IOT devices are widely used in the Internet of Things due to the Internet's explosive growth (IOT). There are several uses for the Internet of Things (IOT). Just a few examples include transportation, healthcare, and intelligent settings. Such battery-powered or self-powered devices use low-power components. Flip-flops (FFs) are key components that account for a sizeable amount of the total power. FFs frequently consume 50% or more of the power consumed for operations in the random logic sector. Due to its redundant transition of internal nodes when the input and output are in the same state, flip-flops (FF) generally consume more than half of the random-logic power in a SoC device. Hence lowering the power consumption of FFs can drastically minimize the amount of energy consumed by Digital systems.

The transmission-gate flip-flop (TGFF) is the FF that is utilized the most frequently in modern digital systems. The TGFF schematic is depicted in Figure 1. The TGFF is a near threshold operation-capable, contention-free FF. The biggest problem with TGFF is the extensive clock network. The internal nodes CKN and CKI toggle, and the nodes CKN and CKI drive a greater number of transistors, regardless of the input data. As a result, TGFF continues to consume a lot of power even when data traffic is minimal. To reduce FF's power usage, complementary clock signals should be used more selectively.

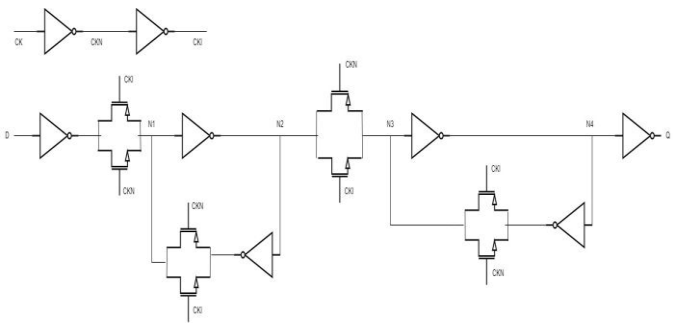

Fig -1: Schematic of D flip flop using transmission gate

Previous publications [2]–[6] have proposed many low-power single-phase-clocked FFs. However, there are still certain issues with the power usage of these FFs' .Some FFs, fail at low supply voltage [2]–[4], [6], and others have a high precharge power [2], [4]–[6]. This article proposes a low-power true-single-phase-clocked (TSPC) FF. The suggested FF is free of contention and can operate at a wide range of supply voltages. Furthermore, in comparison to previous low-power FFs, redundant precharge operation is completely eliminated in the proposed FF, and power consumption is further minimized.

2. STRUCTURE OF PROPOSED FLIP FLOP

The proposed FF's structure is thoroughly explained in this section. Any unnecessary transitions of internal nodes should be avoided in order to reduce the power consumption of FF. To remove redundant precharge and discharge operation following procedures are used to optimize the flip flop. In input aware precharge scheme unnecessary precharge operation of the internal node N2 is completely removed. The floating node, on the other hand, is under consideration in order to avoid short current, which would boost power consumption. Finally, unneeded transistors are merged or removed in order to reduce the area.

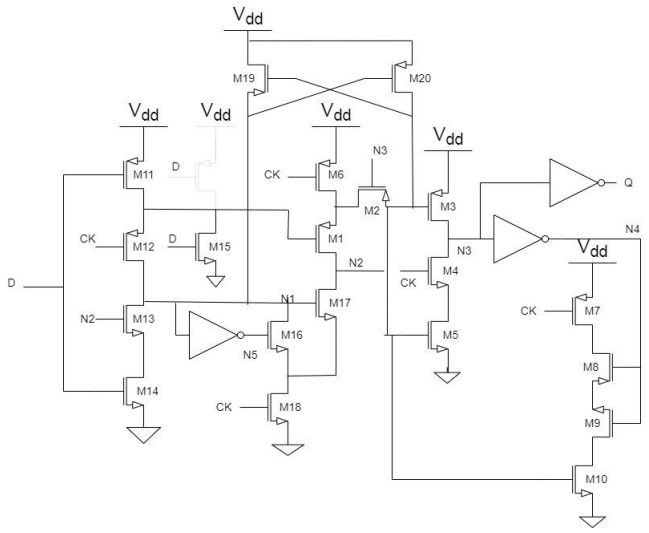

Fig -2: Design of low power D flip flop

Input-Aware Precharge Scheme

When the input data is 0, the precharging of the node N2 is not necessary, hence the precharge path should be cutoff when *D* = 0. . A PMOS M1 that is controlled by the input data is inverted and inserted into the precharge path of flip flop. . If the input data is a 1, PMOS M1 is turned on, and the necessary precharge operation works as expected. When the input data remains zero, the PMOS M1 is turned off, and the precharge path is blocked by the inserted transistor. As a result, the redundant precharge operation is no longer required.

Floating Node Analysis

Floating nodes need to be carefully analyzed since leakage current during transition may cause their voltage to fluctuate, which could lead to the formation of short-circuit routes. The voltage of the node N2 is no longer precharged to VDD at the negative half cycle of CK when the input is zero as a result of the installation of input aware transistors. The state of the node N2 must therefore be carefully examined

Transistor M9 and M10 retain the state of N3 when the output Q = 1, which results in N3 = 0.The voltage of N2 must be high in order to maintain the transistor M3 OFF and the transistor M10 ON at that moment. A transistor M2 is placed to maintain the voltage of N2 in order to prevent N2 from floating while the following input data is 0. When Q = 1, N2 has a precharge channel through M2, which is controlled by N3.

Transistor M7 and M8 retain N3's state when the output Q is equal to 0. When clk is low and input data is 0 precharge path of N2 is cut off and hence voltage of N2 doesn't charge to high. The node N3 is isolated from its pull-down path (M4 and M5) through M4 when N3 = 1, CK = 0, and D = 0, hence the voltage of N2 has no impact on the node N3. Similarly, through M14 (D = 0), N1 is isolated from its pull-down path (M13 and M14), and the voltage of N2 has no effect on the node N1. As a result, the floating of node N2 is insignificant in this case.

Transistor Level Optimization

The redundant precharge operation is eliminated after using the input-aware precharge scheme and floating node analysis, but the FF can be improved further. M11 can be merged with PMOS M11 1, which is used to generate the inversion of the input data. However, the NMOS M15 cannot be combined with M14 at the same time. When both PMOS and NMOS are merged, the drains of M11 and M14 are directly connected, which can result in FF functional failures. As a result, the NMOS M15 is reserved, as illustrated in Fig. 2.

Operation of the Proposed FF

The detailed operation of the proposed FF is shown in Fig. 3.

High-to-Low Transition:

When CK is low, nodes N1 and N2 are charged to VDD through M11-M12 and M6-M2 respectively. Node N3 maintains a low state through M9 and M10, and the output Q remains high. To isolate the FF from changes in the input data, M13 is turned off after N2 is discharged to GND through M17 and M18 at the rising edge of CK. The output Q goes to 0 once the node N3 is charged to VDD through M3. Throughout the positive half cycle of CK, N1 maintains a high voltage through M19, whereas N2 maintains a low voltage through M17 and M18.

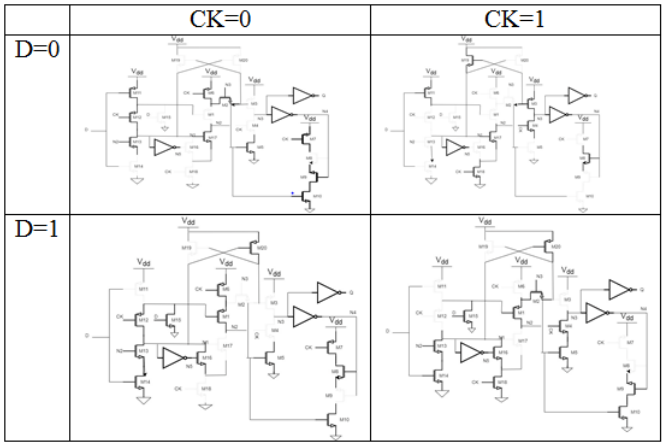

Fig -3: Operation diagram of the D flip flop

Low-to-High Transition

When CK is low, the node N3 maintains a high state through M7 and M8, N2 is charged to VDD through M6 and M1, N1 is discharged to GND through M13 and M14, and the output maintains a low state through M7 and M8. The node N3 is discharged to GND through M4 and M5 and the input data is

isolated through M12 at the CK rising edge, after which the output Q switches to 1. During the positive half cycle of CK, the voltage of N1 remains low through M16 and M18 while the voltage of N2 remains high through M20.

Additional Functions of the Proposed FF

FFs generally need extra features like set, reset, and scan in digital systems. The proposed FF can simply be expanded to include these extra features.

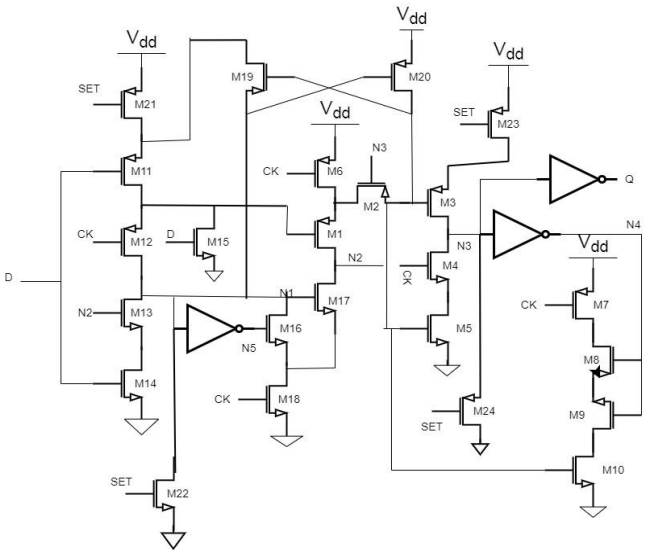

Fig -4: Schematic of the proposed FF with set

Fig 4 shows the schematic of proposed flip flop with set. When SN is low and SET is high the charging path of N1 is blocked by M21, and N1 is dragged down through M22. N2 is charged to VDD through M20 because the node N1 is low. N3's charging path is blocked by M23 at the same time that N3 is pulled down by M24 and the output remains high. The transient waveform of the suggested FF with a set function is shown in Fig. 4.1. As seen in Fig.4.1, the output Q remains high while SN is low, indicating that the FF is in the set state. On the other hand, the FF functions normally when SN is high.

The proposed FF with reset function is shown schematically in Fig.5 when the reset signal RSTN is low and RST is high the charging path of N2 is blocked by M21, and N2 is dragged down through M22, as shown in Fig.4.2. N3 is charged to a high level through M3 since N2 is low, and the output Q remains low. N1 is charged to high through M19 at the same time. When CK = 0 and D = 1, a PMOS M23 is introduced to isolate N1 from the input and prevent short circuit current through M12 and M15.

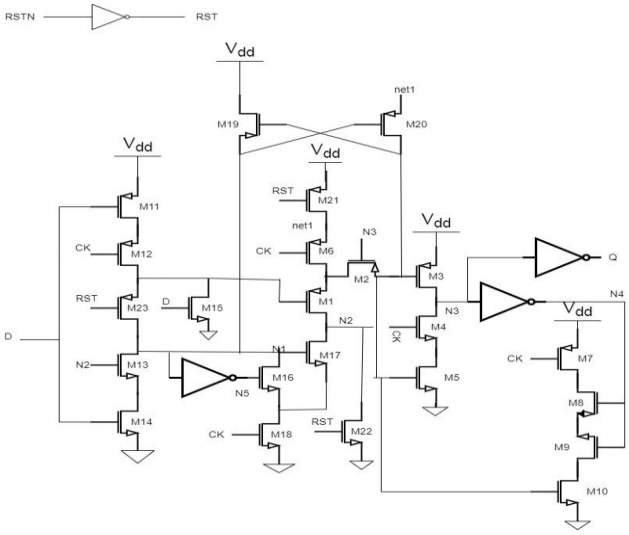

Fig -5: Schematic of the proposed FF with reset

The transient waveform of the suggested FF with reset function is shown in Fig. 5. As seen in Fig. 5 the output Q remains low when RSTN is low, indicating that the FF is in the reset state. In contrast, the FF successfully collects the input data at the rising edge of CK when RSTN is high.

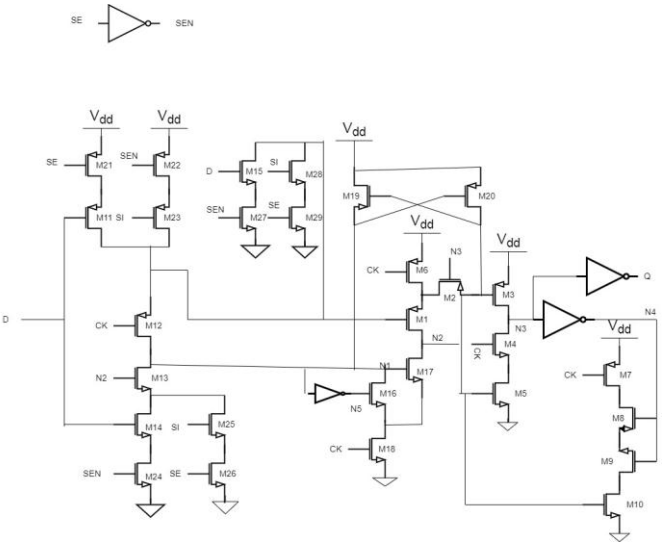

Fig -6: Schematic of the proposed FF with scan

The proposed FF with the scan function is shown schematically in Fig.6. As seen in Fig.6, the input data D is separated from the FF when the scan enable signal SE is high, and the FF captures the data of the scan input SI at the rising edge of CK. The FF catches the input data D at the rising edge of CK when SE is low, isolating SI from the FF.

3. RESULTS AND DISCUSSIONS:

Simulation using 22-nm CMOS is used to show the performance of Proposed FF. For the simulation, the same transistor size is used. The proposed FF can offer significant

energy efficiency improvements when applied to large-scale integrated circuits, which is due to the removal of redundant precharge operations, as described in [4], which states that the average data activity of FFs in large-scale integrated circuits is typically between 5 and 15 percent. In nearly all areas of data activity, Proposed FF uses the least amount of power.

Power comparison of proposed FF and TGFF at different technology node is listed in table 1.Here analysis is done for 180nm, 45nm, 32nm and 22nm CMOS technology node. Power dissipation keeps on decreasing as we move from higher technology node to lower technology node and power dissipation of proposed FF is less compared to TGFF in every technology node.

At 10% data activity, the power dissipation of proposed FF is 66% lower than that of TGFF. Similarly at 0% data activity the power dissipation of proposed FF is 98% lower than TGFF which is listed in table2. The proposed FF uses only 1.5% of the power used by the TGFF when data activity is zero. This is mostly due to the fact that the proposed FF requires no additional operations while there is no data activity, hence the only power consumption at this time is leakage power. When the data activity for TGFF is 0, the internal nodes (CKN and CKI) still need to function as usual, wasting a lot of power.

Technology	Parameters	Transmission gate FF	Proposed FF
22nm	Power	1.0519E-07	7.4683E-08
	Delay	4.0628E-09	4.0617E-09
32nm	Power	1.9822E-07	1.6852E-07
	Delay	4.0886E-09	4.0536E-09
45nm	Power	3.8184E-07	2.6824E-07
	Delay	4.0936E-09	4.0559E-09
180nm	Power	4.1599E-05	2.5956E-05
	Delay	4.1940E-09	4.0793E-09

Table 1: Comparison of power and delay at different technology node

Precharge and discharge processes are still required for other FFs such the SPC-18T FF and S2CFF while the data is still 0, which indicates lesser energy efficiency compared to

the proposed FF. In ACFF and TCFF, there is no redundant precharge process, and both types of FFs exhibit good energy efficiency when there is no data activity. However, the two FFs' power increases more quickly with data activity due to current contention (in ACFF) and a large number of shared transistors (in TCFF), which lowers their energy efficiency.

Flip Flop	Transmission gate FF	Proposed FF
Average Power when data activity is 10%	1.0519E-07	7.4683E-08
Average Power when data activity is 0%	5.1698E-08	5.9309E-10

Table 2: Comparison of power at different data activity

4. CONCLUSIONS

An energy-efficient retentive TSPC FF is proposed in the paper. The input-aware precharge approach considerably reduces the power of the proposed FF by eliminating superfluous precharge and discharge procedures. The proposed structure is also subjected to floating node analysis to prevent the formation of short-circuit routes. The circuit is then optimized at the transistor level to further reduce its size and power usage. According to post layout simulation results, the suggested FF consumes less power than TGFF with less than 10% data activity.

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