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A PV BASED MODIFIED MULTILEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES

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Abstract - *Multilevel inverters are used in industrial applications for high power and medium voltage situations. Along with the generation of high voltage levels, Multilevel inverters (MLIs) demonstrates less Total Harmonic Distortion (THD) than a normal inverter. With the generation of multi levels of voltage, formation of high-quality waveforms can be facilitated. Based on the components used, there are three types of MLIs. Among those three, cascaded H bridge MLI uses lesser number of components such as capacitors and diodes. But it also requires two voltage sources and eight switches to generate five levels of voltage as output, making the system more bulky and expensive. In order to overcome the current constraints, a modified multilevel inverter with reduced number of switches and using renewable source of energy is introduced. In this modified Multilevel Inverter, we are using five switches and renewable energy based voltage source to generate five levels of voltage thereby reducing the harmonics experienced by the circuit alongside make the system less complex and more compact.*

Key Words: Multilevel inverters, Total Harmonic Distortion.

1.INTRODUCTION

Multilevel inverters can operate in high power using low rating devices. If the number of levels and the frequency with which they are switched is more, the approximation to a sine wave for the output voltage signal will be close enough. There are three different types of multilevel inverters such as Diode clamped Multilevel inverter, Flying capacitor Multilevel inverter and Cascaded H bridge Multilevel inverter. Diode clamped multilevel inverter, generating m levels of output voltage and requires (m-1) capacitors, 2(m-1) number of switches and (m-1)(m-2) numbers of clamping diodes. 'm' being the levels of output voltage required. So, inorder to generate five levels of output voltage, it requires 8 switches, 12 diodes and four capacitors. Similarly, Flying capacitor Multilevel inverter requires 0.5*((m-1)(m-2)) clamping capacitors, making use of (m-1) main dc bus capacitors to generate m level of output voltage. Among these three Multilevel inverters, Cascaded H bridge MLI uses reduced number of diodes and capacitors. Still it needs two voltage sources and eight switches and a diode to generate five levels of output voltage. This makes the system more bulky and expensive. In this modified system, an attempt is made to reduce the number of switches to the utmost and to reduce the harmonics experienced by the circuit. In this modified system, an attempt is made to reduce the number of switches to the utmost and to reduce the harmonics experienced by the circuit.

2. MODIFIED MULTILEVEL INVERTER

1.1 Circuit Diagram

The conventional Cascaded H Bridge multilevel inverter needs two voltage sources and eight switches to generate five levels of output voltage. This makes the system expensive and bulky. An attempt is made to reduce the number of switches used in the cascaded H bridge multilevel inverter and in the modified version of cascaded H bridge MLI, we are going to generate the same five levels of output voltage using two voltage sources and five switches. Two or three switches are turned on at a time to produce a particular level of output voltage. Based on the requirement, we could generate required level of voltage when connecting with the grid.

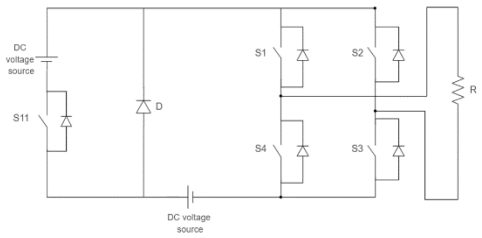

Fig -1: Circuit diagram

In order to generate an output voltage twice that of input voltage given, three switches are turned on and to generate an output voltage level same as what we have given at the input side, two switches are turned on at the same time.

1.2 SWITCHING PATTERN

Based on the occasions at which switches are turned on and turned off, a look up table is made. Using this look up

table we could easily determine which switches are turned on and turned off at a particular time period and then it will be easy to develop a switching pattern. For instance, to get V_1 voltage as output, S_1 and S_3 will be turned on and diode will be forward biased. In the look up table, turning on of switches is represented in one's and turning off is represented in zeros. Since diode is a unidirectional device, it will prevent backflow of current from occurring.

Sl:No	Voltage level	S_1	S_2	S_3	S_4	S_5	Diode
1	0	1	1	0	0	0	0
2	V_1	1	0	1	0	0	1
3	V_1+V_2	1	0	1	0	1	0
4	V_1	1	0	1	0	0	1
5	0	0	1	1	0	0	0
6	$-V_1$	0	1	0	1	0	1
7	$-(V_1+V_2)$	0	1	0	1	1	0
8	$-V_1$	0	1	0	1	0	1

Table -1: Switching Pattern

From this look up table, switching pattern is developed. If the total time period is T seconds, then from the lookup table we can observe that switch S_1 is turned on for half of the time period and the remaining time it is kept in off mode.

Here we are giving a switching frequency of 50Hz. So, the total time period will be around 0.02 seconds. And then we can say that switch S_1 is turned on for half the time period and then turned off for the remaining half. That is it is turned on for 0.01 seconds and kept turned off the remaining period. Five levels of voltages, OV, +V, -V, +2V and -2V can be generated using this switching pattern using only five number of switches.

3. COMPARISON BETWEEN CASCADED H BRIDGE MLI AND MODIFIED MLI

3.1 CIRCUIT AND WAVEFORM OF CASCADED H BRIDGE MLI

Simulation is made using MATLAB/SIMULINK. Circuit diagram is made using blank model of MATLAB and using powergui, simulation is executed. By switching properly using pulse generator, output voltage levels can be generated.

Input voltage of 20 Volt is given as voltage at the input side. Pulse generator is set with a switching frequency of 50Hz and corresponding switching is given. Output voltage waveform and gate pulses are observed. Input voltage waveform is as shown in Fig 3.

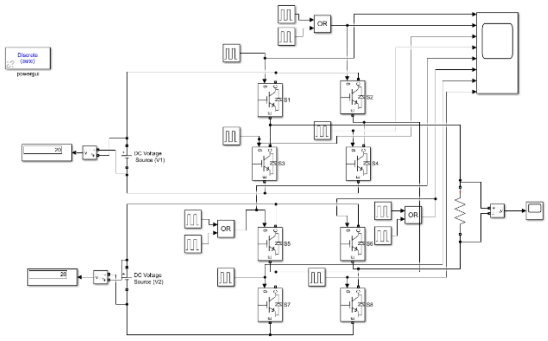

Fig -2: Simulink model of CHBMLI

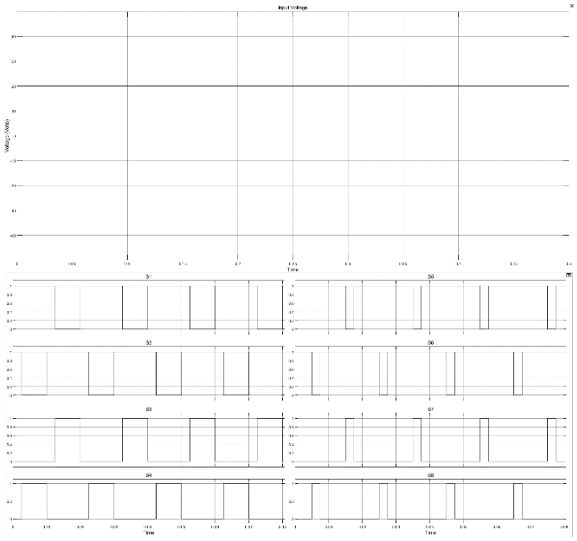

Fig -3: Input Voltage and Pulses

The gate pulses are generated using the switching look up table, the given pulses are evaluated using scope. Pulses given for each switches $S_1, S_2, S_3, S_4, S_1', S_2', S_3', S_4'$.

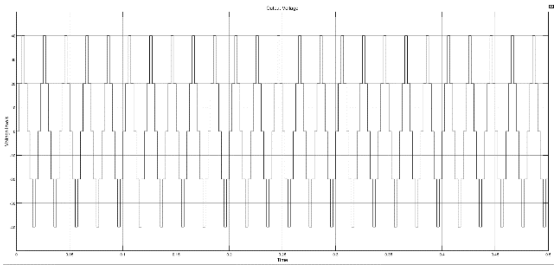

Fig -4: Output Voltage

With the given pulses, output voltage obtained is as shown in Fig 4. Five levels of output voltage with voltage levels 0 Volt, 20 Volts and 40 Volts obtained for an input of 20V from DC voltage source.

3.2 CIRCUIT AND WAVEFORM OF MODIFIED MLI

Modified Multilevel inverter is made with reduced number of switches and with same number of voltage sources as in

cascaded H bridge MLI. The five switches are arranged in a particular topology so that while turning on 2 or more switches, desired value of output voltage can be generated.

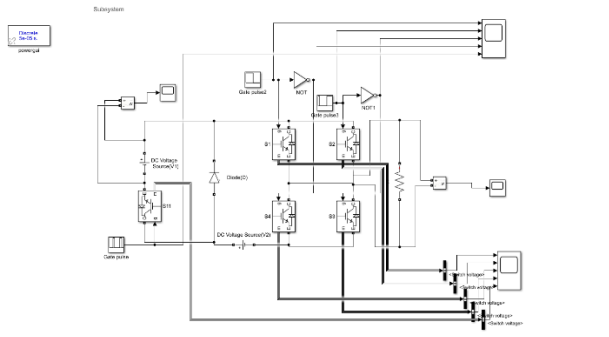

Fig -5: Simulink model of Modified MLI

Simulation is done in MATLAB/SIMULINK. 20 V is given using each voltage sources and gate pulses are given using repeating sequence block. Simulink model of modified Multilevel Inverter is shown in Fig 5.

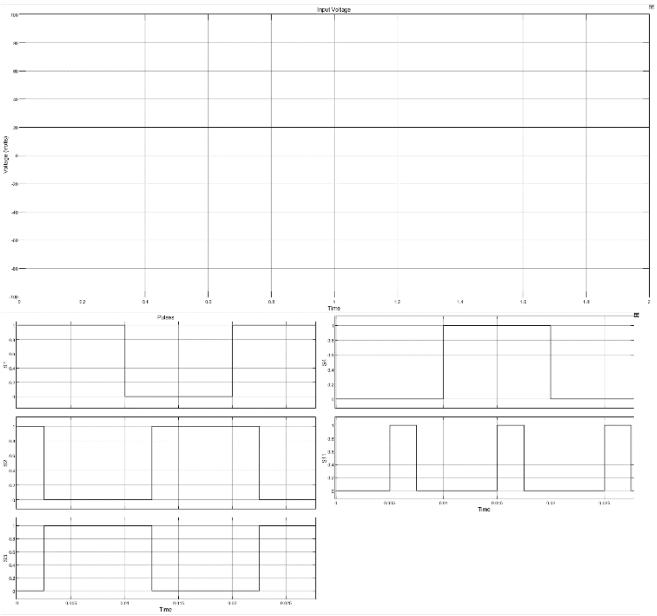

Fig -6: Input voltage and Pulses

Input Voltage waveform, gate pulses given and output voltage waveform is observed. Input Voltage waveform and Gate pulses given to the five switches is as shown in Fig 6. The output voltage waveform obtained after giving these gate pulses is shown in Fig 7.

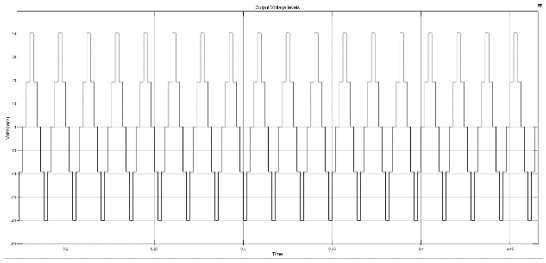

Fig -7: Output Voltage of modified MLI

3.3 COMPARISON OF HARMONICS OF CHBMLI AND MODIFIED MLI

Unwanted distortions in the power system creates increase in current in power system which results in high temperatures in the components that we are using. So, it is crucial to analyze and mitigate the harmonics experienced by the system.

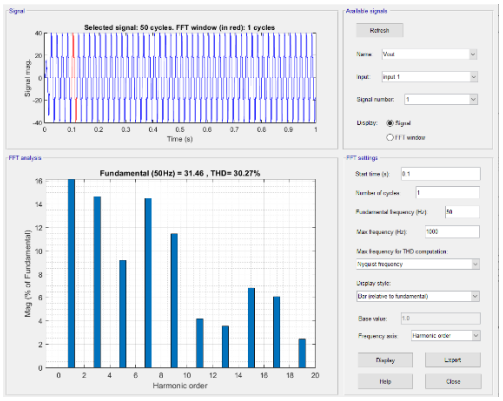

Fig -8: THD of CHBMLI

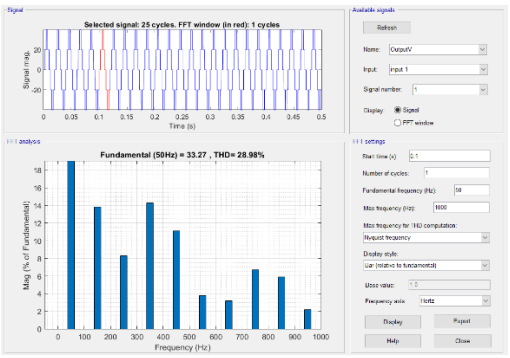

Fig -9: THD of Modified MLI

Total Harmonic Distortion (THD) experienced by the Cascaded H Bridge Multilevel inverter is shown in Fig 8.

The THD observed in cascaded H bridge multilevel inverter is around 30.27\%

The THD of modified multilevel inverter is around 28\%. Which is less than the conventional system. So we can say

that, with the reduction of switches in the multilevel inverter, harmonics can easily be reduced to a certain level.

4. PV BASED MODIFIED MULTILEVEL INVERTER

Multilevel inverters require more than one voltage sources for its proper working. Making use of DC voltage sources like batteries may make the system more bulky. By making use of renewable source of energy as the supply, its easy to give power to the system and thus it becomes more compact.

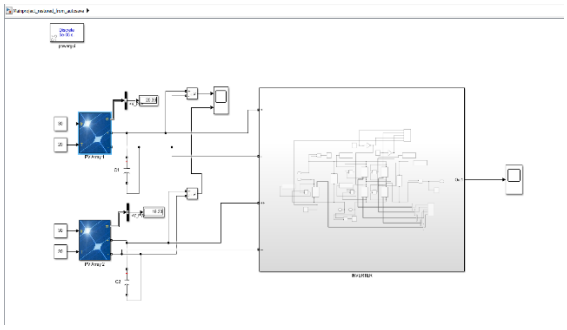

Fig -10: PV based Modified MLI

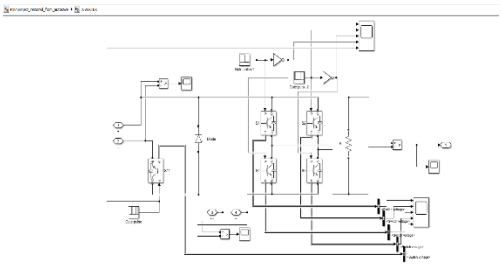

Fig -11: Inverter Subsystem

PV array panel in MATLAB/SIMULINK is used as the voltage source for the simulation. Irradiance of 30 W/m^2 and temperature of 20^{0}C is given as input to PV panel using constant block. PV panel is set with 36 cells using user defined option in PV array. If the voltage generated by each cell is around 0.56 Volt, then the expected output voltage from the solar panel will be (0.56*36) = 20.16 Volts. From Fig 10, the output from solar panel is observed to be around 20 Volt from one panel and 19 Volt from another panel. These two voltages are fed to the inverter subsystem shown in Fig 11. Simulation parameters is as shown in look up table.

SIMULATION PARAMETERS	VALUES
Irradiance	30 W/m^2
Temperature	20^{0}C
Cells per module (Ncell)	36
Resistor	100 ohms

With the given gate pulses, output voltage waveform obtained is as shown in Fig 12.

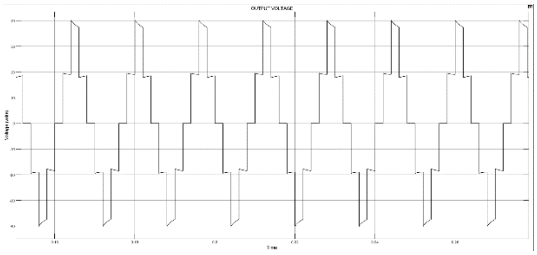

Fig -12: Output Voltage

4.1 CIRCUIT AND WAVEFORM OF MODIFIED MLI

Proteus is a design software used for electronic design automation. It is used to create schematics and electronic prints and to generate PCB layout for printed circuit boards (PCBs).

4.1.1 PROGRAM CODE FOR MICROCONTROLLER

Programming language used is C programming using mickroC software. Switching pattern is fed within a while loop and then pulses are generated.

```
#include <xc.h>

void main(void)
{
  trisc=0;
  portc=0;
  delay_ms(500);

  while (1) {
        portc.f0=0;
              portc.f1=1;
              portc.f2=1;
              portc.f3=0;
              portc,f4=0;
              delay_us(2500);

              portc.f0=0;
              portc.f1=1;
              portc.f2=0;
              portc.f3=1;
              portc.f4=0;
              delay_us(2500);
```

```
            portc.f0=1;
            portc.f1=1;
            portc.f2=0;
            portc.f3=1;
            portc.f4=0;
            delay_us(2500);

            portc.f0=0;
            portc.f1=1;
            portc.f2=0;
            portc.f3=1;
            portc.f4=0;
            delay_us(2500);

            portc.f0=0;
            portc.f1=0;
            portc.f2=0;
            portc.f3=1;
            portc.f4=1;
            delay_us(2500);

            portc.f0=0;
            portc.f1=0;
            portc.f2=1;
            portc.f3=0;
            portc.f4=1;
            delay_us(2500);

            portc.f0=1;
            portc.f1=0;
            portc.f2=1;
            portc.f3=0;
            portc.f4=1;
            delay_us(2500);

            portc.f0=0;
            portc.f1=0;
            portc.f2=1;
            portc.f3=0;
            portc.f4=1;
            delay_us(2500);
        }
}
```

Ports represented here refers various pins of the microcontroller. Portc.0 is 10th pin of microcontroller PIC16F676. Portc.1 represents 9th pin, portc.2 represents 8th pin, portc.3 represents 7th pin and portc.4 represents 6th pin of microcontroller.

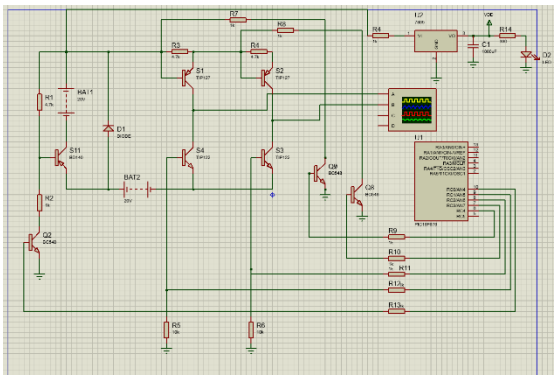

Fig -13: Proteus Simulation

Microcontroller pin 10 is used for S_{11} control Pins 9, 8, 7, 6 are for the control of switches S_1, S_2, S_3, S_4 respectively. Thus pulses are generated in each pin of the microcontroller to drive each switches.

Connection using microcontroller is done using proteus software so that it will be easy to generate the PCB layout of the whole system. Shown in figure 13.

5. COMPONENT SELECTION

Breadboard connection of the whole circuit is made to check the feasibility of the connection as shown in Fig 14.

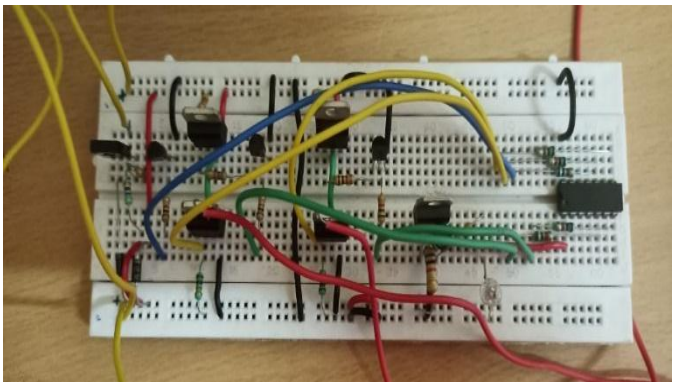

Fig -14: Breadboard Connection

The output voltage obtained from the Digital Storage Oscilloscope is as shown in Fig 15.

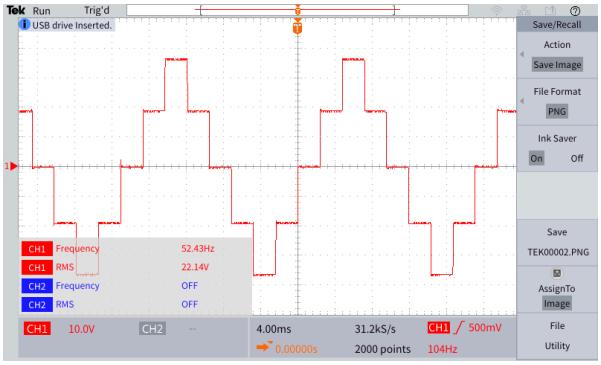

Fig -15: Output Voltage from Breadboard connection

By keeping the DSO in measurement mode, Peak to peak voltage, mean value of voltage and frequency of the waveform is easily obtained. From Fig 15, we can see that the output voltage obtained is around 79 Volts and frequency is around 50 Hz.

5. CIRCUIT BOARD CONNECTION USING PV PANEL

With the usage of PV panel, DC voltage sources that makes the system bulky, can be replaced. PV panel and etched circuit board is as shown in Fig 16.

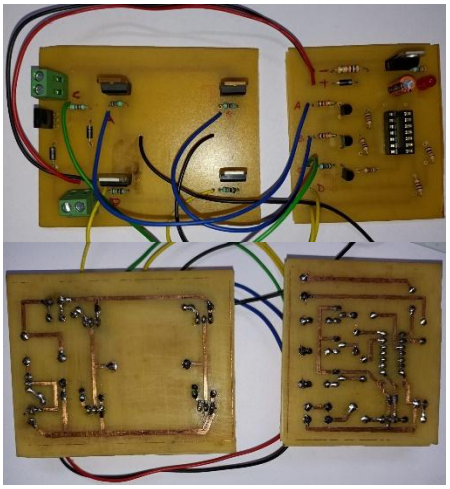

Fig -16: Input PV panel, Circuit connection and Etched connection

Output from the solar panels is as shown in Fig 17. This is given as input to the circuit connection.

Fig -17: Output from Panel 1

Fig -17: Output Voltages from panel 2

Peak to peak value of 16 volt and 7 volt is obtained from the output of solar panel.

Based on the input voltage waveform obtained, five level output voltage with a maximum peak to peak value of 56 Volts and a frequency around 50 Hz can be observed.

6. CONCLUSIONS

With the advancements in technology, development of clean and more compact form of power electronic devices plays a pivotal role for the furtherance in aiding sustainable energy scheme. The role of multilevel inverter in that is unavoidable. Through this project aiming at reducing the number of components used in a conventional multilevel inverter, a small advancement can be made in this arena. Initially, by comparing the structures of modified MLI with the conventional one and by evaluating the harmonics developed by both of them, we could conclude that the modified MLI demonstrates reduced harmonics than conventional system and thereby we can speculate that the modified MLI is more advantageous and compact than conventional cascaded H bridge multilevel inverter.

7. ACKNOWLEDGMENT

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