Design of Symmetrical Seven Level Multi Level Inverter

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ABSTRACT

The major problem of conversion using power electronic switches is harmonic content at the output. Harmonics can be minimized by decreasing the number of switches by cascaded multilevel inverter (CMLI). The developed topology requires eight switches for seven level inverter will produce same output as conventional one. SVPWM technique is instigated to generate gate pulse to switches. The multilevel inverter perform well in both positive and negative half cycles as well as performance parameters improved in reducing total harmonic distortion in output voltage. The proposed MLI model compared and verified by MATLAB.

Keywords: Metal Oxide Semiconductor Field Effect Transistor (MOSFET), Multi Level Inverter (MLI), H-Bridge (H-B), Total Harmonic Distortion (THD), Cascaded Multi Level Inverter (CMLI), Space Vector Pulse Width modulation (SVPWM) etc.

1. INTRODUCTION

In recent days, industries and domestic consumers required electricity with high power quality and more reliability. Conventional two level inverters are operated at high frequency to reduce the switching losses and harmonic distortion which leads to poor efficiency. Hence the implementation of MLI in industries have been increased, as it exhibits reduced THD. Cascaded multilevel inverter includes DC source with low frequency transformer and switches. The topology designed with seven level MLI and eight switches produce conventional Output. In cascaded H-bridge MLI topology, all units will have same value of dc voltages. Use of extra electronic switches and dc sources become complex in control technique. The symmetrical topology with eight switches and single voltage source can be connected in series by three capacitors.

2.FULL BRIDGE CONVERTER

The reduced switches of MLI produced seven level output like bridge rectifier uses number of switches as eight which results reduce switching losses. The voltage divider is made of three capacitor connected in series. After passing power through the capacitor the voltage divider divides the supply voltage and then supplied to the H-bridge made of MOSFETs and four diodes.

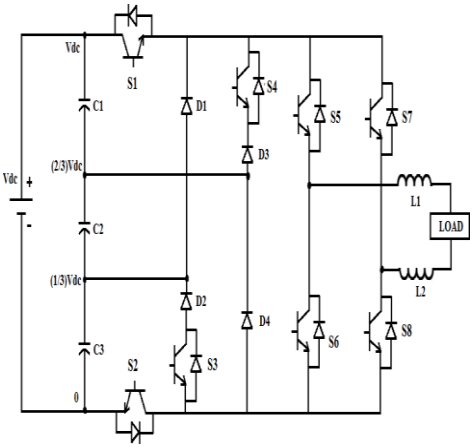

Fig No.1: FULL BRIDGE CONVERTER

MODE 1

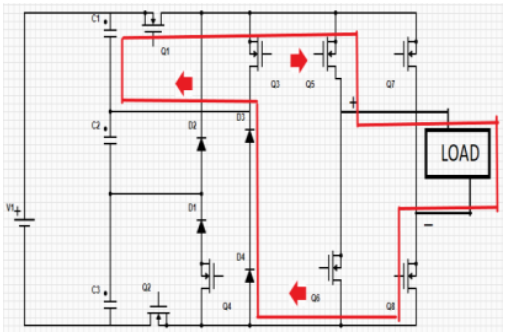

Fig No.2

For the output voltage level, $V_0 = \frac{1}{3} V_i$, the MOSFET 1 is operate only ON during first half cycle. The MOSFET 5 and MOSFET 8 are also operated and the energy is delivered by capacitor C1 i.e. $\frac{1}{3} V_i$.

MODE 2

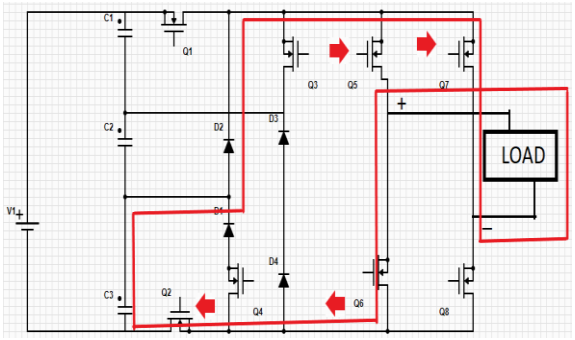

Fig No.3

For the output voltage level, $V_0 = \frac{2}{3}V_i$, the MOSFET 1 and MOSFET 4 are operated as ON state during first half cycle . The MOSFET 5 and MOSFET 8 are also operated as ON state and the energy is delivered by capacitor C1 and C2 i.e. $\frac{2}{3}V_i$.

MODE 3

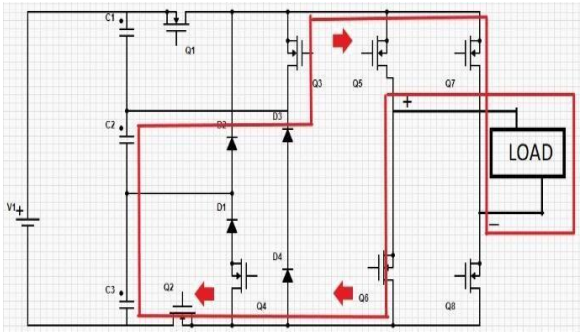

Fig No.4

For the output voltage level, $V_0 = V_i$, the MOSFET 1 and MOSFET 2 are operated ON state during first half cycle . The MOSFET 5 and MOSFET 8 are also switched ON and energy is delivered by capacitor C1, C2 and C3 i.e. V_i.

MODE 4

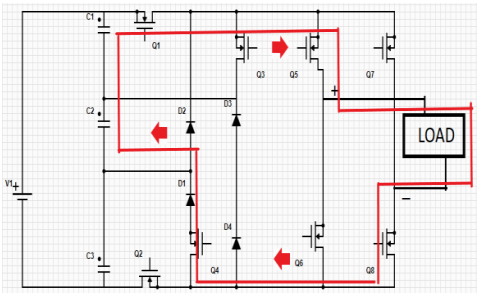

Fig No.5

For the output voltage level, $V_0 = -\frac{1}{3}V_i$, the MOSFET 2 is operated ON for the first half cycle. The switches MOSFET 6 and MOSFET 7 are also operated ON state and the energy is delivered by capacitor C3 i.e. $-\frac{1}{3}V_i$.

MODE 5

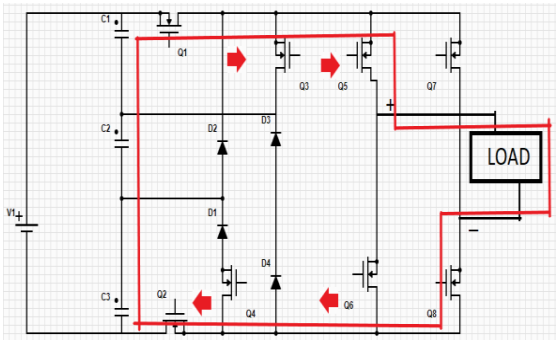

Fig No.5

For the output voltage level, $V_0 = -\frac{2}{3}V_i$, the MOSFET 2 and MOSFET 3 are operated on state during second half cycle. The switches MOSFET 6 and MOSFET 7 are operated on state during first half cycle and the energy is delivered by capacitor C3 and C2 i.e.- $\frac{2}{3}V_i$.

MODE 6

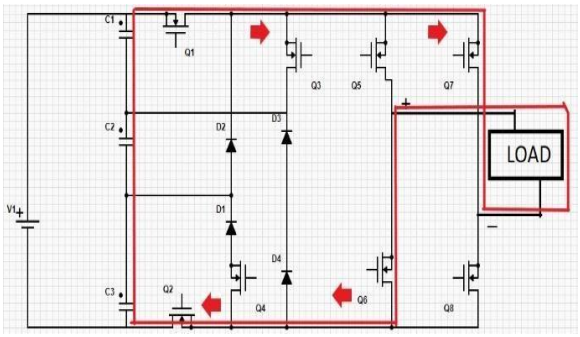

Fig No.6

For the output voltage level, $V_0 = -V_i$, the MOSFET 2 and MOSFET 1 are operated ON state. The MOSFET 6 and MOSFETT 7 are also operated ON state during first half cycle and the energy is delivered by capacitor C1, C2 and C3 i.e. - V_i.

3. SIMULATION

The input voltages obtained for the seven levels Multi level inverter are 0, V_i,1/3V_i,2/3V_i,-V_i,-1/3V_i,-2/3V_i.

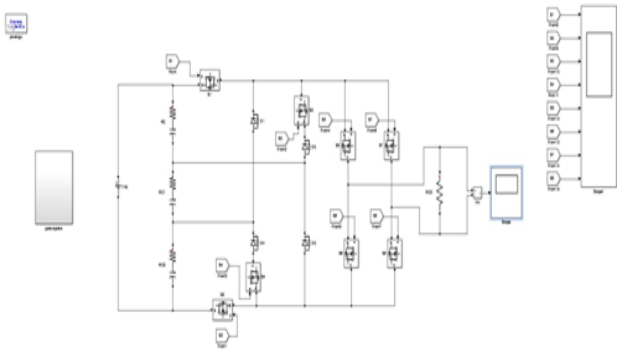

Fig No.7 Simulation circuit of 7 Level MLI

V0	S1	S2	S3	S4	S5	S6	S7	S8	C1	C2	C3
1/3Vi	1	0	0	0	1	0	0	1	1	0	0
2/3 Vi	1	0	0	1	1	0	0	1	1	1	0
Vi	1	1	0	0	1	0	0	1	1	1	1
0	0	0	0	0	1	0	1	0	0	0	0
-1/3 Vi	0	1	0	0	0	1	1	0	0	0	1
-2/3 Vi	0	1	1	0	0	1	1	0	0	1	1
-Vi	1	1	0	0	0	1	1	0	1	1	1

Table- 1 Output voltage levels for proposed 7-level MLI

4. CONCLUSION

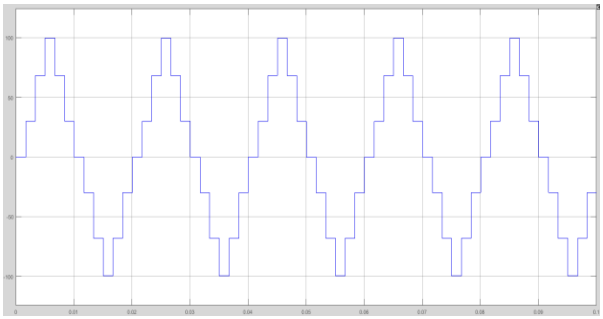

Fig No.8 Output voltage waveform

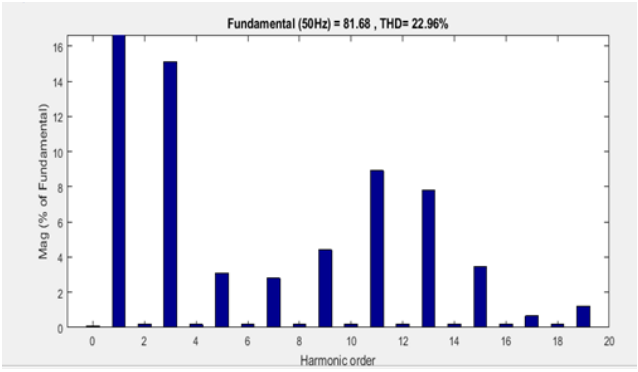

Fig No.9 Simulation result of 7 Level MLI

In this project THD value is reduced to 22.96 percent from 33.96 percent because of the proposed topology uses minimum number of switches. The lower order harmonics can also eliminated by using conventional static harmonic elimination technique. By using eight switches and single DC source.

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