Analog/RF Performance of Dielectric Pocket Double Gate (DP-DG) AlGaN/GaN MOSHEMT

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Abstract - *In this study, we have signified and interpreted various RF in preference to analog performance of a 80nm gate length AlGaN/GaN metal oxide semiconductor high electron mobility transistor grown on increasing –K dielectric oxide material with numerical modeling based on TCAD simulation. Wideband AlGaN and narrowband GaN layers are used as the device channel in single gate devices, along with SiO_2, Al_2O_3, HfO_2 are used as the high –K gate dielectrics. For improve DC performance, low gate leakage current and improve RF drain current, further double gate and dielectric pocket double gate MOSHEMTs have been designed. Specifically, a HfO_2 dielectric MOSHEMTs have shown excellent RF performance such as high drain current (I_D), high drain conductance (g_d), high trans-conductance (g_m), high intrinsic gain (A_V) and maximum cut-off frequency (f_T). All the results of modeling and simulation are created by VISUAL TCAD simulator and hence, obtained up to the mark in terms of analog and sub-millimeter wave applications. Here, the effective oxide thickness is specified at 3nm for SiO_2, 6nm for Al_2O_3 and 10nm for HfO_2 gate dielectric MOSHEMT device. The proposed HfO_2 gate DP-DG MOSHEMT device shown higher-up performance like threshold voltage of -2V, high current in drain region (I_D) of 8500mA/mm, high output conductance (g_d) of 2300mS/mm, high transconductance (g_m) of 3600mS/mm, intrinsic gain (A_V) of 21.82dB and maximum cut-off frequency (f_T) of 1.95THz at V_{DS} 5V corresponding to SG MOSHEMT and DG MOSHEMT. The performance of the device is significantly enhanced by the high –K AlGaN/GaN based DP-DG MOSHEMT.*

***Key Words*: GaN, AlGaN, SG MOSHEMT, DG MOSHEMT, DP-DG MOSHEMT, high –K, HfO_2**

1. INTRODUCTION

The heterojunction is created by two distinct materials, namely aluminium gallium nitride and gallium nitride, in the High-Electron-Mobility Transistor (HEMT), too noted as the two-dimensional Electron Gas Field Effect Transistor (TEGFET) and the Heterostructure Field-Effect Transistor (HFET) [1]. A potential well forms in the conduction band on the GaN side of the interface attributable to the significant bandgap energy contrast in the middle of AlGaN and GaN. The AlGaN layer's electrons will transfer to the GaN layer, where they will be restricted close to the polarization-procured electric field to produce a fine conduction layer. This surface of electrons is declared as the Two-Dimensional Electron Gas (2DEG). In contrast to the MOS Field-Effect Transistor (MOSFET), electrons from 2DEG can move without colliding with impurities because the GaN layer is undoped. As a result, the transistor can achieve high electron mobility, which should lead to lower noise figures [1- 3]. The first HEMT to be manufactured was a GaAs/AlGaAs HEMT. High-frequency performance is often better in devices with more indium, although gallium nitride HEMTs have gained popularity in recent years due to their high-power performance [3]. The advantages of HEMTs comprise their high gain, which drives them competent as amplifiers, high-level switching speeds made possible by the fact that majority carriers dominate the charge carriers in modulation doped FETs (MODFET), while minority carriers are only moderately involved, and exceptionally low noise values generated by the fact that current fluctuation in these devices is minimal in comparison to other devices [4, 5].

When compared to other materials, the GaN material has a variety of special characteristics. For instance, its breakdown field is a substantially larger than GaAs and Si, and its electron mobility is approximately twice of silicon. GaN's huge bandgap also makes it possible for a GaN transistor to operate at high temperatures (like 300 °C), whereas the silicon device's functionality is constrained [1-4]. GaN-based devices have many benefits, including good energy density (> 1000 mW/mm), multi-octave radio band, high-up efficiency (> 50%), linearity, moderate phase noise and low noise factors. GaN has an high degree of polarity and is a polar material. As a result, the end faces of the crystal accumulate sheet charge. Although it's possible that the overall channel charge will be three to four times greater than that of an AlGaAs/GaAs based HEMT. The research is crucial for creating a model for high-level speed and power applications [5, 6].

Single-gate MOS-HEMT simulation and fabrication have been the subject of several studies [7, 8]. Device performance has improved in devices with several heterostructures, including AlGaN/GaN, InP/InGaAs and AlInN/GaN [4][7][8]. The impression of different high –K gate dielectric, like HfO_2, Al_2O_3 and ZrO_2 on the gate leakage

current were explored in [8-10]. Also, the effect of low –K dielectric oxide was investigated in [16, 17]. Pardeshi et al. [15] have detailed the DC investingation of an underlapping dual gate MOS-HEMT and comparability with a silicon underlap MOSFET. Gate stacked and double gate MOSHEMT and MOSFET was also analyzed in [9-14]. Different device structures such as gate recessed MISHEMT was designed and investigated in [18]. By taking different gate shapes and atomic layer deposition of different oxides in AlGaN/GaN MOHEMT was designed in [19].

The double-gate controllability in [11] improves current density and transconductance, which improves the model's performance in expressions of half-power frequency (f_T), higher frequency of oscillation (f_{max}), and noise parameters compared to its single-gate equivalent. In [20], GAA MOSFET and dielectric pocket GAA MOSFET have been compared and found that due to dielectric pocket DPGAA has better immunity towards SCEs and also leakage current is seen suppressed with temperature variation.

The categorization of paper is as follows. With the help of various oxide materials, we have shown the AlGaN/GaN based single gate MOSHEMT. We further simulated double gate and dielectric pocket double gate MOSHEMTs to compare and evaluate the analog and linearity performances. The device architectures and modelling equations are described in Sections II and III. In Section IV, the simulated results of SG MOSHEMTs are compared and discussed. By keeping the same device dimensions, the transfer characteristics of SG MOSHEMT are compared with DG and DP-DG MOSHEMTs. Finally in Section V, the finding is explained.

2. DEVICE STRUCTURES AND DIMENSIONS

Figure 1(a) displays the partial view of $Al_{0.2}Ga_{0.8}N$/GaN based single gate MOSHEMT. There are three different oxide materials have been used in SG device and have dielectric constant 3.9 for SiO_2, 8.5 for Al_2O_3, and 25 for HfO_2. For investigating the impact of high –K dielectric material, devices with a fixed gate length (L_g) of 80nm at source/drain ends are operated. The source and drain consist of Al metal and gate consists of NpolySi metal which is deposited on the high –K dielectric metal. To keep the AlGaN barrier layer's Al content at 0.2 and retain its positive GaN/AlGaN interface properties. In this device, GaN performs as a channel layer and AlGaN performs as a barrier layer. Impurity scattering is lessened using the undoped layer's function [7]. In figure 1(b), double gate MOSHEMT is designed with same GaN channel, barrier length, and the length of gate, gate-source, also gate-drain as SG MOSHEMT to improve the DC and RF performance. Further, in figure 1(c), for better performance dielectric pocket technology has been used in DG MOSHEMT. HfO_2 has been used in dielectric pocket with the length DP_L = 60nm and thickness DP_T = 80nm nearby the source-channel and drain-channel interface [20]. By using the linear interpolation method, the physical properties of $Al_X Ga_{(1-X)} N$ material can be expressed as,

$$Al_X Ga_{(1-X)} N = X \cdot AlN + (1-X) GaN \quad (1)$$

2.1 Single Gate MOSHEMT

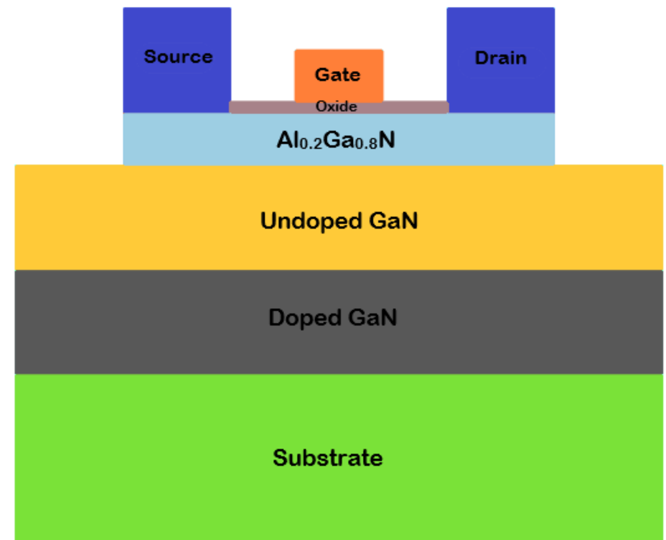

Fig -1(a): Proposed HfO_2 gate dielectric SG MOSHEMT structure [7]

2.2 Double Gate MOSHEMT

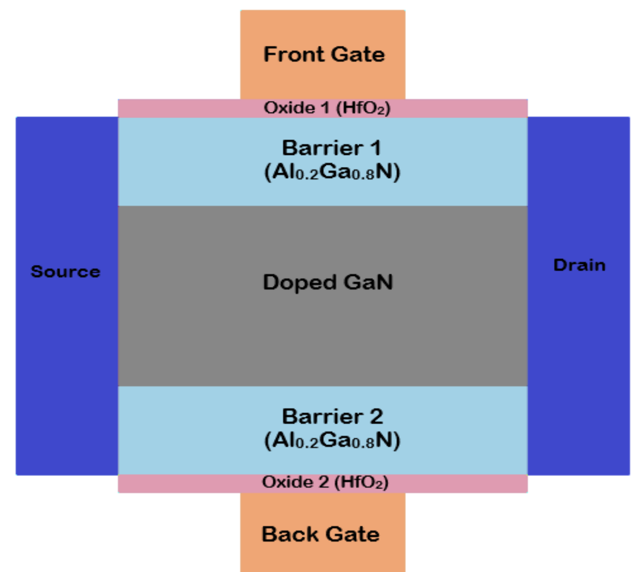

Fig -1(b): HfO_2 gate dielectric DG MOSHEMT structure

In table 1, effective oxide thickness (EOT), represented by T_{OX}, is the gate oxide thickness of the SiO_2 layer of a transistor that would be needed to attain comparable electrical

performance as the high –K material is employed. The effective oxide thickness can be calculated using following formula,

$$\text{EOT} = t_{\text{high-}k}\left(\frac{k_{SiO_2}}{k_{\text{high-}k}}\right) \tag{2}$$

Table -1: Oxide thickness of different device structures

Oxide Material	SG MOSHEMT		DG MOSHEMT		DP-DG MOSHEMT	
	EOT	T_{OX}	EOT	T_{OX}	EOT	T_{OX}
SiO_2	3nm	3nm	--	--	--	--
Al_2O_3	3nm	6nm	--	--	--	--
HfO_2	3nm	10nm	3nm	10nm	3nm	10nm

Table -2: Device Structure Parameters

PARAMETER NAME	Single Gate	Double Gate	Dielectric Pocket Double Gate
Length of gate (L_g)	80nm	80nm	80nm
Length of source (L_s)	100nm	100nm	100nm
Length of drain (L_d)	100nm	100nm	100nm
Length of channel (L_c)	200nm	200nm	200nm
Drain doping (n+ type) (N_d)	10^{18} cm^{-3}	10^{18} cm^{-3}	10^{18} cm^{-3}
Source doping (n+ type) (N_d)	10^{18} cm^{-3}	10^{18} cm^{-3}	10^{18} cm^{-3}
Channel doping (p type) (N_a)	10^{12} cm^{-3}	10^{12} cm^{-3}	10^{12} cm^{-3}
Gate-source spacing (L_{gs})	100nm	100nm	100nm
Gate-drain spacing (L_{gd})	100nm	100nm	100nm
Barrier thickness (T_{BOX})	50nm	50nm	50nm
Undoped GaN thickness (T_{UOX})	100nm	--	--
C- doped GaN (p type) (N_a)	10^{16} cm^{-3}	10^{16} cm^{-3}	10^{16} cm^{-3}

For investigating the analog as an alternative RF performance of the SG, DG and dielectric pocket double gate MOSHEMT devices, all the parameters such as, gate length, source/drain length, HfO_2 oxide thickness, barrier, and GaN channel thickness are kept same as single gate MOSHEMT.

2.3 Dielectric Pocket Double Gate MOSHEMT

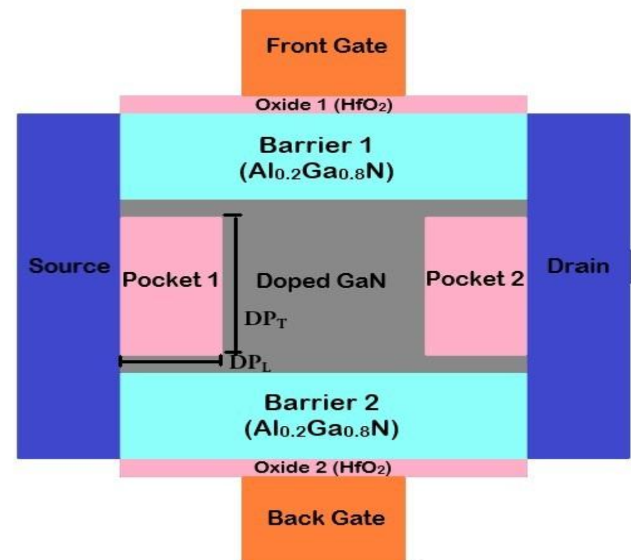

Fig -1(c): HfO_2 dielectric pocket double gate MOSHEMT structure

3. MODELING EQUATIONS

The gate voltage at which the least carrier charge density extends a specific esteem to bring off switch on the on state is known as the threshold voltage (V_T). The constant drain current (I_D) approach of V_T extortion, which is often used in numerical simulation and investigational estimations, is equal to this definition [21].

The threshold voltage can be demonstrated as,

$$V_T = \phi_{GC} - 2\phi_F - \frac{Q_B}{C_{OX}} - \frac{Q_{2DEG}}{C_{OX}} \tag{3}$$

Where, ϕ_{GC} is the work function distinction connecting the gate and the channel, ϕ_F is the Fermi potential of the gate, Q_B is the depletion region charge density, Q_{2DEG} is the 2DEG region charge density and C_{OX} is the oxide capacitance.

Depending on the gate material, the work function difference for polysilicon gate is,

$$\phi_{GC} = \phi_F(\text{Substrate}) - \phi_F(\text{Gate}) \tag{4}$$

Fermi potential for the p-type substrate is,

$$\phi_F = \frac{kT}{q} \ln \frac{n_i}{N_A} \quad (5)$$

The depletion region charge density can be calculated by using following formula.

$$Q_B = -\sqrt{2qN_A \varepsilon_{GaN} \left| -2\phi_{F(substrate)} \right|} \quad (6)$$

Here, the depletion region charge density is -8.83×10^{-8}C/cm^2 and the Fermi potential for polysilicon gate is 0.55V.

The 2DEG region charge density can be calculated,

$$Q_{2DEG} = C_{OX}\left(V_{GS} - V_T - V_{CH}\right) \quad (7)$$

Calculation of capacitance oxide,

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{\varepsilon_r \cdot \varepsilon_o}{t_{ox}} \quad (8)$$

Here, ε_r is relative permittivity or dielectric constant, ε_o is permittivity of free space, and t_{ox} is oxide thickness. V_{GS} and V_{CH} are gate to source along with channel voltages.

3.1 Calculation of drain current of n-channel MOSHEMT

The drain current equation has been derived under the following voltage assumption [21].

$$\begin{aligned} &V_{GS} \geq V_T \\ &V_{GD} = V_{GS} - V_{DS} \geq V_T \\ &V_{DS} \geq V_{DSAT} = V_{GS} - V_T \end{aligned} \quad (9)$$

Here, V_{GS} and V_{DS} are gate to source along with drain to source voltages, V_{GD} is gate to drain voltage and V_{DSAT} is saturation drain voltage.

Now, C_{OX} and V_T from Equation (8) and (3) can be calculated in drain current equations for MOSHEMT in linear mode.

For $V_{GS} \geq V_T$ and $V_{DS} < V_{GS} - V_T$,

$$I_{D,lin} = \frac{\mu_{n_{GaN}} \cdot C_{ox}}{2} \cdot \frac{W}{L_c} \cdot \left[2\cdot\left(V_{GS} - V_T\right)V_{DS} - V_{DS}^{\ 2}\right] \quad (10)$$

Where, $\mu_{n_{GaN}}$ is the electron mobility in GaN, L_c is the length of channel and W used as the width of the channel.

Similarly, for $V_{GS} \geq V_T$ and $V_{DS} \geq V_{GS} - V_T$ the current equation in saturation mode is stated by,

$$I_{D,sat} = \frac{\mu_{n_{GaN}} \cdot C_{ox}}{2} \cdot \frac{W}{L_c} \cdot \left(V_{GS} - V_T\right)^2 \quad (11)$$

For cut-off region,

$I_D = 0$, Where $V_{GS} < V_T$ (12)

3.2 Calculation of Analog/RF parameters for MOSHEMT

The output-conductance (g_d), trans-conductance (g_m), trans-conductance generation factor (TGF), intrinsic gain (A_V), and cut-off frequency (f_T) are ultimate crucial factors in terms of analog/RF performance [6].

The fraction of the change in I_D to the change in V_{GS} with steady V_{DS} is called gate transconductance (g_m). Similarly, the ratio of drain current I_D variation to drain voltage V_{DS} and constant gate voltage V_{GS} is known as output or drain conductance (g_d). The numerical equations has been used to measure trans-conductance are as follows:

$g_m = \frac{\partial I_D}{\partial V_{GS}}$, Where V_{DS} is constant. (13)

$g_d = \frac{\partial I_D}{\partial V_{DS}}$, Where V_{GS} is constant. (14)

The transconductance generation factor conveys how well the current is used to produce a specific transconductance value. The mathematical equation used to measure TGF is,

$$TGF = \frac{g_m}{I_D} \quad (15)$$

The intrinsic gain is directly corresponding to the transconductance and to the value of the drain resistor.

$$\begin{aligned} &A_V = \frac{g_m}{g_d} \\ &\Rightarrow A_V = g_m \cdot r_0 \end{aligned} \quad (16)$$

Where, r_0 is drain resistor.

Cut-off frequency or break frequency (f_T) is one of the most significant factors in determining the device's RF performances. Generally, f_T is the frequency of an input signal at which the current gain is unity [6].

$$f_T = \frac{g_m}{2\pi C_g} \quad (17)$$

Where, gate capacitance $C_g = C_{ox} \cdot W \cdot L$

4. RESULTS AND DISCUSSIONS

The precision and effectiveness of a model structure depend on the precise meshing, size, and parameter selection with precise measurements. A fine meshing is employed for device simulations at key places like the channel and source/drain edge. For each and every proposed structure, the results are produced.

4.1 DC and Analog performance of the Single Gate MOSHEMT

In this section, the simulation results of SG device with three different oxide materials are compared and described. Figure 2(a), 2(b) and 2(c) represent a good match between simulated and theoretical output current-drain voltage characteristic curves (I_D-V_D) of SiO_2, Al_2O_3 and HfO_2 gate dielectric MOSHEMT in linear scale for different gate voltages. The mobility of carriers, which is influenced according to the doping concentrations, is an important factor of the drain current.

The GaN/AlGaN based SG devices have appeared high electron mobility in the scale 100 to 800 cm^2/V-sec. Figure 2(c) displays highest I_D at V_{GS}=3V is simulated at 700mA/mm for HfO_2 gate dielectric MOSHEMT while for SiO_2 and Al_2O_3, I_{Dmax} are 400mA/mm and 350mA/mm. It reveals that the HfO_2 gate dielectric layout has an elevated ON current as compared to SiO_2 and Al_2O_3 gate dielectric structures. The HfO_2 device indicated a highest current density of 440mA/mm at V_{GS}=2V and 180mA/mm at V_{GS}=1V. The three different oxide materials structured devices are pinched-off completely which means $V_{GS} < V_T$ and the devices are in OFF state at V_{GS}=0V.

Figure 3 displays the drain conductance-drain voltage characteristic curves (g_d-V_D) of SiO_2, Al_2O_3 and HfO_2 gate dielectric MOSHEMT for V_{GS}=3V. Maximum output conductance at V_{GS}=3V is 170mS/mm for HfO_2 gate dielectric MOSHEMT while for SiO_2 and Al_2O_3, g_{dmax} are 100mS/mm and 115mS/mm.

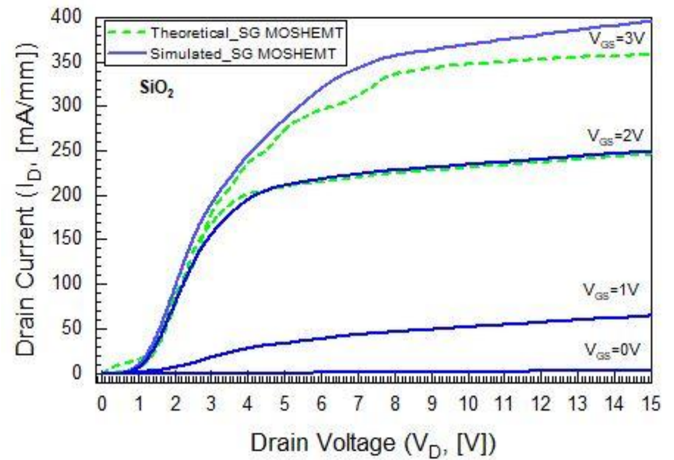

Fig -2(a): I_D-V_D characteristic curves of SiO_2 at gate voltages 0V to 3V.

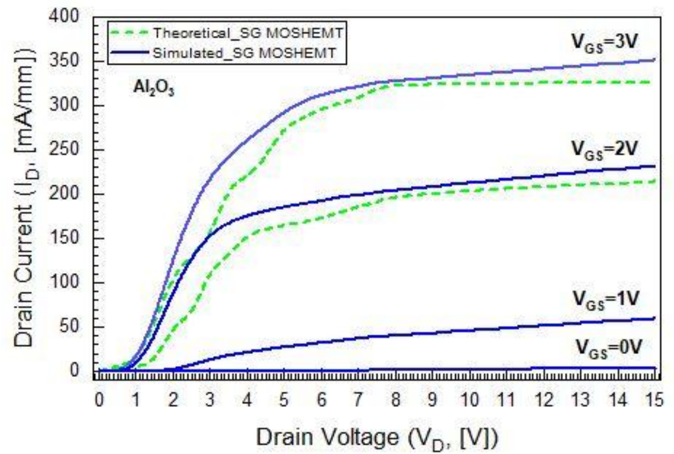

Fig -2(b): I_D-V_D characteristic curves of Al_2O_3 at gate voltages 0V to 3V.

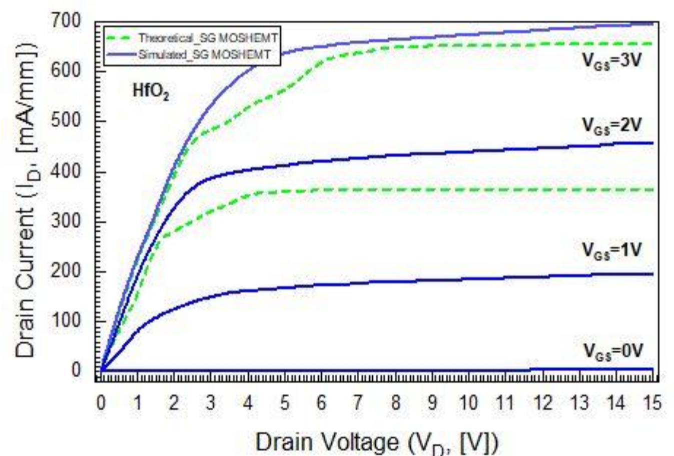

Fig -2(c): I_D-V_D characteristic curves of HfO_2 at gate voltages 0V to 3V.

Figure 4, represents the drain current (I_D-V_G) together with transconductance (g_m-V_G) with respect to gate voltage characteristic curves of SiO_2, Al_2O_3 and HfO_2 gate dielectric MOSHEMT in linear scale at constant drain voltage 5V. Here, the ON current elevates as gate dielectric constant of the structure increases. The OFF current decreases as the V_T also decreases. Due to increase in dielectric constant, capacitance oxide also increases and hence, the drain current reaches maximum at high –K dielectric. This proves the equations (10) and (11), in which drain current is directly proportional to dielectric constant and capacitance oxide and inversely proportional to threshold voltage. For output current-gate voltage (I_D-V_G), figure (4) shows maximum drain current is 800mA/mm for HfO_2 gate dielectric MOSHEMT while for SiO_2 and Al_2O_3, I_{Dmax} are 320mA/mm and 350mA/mm. For transconductance-gate voltage (g_m-V_G), maximum transconductance at V_{DS}=5V is 370mS/mm for HfO_2 gate dielectric MOSHEMT while for SiO_2 and Al_2O_3, g_{dmax} are 190mS/mm and 160mS/mm.

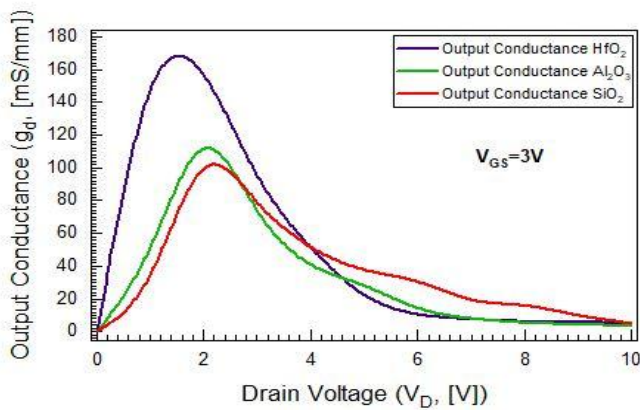

Fig -3: Comparative (g_d-V_D) characteristic curves between SiO_2, Al_2O_3, and HfO_2 dielectric SG MOSHEMTs at V_{GS}=3V

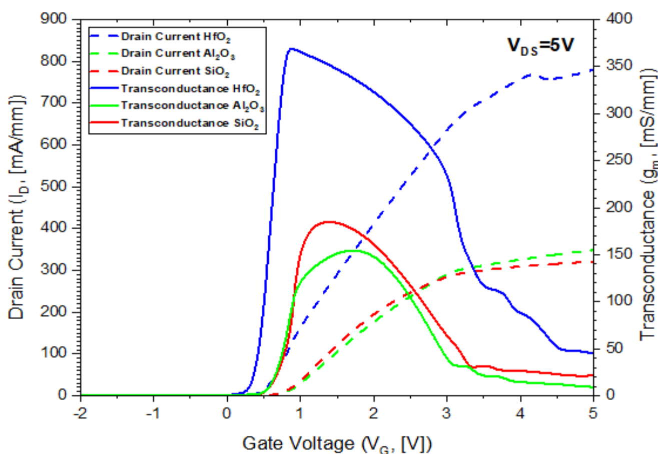

Fig -4: Comparative (I_D-V_G) and (g_m-V_G) characteristic curves between SiO_2, Al_2O_3, and HfO_2 dielectric SG MOSHEMTs

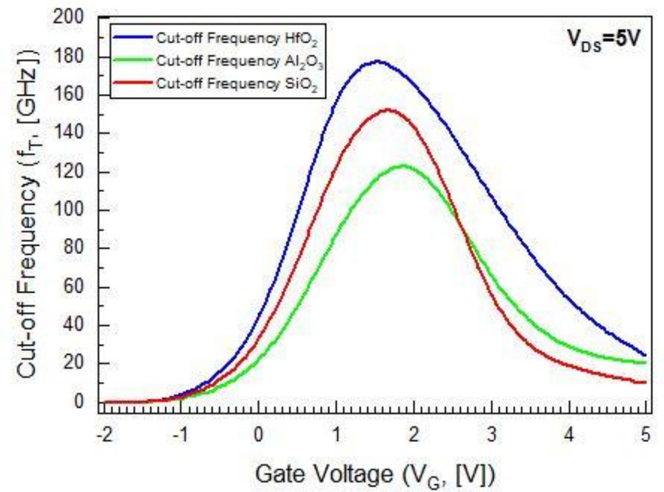

Fig -5: Comparative (f_T-V_G) characteristic curves between SiO_2, Al_2O_3, and HfO_2 dielectric SG MOSHEMTs

Table -3: Comparative analysis of SiO_2, Al_2O_3 and HfO_2 gate dielectric SG MOSHEMT

Oxide Material	SiO_2	Al_2O_3	HfO_2
Dielectric Constant (K)	3.9	8.5	25
I_D (Max.) at V_{GS}=3V [mA/mm]	400	350	700
I_D (Max.) at V_{DS}=5V [mA/mm]	320	350	800
g_d (Max.) [mS/mm]	100	115	170
g_m (Max.) [mS/mm]	190	160	370
f_T (Max.) [GHz]	145	120	180

Figure (5) represents the cutoff frequency- gate voltage (f_T-V_G) characteristics curve, which shows maximum f_T at 180GHz for HfO_2 gate dielectric MOSHEMT. But, the SiO_2 gate dielectric has better frequency as compare to Al_2O_3 gate dielectric. In transconductance (g_m) plot, SiO_2 gate dielectric has also better transconductance than Al_2O_3 gate dielectric. Hence, it demonstrates that transconductance is directly proportional to cut-off frequency, which satisfies the equation (17).

From the table (3), it is observed that, out of these three structures, HfO_2 gate dielectric MOSHEMT has shown excellent DC and analog performance. The primary causes responsible for using high –K dielectric materials are larger physical thickness than SiO_2, and provide high ON currents.

4.2 DC and Analog/RF performance of HfO_2 gate dielectric single gate, double gate and dielectric pocket double gate MOSHEMTs

Considering analog/RF performance, the most important parameters are the trans-conductance (g_m), output-

conductance (g_d), trans-conductance generation factor (TGF), intrinsic gain (A_V), and cut-off frequency (f_T) to be compared and analyzed between HfO_2 gate dielectric single gate, double gate and dielectric pocket double gate MOSHEMTs.

Figure 6, shows an appropriate match between the comparative simulated and theoretical threshold voltages of SiO_2, Al_2O_3 and HfO_2 dielectric single gate MOSHEMTs, HfO_2 dielectric DG and DP-DG MOSHEMTs. It is observed that, SG device structures have positive threshold voltages, where as DG and DP-DG device posses negative V_T. So, for normally OFF operations SG MOSHEMT structure is the appropriate choice due to positive threshold. As we can see, if dielectric constant increases threshold voltage decreases and hence, drain current also increases [20]. In figure 7(a), at V_{GS}=3V, DP-DG device has the highest drain current of 8000mA/mm and output conductance of 2300mS/mm as compared to DG MOSHEMT. At V_{DS}=5V, figure 7(b) compares the transfer properties of HfO_2 dielectric SG, DG and DP-DG MOSHEMTs on a linear scale. From this result, the I_{ON}/I_{OFF} current ratio in DP-DG MOSHEMT was subsequently improved which clearly shows that the existence of dielectric pockets reduces the charge sharing at the interfaces of the source-channel as well as drain-channel and, consequently, the I_{OFF} current [20].

Figure (8), explores by varying in transconductance generation factor of HfO_2 dielectric SG, DG and DP-DG MOSHEMTs against gate to source voltage at V_{DS}=5V. It can be noticed from the figure (8) that, SG MOSHEMT has higher TGF, which is considered to be highly efficient. Higher TGF leads the device performances increases and can operate at low supply voltage. For TGF between $10V^{-1}$ and $5V^{-1}$ variations with V_{GS} from -1V to 1.5V typically used for analog performance [20].

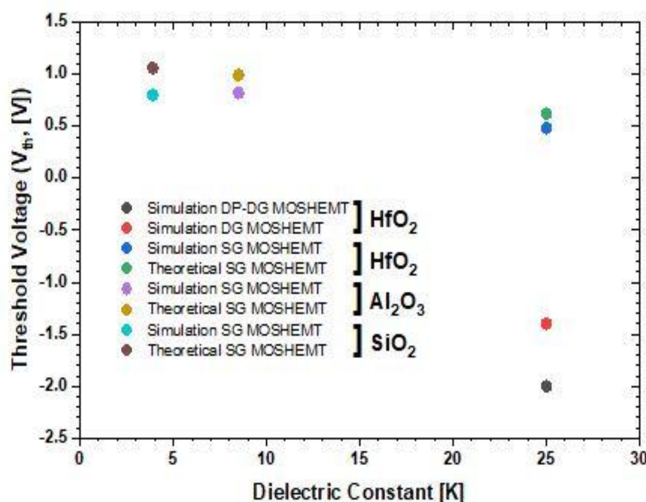

Fig -6: Comparison of (V_T -K) between dielectric SG, DG and DP-DG MOSHEMTs

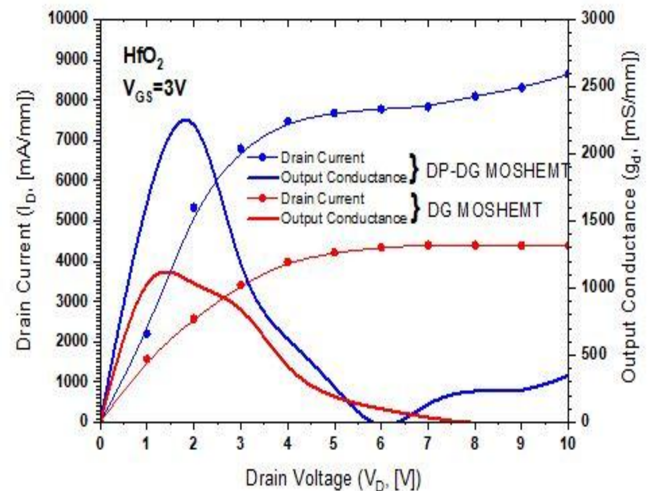

Fig -7(a): Comparative (I_D -V_D) and (g_d-V_D) characteristic curves between HfO_2 dielectric DG and DP-DG MOSHEMTs

Additionally shown in figure (9), relation to gate to source voltage (V_{GS}) is the device's intrinsic gain, which is the transconductance to output conductance ratio for different device structures at V_{DS}=5V. Here, DP-DG MOSHEMT reduces the gain while improving the device's linearity.

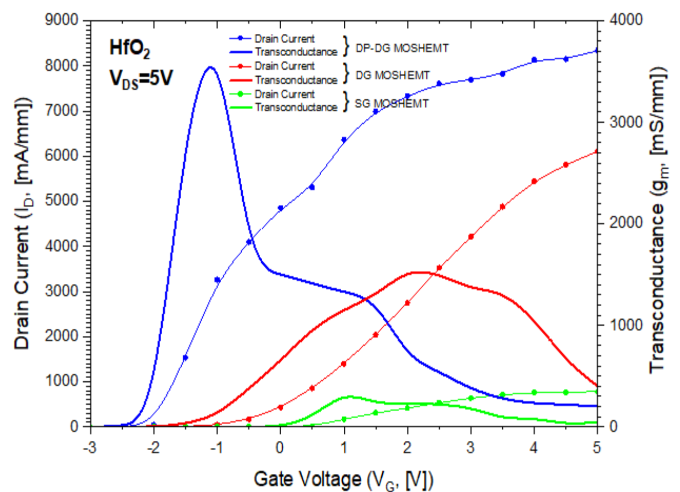

Fig -7(b): Comparative (I_D –V_G) and (g_m-V_G) characteristic curves between HfO_2 dielectric SG, DG and DP-DG MOSHEMTs

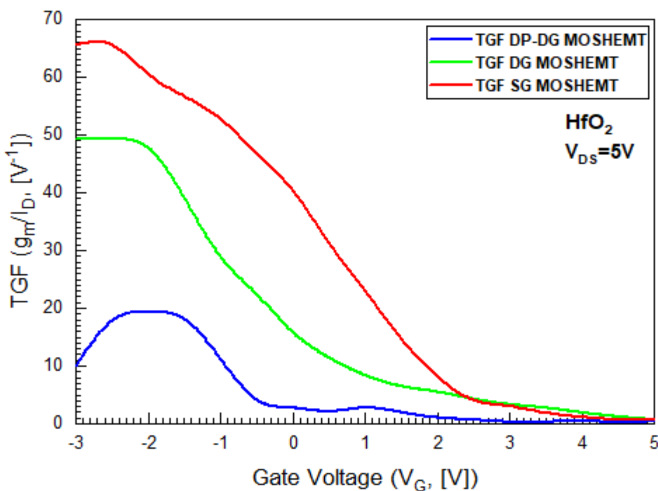

Fig -8: Comparative TGF variation with V_{GS} between HfO_2 dielectric SG, DG and DP-DG MOSHEMTs

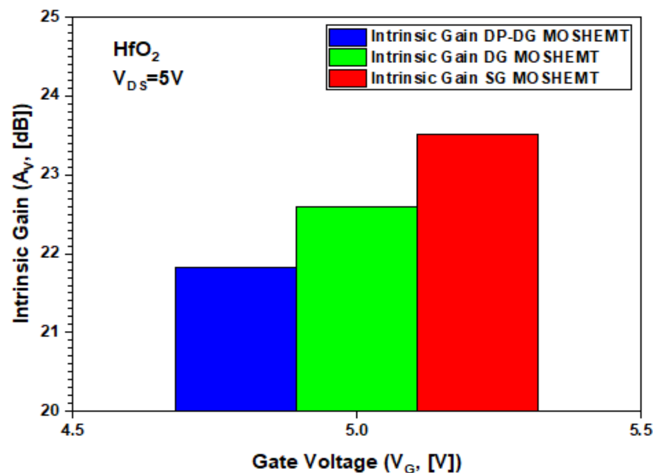

Fig -9: Comparative maximum intrinsic gain variation with V_{GS} between HfO_2 dielectric SG, DG and DP-DG MOSHEMTs

For estimating the radio frequency performance of the device, cut-off frequency is one of the most significant specifications. From figure (10), the deviation of cut-off frequency can be observed in respect of gate to source voltage (V_{GS}) to the order of V_{DS}=5V. Here, the higher value of cut-off frequency obtained at 1.95THz for the dielectric pocket double gate device. By virtue of the previous statements, the g_m value is high for DP-DG MOSHEMT and low for SG MOSHEMT. As per the above reference it is understandable that g_m and f_T are exactly sustained by the drain current. Figure (11) displays the modification of channel potential across the channel from source to drain side for SG, DG and DP-DG device structures. For SG model, the work function of gate material (NPolySi) is better at the drain edge. But, for DG layout, the work function of gate material is better at the source side and for DP-DG layout, the work function of gate material is better at source as well as drain end. The figure (11) shows that, at the drain end DG MOSHEMT has been the negligible channel potential curve amidst the three which signifies that DG structure sustains from minimal amount of hot carrier effect [22].

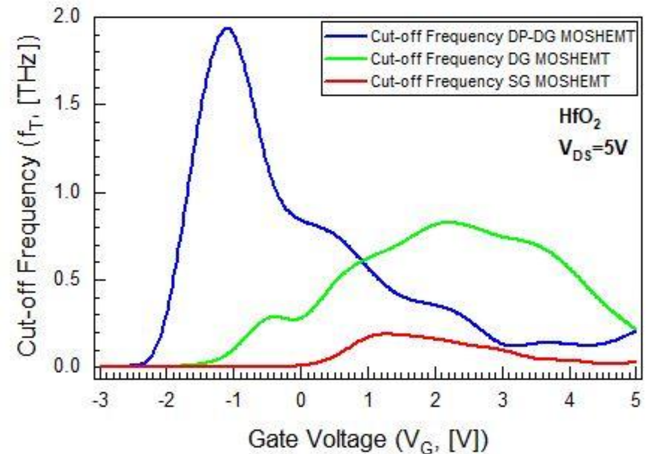

Fig -10: Comparative cut-off frequency variation with V_{GS} between HfO_2 dielectric SG, DG and DP-DG MOSHEMTs

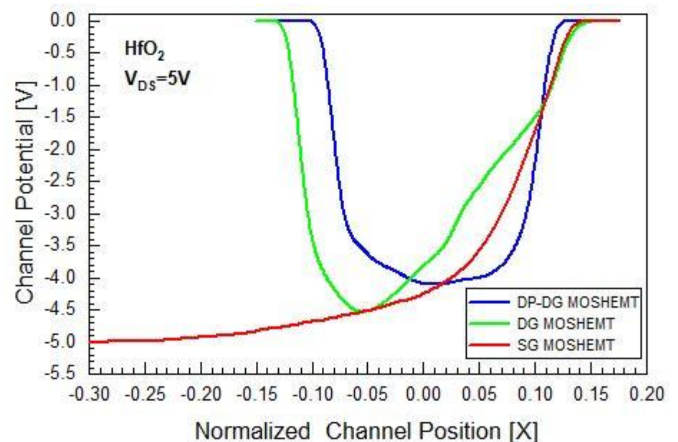

Fig -11: Comparative channel potential deviation with normalized channel position between HfO_2 dielectric SG, DG and DP-DG MOSHEMTs

Figure (12), depicts the energy band diagram of the AlGaN/GaN formed DP-DG MOSHEMT. The device's conduction band deviates from the Fermi level (E_F), forming a well across the interface. That well is known as quantum/ potential well [8]. It shows that, 2DEG has been formatted with electrons supplied by surface donor states in DP-DG device [12]. Table (4) compares the RF/Analog parameters of this work using HfO_2 dielectric.

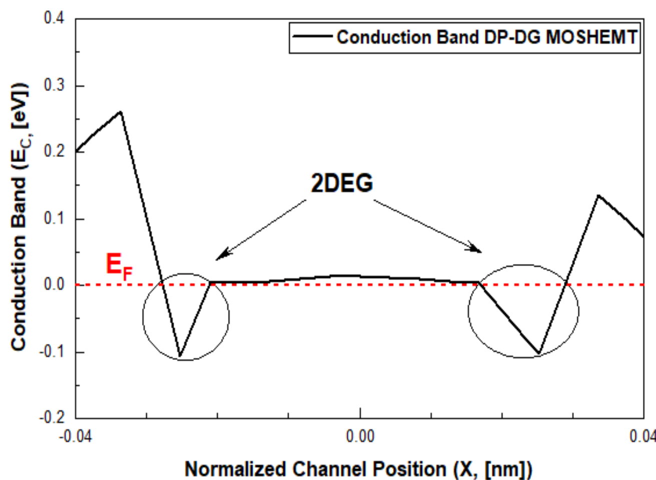

Fig -12: The proposed AlGaN/GaN heterostructure-based DP-DG MOSHEMT's band structure outline

Table -4: Comparative analysis of HfO_2 gate dielectric SG, DG and DP-DG MOSHEMTs

Device Structures	Single Gate	Double Gate	Dielectric Pocket Double Gate
Threshold Voltage (V_T, [V])	0.48	-1.4	-2
I_D (Max.) at V_{GS}=3V [mA/mm]	700	4500	8000
I_D (Max.) at V_{DS}=5V [mA/mm]	800	6000	8500
g_d (Max.) V_{GS}=3V [mS/mm]	170	1200	2300
g_m (Max.) V_{DS}=5V [mS/mm]	370	1600	3600
TGF, V_{DS}=5V [V^{-1}]	65	50	19
Intrinsic gain (A_V, [dB])	23.52	22.6	21.82
f_T (Max.) [THz]	0.18	0.8	1.95

From the above experiments, it is concluded that for RF/Analog performance high –K dielectric material is more preferable because of its better control over the channel electrons as well as larger physical thickness than low –K dielectric. By using high –K dielectric, the DP-DG MOSHEMT structure has been performed better because of dielectric pocket technology. Even if, it has been low TGF and gain, but it provides maximum transconductance and cut-off frequency. Simultaneously, it can be easily seen in SG and DG MOSHEMT, stronger TGF results in improved device efficiency and preferable gain performance at lesser voltages.

5. INTERPRETATION

This paper presents a modified study of the analog/RF characteristics for the AlGaN/GaN SG MOSHEMT and further, DG and DP-DG MOSHEMTs are contemplated and analyzed by using device design guidelines. By maintaining a constant channel length and gate length, the effects of high –K dielectric on device performance have been investigated considering DC, analog, and RF applications. Our calculated and simulated results in SG device show that HfO_2 gate dielectric will be preferable for analog and RF performance. By keeping the same device dimensions, further HfO_2 dielectric DG and DP-DG MOSHEMTs have been designed and observed. With reference to RF and analog applications, the devices need to be operated in above threshold regime. From the simulated results, DP-DG device has lowest threshold voltage and hence, I_{OFF} current is also decreasing. Due to the implementation of dielectric pocket in DG MOSHEMT, it alleviates the charge sharing at the interfaces of the source as well as drain-channel, and hence, ON current is maximum and observed at 8500mA/mm. Similarly, in DP-DG device the output conductance is increased by 91.66%, and transconductance is enhanced by 125% from DG MOSHEMT. But, in case of TGF and intrinsic gain [A_V], SG device has been performed more efficiently and it can be operated at low supply voltage. But, it is observed that DP-DG device has maximum frequency of 1.95 THz, which can be used in sub-millimeter wave applications. Hence, the present DP-DG MOSHEMT using HfO_2 gate dielectric leads to further improvement in TGF and intrinsic gain as it is providing superior transfer characteristics. The performance of SG, DG, and DP-DG MOSHEMTs can be enhanced by adjusting the other device parameters in accordance with the requirements of the applications.

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