Impact of Gate Length Modulation On a $Al_{0.83}Ga_{0.17}N$/GaN Dual Double Gate MOSHEMT for Radio Frequency Application

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Abstract - *This work come across the capable strength of comparison of AlGaN/GaN under lap DG MOS-HEMT and Dual DG MOS-HEMT with variation of different gate length and has been investigated in Visual TCAD simulation. The device channel is a wideband mesh-matched channel. of $Al_{0.83}Ga_{0.17}N$ and slender band Gallium Nitride sheet, along with SiO_2, Al_2O_3 and high-K HfO_2 as the dielectric of gate. The key device performance parameters of analog and RF analysis is completed for a variety of different gate length (L_g). In scaling down of gate length (L_g) then increment in the drain current (I_D), cut-off frequency (f_T), trans-conductance (g_m) happen and reduced in intrinsic gain (Av) and trans-conductance generation factor(g_m/I_D) with respect to 1nm oxide thicknesses. The use of the double 2-DEG hetero-structure helps to obtain outstanding device linearity and it also give the higher current according to gate length and from this simulation work we have revealed that the Dual Double Gate MOS-HEMT's drain current is very high than DG MOS-HEMT drain current i.e. 66.67%, and also found the peak cutoff frequency of approx 1766 GHz in DDG-MOSHEMT. These results denote the capability of $Al_{0.83}Ga_{0.17}N$/GaN based Dual Double Gate MOSHEMT can be acceptable replacement for high current and high-frequency performance.*

Key Words: DG MOS-HEMT, DDG MOS-HEMT, Gate Length, AlGaN/GaN 2-DEG hetero-structure, TGF, Intrinsic gain, Cutoff frequency.

1. INTRODUCTION

High electron mobility transistors based on AlGaN/GaN are the best transistor for high frequency implementation (HEMTs)[1]. Because of the different band-gap energies, an $Al_xGa_{1-x}N$/GaN hetero-structure is produced when the AlGaN barrier is formed on a reasonably thick layer of GaN. [2-6]. In the upper region of the GaN layer, close to the boundary, the band bends, and electrons form a two-dimensional conductive channel [7,8]. The 2-dimensional electron gas (2DEG)[9] features, which arise at the $Al_xGa_{1-x}N$/GaN hetero-structure without the need for any doping and are used to increase the frequency execution of AlGaN/GaN HEMTs, govern the execution of AlGaN/GaN HEMTs[10].By adding holes from the [p-type] AlGaN to the hetero-structure of AlGaN and GaN, the 2DEG density is raised. This can lead to conductivity modulation.$Al_xGa_{1-x}N$ with Al formation of about 0.83 and GaN formation of about 0.17, and high-quality $Al_xGa_{1-x}N$/GaN hetero-structure[11]been fill out by the process of metal organic chemical vapor deposition (MOCVD).

Double Gate MOSFET structure has single material[12] that revealed increased exemption to short channel effects, but Double Gate MOS-HEMT hetero-structure[13-17] has III-V hetero-structure layer into the channel offer high drain current. HEMTs are used in SoCs and it also known for low noise amplifiers and high drain current applications. HEMT transistors are unique and it is able to operate at very higher frequency than ordinary transistors, in low power amplifiers, satellite receivers, mobile phones, voltage converters, radar equipment, as well as in the defense sector. It is also employed in high-frequency goods like these.

As far as we are aware, 2-DEG's RF performance of AlGaN/GaN hetero-structure based Dual Double Gate MOS-HEMT device with variation of gate length has not been demonstrated yet. So we investigated the parameters such as I_D, g_m, TGF (g_m/I_D), intrinsic gain (Av) and f_T and comparable to the specifications of DG MOS-HEMT and its range of gate lengths(L_g).

2. DEVICE STRUCTURE

We have observed the production of Al0.83Ga0.17 N/GaN under lap DG and DDG MOS-HEMT device having the varying gate length of 12 nm,15nm, 18nm, 21nm and 3 nm, 4 nm and 5 nm respectively. The proposed structure Fig. I & II is two AlGaN barriers followed by Gallium Nitride hetero layer. Based on the creation of both AlGaN/GaN interfaces, there is double 2-DEG, two AlGaN/GaN heterostructures exist. The device body consist of barrier thickness(T_b) and channel

thickness(T_{ch}) with upper and lower barrier thickness(T_b) of 3nm and channel thickness of 10nm, where T_{si} = T_{Ch} + $2.T_b$. The conduction band edge of the AlGaN layer is offset with respect to the channel, and reducing traps at the interface through mesh matching with the GaN layer. The lengths of the source and drain are fixed. Lun = 5 nm, and the high-K HfO_2 dielectric material's are of 1nm for both upper and lower gate oxide thicknesses (T_{ox}). Both the structure consist of gate with different length i.e in DG MOS-HEMT there is 12nm, 15nm, 18nm and 21nm gate length is used while in DDG MOS-HEMT3nm, 4nm and 5nm gate length is used and they having width of 1um and consists of material Al with maximum mesh size 0.1um. The n-type doping concentration in the source and drain regions is high N_D = 10^{18} cm^{-3} and the valuation of device structure is enumerated in TABLE I & II.

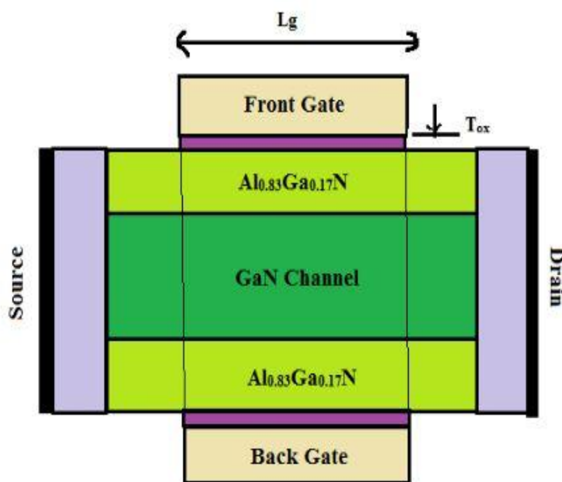

Fig-1: Cross section of an$Al_xGa_{1-x}N$/GaN based DG MOS-HEMT [10].

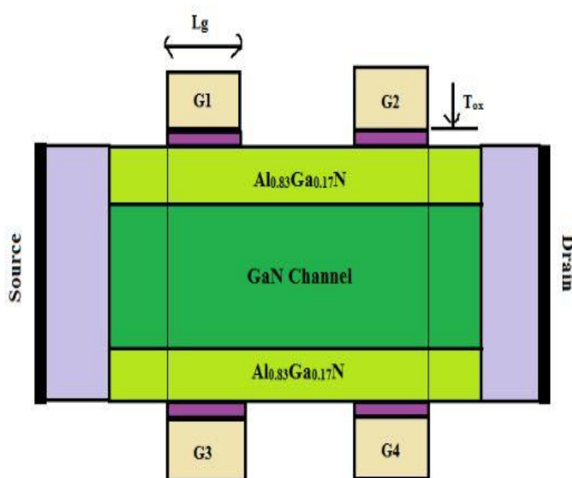

Fig-2: Proposed structure of $Al_xGa_{1-x}N$/GaN based DDG MOS-HEMT.

Table-1: Device Structure Parameters

Parameter	**Value**
Gate length (L_g)	12nm,15nm, 18nm, 21nm(For DG) and 3nm,4nm,5nm(For DDG)
Underlap length (L_{un})	5nm
AlGaN layer thickness (T_b)	3nm
GaN layer thickness(T_{ch})	10nm
Oxide layer thickness(T_{ox})	1nm

Table-2: Parameters and it's Doping Profile

Doping Profile	**Value**
Source [n^+-Type]	10^{18} cm^{-3}
Drain [n^+-Type]	10^{18} cm^{-3}
Channel [p-Type]	10^{17} cm^{-3}
Barrier Thickness (T_b)	10^{17} cm^{-3}

3. RESULT AND DISCUSSION

3.1 Variation of Gate Voltage with respect to Drain Current with different Gate Lengths and Comparison of Transconductance values

The I_D-V_g output characteristics of a symmetrical underlap DG and Dual DG MOS-HEMT are observed using Visual TCAD at variation of different lengths of gate voltages(V_g) is varied from -1 V to 1.5 V with a pace of 0.05 V with constant drain voltage 1V. The current increases when the gate-to-source potential is changed because there are more carriers, or 2-DEG, in the channel.

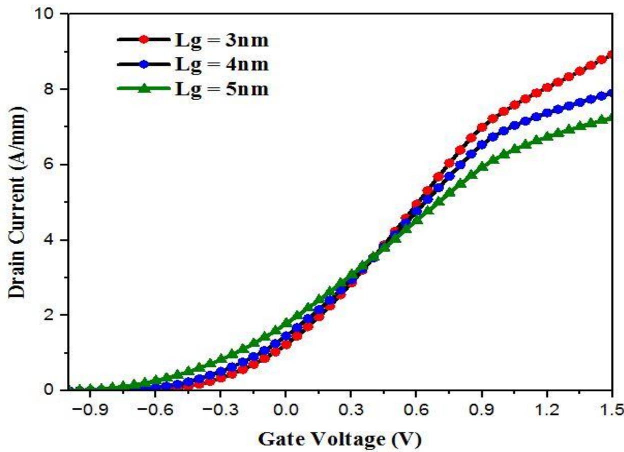

Fig-3: I_D-V_g characteristic of Dual DG MOS-HEMT at different gate voltages where L_g = (3,4,5)nm with 1nm oxide thickness.

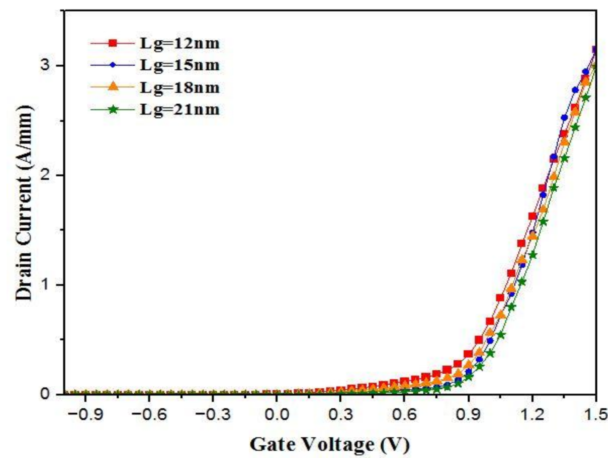

Fig-4: I_D-V_g characteristic of DG MOS-HEMT at distinct gate voltages where L_g = (12,15,18,21)nm with 1nm oxide thickness.

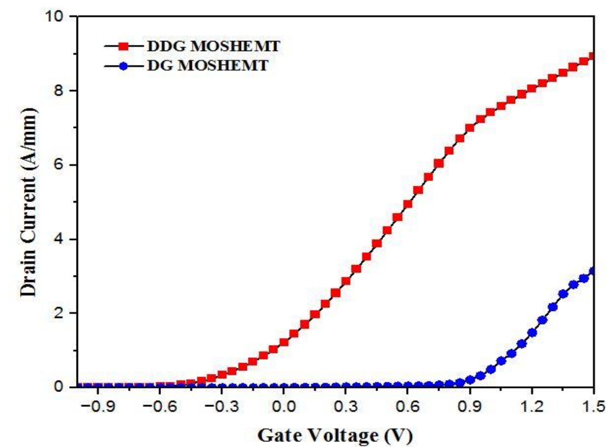

Fig-5: I_D-V_g characteristic of DG and Dual DG MOS-HEMT at 1nm oxide thickness.

Table-3: Drain Current Comparison For DG and Dual DG MOS-HEMT

Double Gate	**Dual Double Gate**	**ΔIds** $= \frac{I_{ds(DDG)} - I_{ds(DG)}}{I_{ds(DDG)}} X\ 100$
0.003A/um	0.009A/um	66.67%

Here we observed, the effect of scaling down of gate length is cause of the increment in drain current and at 3nm gate length I_D is about 0.009A/um (9A/mm)and at 12nm gate length I_D is about 0.003A/um (3A/mm) of two different MOS-HEMTs that is Dual DG and DG respectively and at1nm T_{ox}, the drain current of Dual DG is 66.67% more than DG MOS-HEMT. Comparing with an existing paper[10] the I_D is 0.0025A/um which is lower value.

A transconductance gives current with directly proportional to its input voltage. Transconductance is the proportion of alteration of drain current to the alteration of gate voltage. Comparing both the MOS-HEMTs with different gate lengths and we observed the plot between gate voltage and transconductance in Fig.6

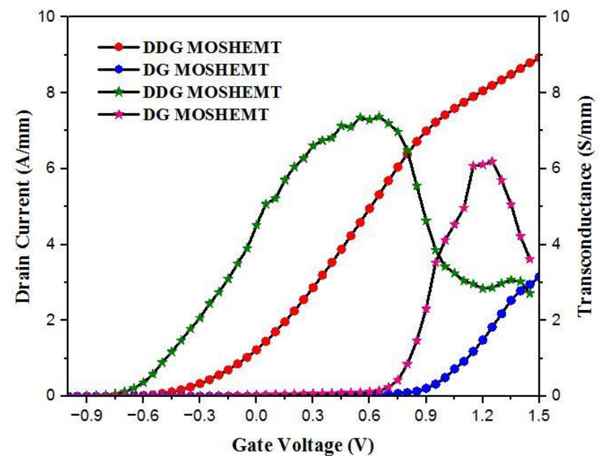

Fig-6: I_D-V_g and Transconductance characteristic of DG and Dual DG MOS-HEMT at 1nm oxide thickness.

Table-4: Observation of Transconductance at 1nm Oxide Thickness

L_g=12nm	L_g=3nm
6.2×10^{-3}	7.37×10^{-3}

After observing the transconductance values and take the transconductance peak values of both MOS-HEMTs we found that an increase in transconductance is caused by a decrease in gate length. Approximately 16% higher

transconductance of Dual DG MOS-HEMT than DG MOS-HEMT. The significance of g_m is that if more transconductance then amplification will also greater.

3.2 Variation of Drain Voltage with respect to Drain Current with different Gate Length and Comparison of conductance values

The I_D-V_D features of a symmetrical system's output under lap DG and Dual DG MOS-HEMT are observed using Visual TCAD at drain voltage (V_D) is varied from 0V to 1V with a step of 0.01 V with constant gate voltage (V_g) 0V. When the drain bias is low, when the drain bias is large, the carrier density depends on the saturated drive current, and the linear drive current is exactly proportional to the conductance.

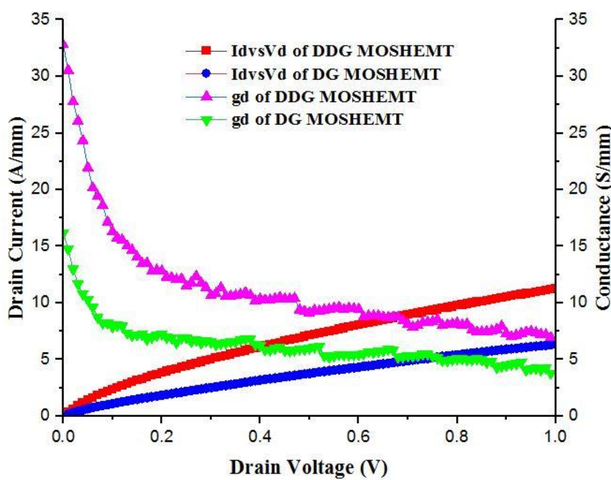

Fig-7: I_D-V_D and conductance characteristic of DG and Dual DG MOS-HEMT at 1nm oxide thickness.

A) Model Equations:

The drain current equation of a n-channel MOS-HEMT in cut-off region is,

$$I_D = 0 \qquad \text{Where,} [\, V_{GS} < V_T] \qquad (1)$$

The drain current equation of a n-channel MOS-HEMT in linear region is,

$$I_{DLin} = \frac{\mu_n . C_{ox}}{2} . \frac{W}{L_G} . [\, 2(V_{GS} - V_T)V_{DS} - {V_{DS}}^2] \qquad (2)$$

$$\text{Where, } [\, V_{GS} \geq V_T \text{and} V_{DS} < V_{GS} - V_T \,]$$

The drain current equation of a n-channel MOS-HEMT in saturation region is,

$$I_{DSat} = \frac{\mu_n . C_{ox}}{2} . \frac{W}{L_G} . (V_{GS} - V_T)^2 \qquad (3)$$

$$\text{Where, } [\, V_{GS} \geq V_T \text{and} V_{DS} \geq V_{GS} - V_T \,]$$

Here, C_{ox} is the oxide capacitance of device, I_D is the drain current, W is the device width, L_G is gate length, μ_n is the electron mobility, V_{GS} is gate to source voltage while V_{DS} is drain to source voltage and V_T is threshold voltage.

Capacitance Oxide of the device is,

$$C_{ox} = \frac{\varepsilon_{ox}}{T_{ox}} = \frac{\varepsilon_r . \epsilon_0}{T_{ox}} \qquad (4)$$

Where ε_r= relative permittivity or dielectric persistent of high-K dielectric material,$\varepsilon_0$is the constant permittivity of 8.854×10^{-12} F/m and T_{ox} is oxide width of device.

3.3 Comparison of High-K HfO2 dielectric with SiO2and Al2O3

High-K materials such as HfO_2, ZrO_2 and TiO_2 have high K values that is higher than 3.9. This high-*k* material that is HfO_2 is responsible for increase the transistor drive current and the transistor switching speed.

Table-5: Values of Dielectric Material

Dielectric Material	Constant Value
HfO_2	25
SiO_2	3.9
Al_2O_3	9

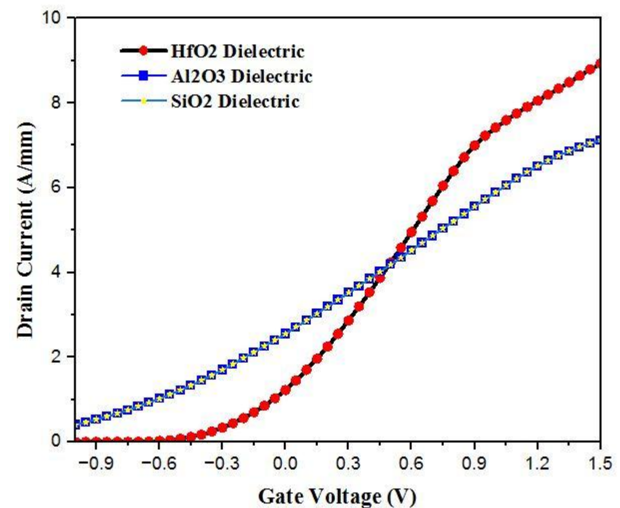

Fig-8: Comparison of different dielectric of I_D-V_g characteristic of Dual DG MOS-HEMT at 3nm gate length at different gate voltages with 1nm oxide thickness.

Table-6: Observation of Drain Current of Different Dielectric Constant

Dielectric Material	Id [A/um]
HfO_2	0.0087
SiO_2	0.0069
Al_2O_3	0.007

3.4 RF Analysis

In this work, we observing the effect of L_g on the small-signal RF parameters like cut-off frequency (f_T), transconductance generation factor (1/V), transconductance (g_m) and intrinsic gain (Av). The frequency f_T is the one at which the current gain equals one. A major role for high-speed digital applications is the f_T.

A) Model Equations:

The proportion of the variation the drain current to the alteration of the gate voltage with constant drain voltage is known as trans-conductance (g_m), and the proportion of the variation of the drain current to the alteration of the drain voltage with persistent gate voltage is known as conductance (g_d).

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \quad \text{Where, } V_{DS} \text{ is constant} \tag{5}$$

$$g_d = \frac{\partial I_D}{\partial V_{DS}} \quad \text{Where, } V_{GS} \text{ is constant} \tag{6}$$

For RF applications, the cut-off frequency is,

$$f_T = \frac{g_m}{2.\pi.C_G} \tag{7}$$

$$C_G = C_{ox}.W.L_G \tag{8}$$

Where, g_m is the transconductance and g_d is the output conductance. C_G is the total gate capacitance.

B) DG and Dual DG MOSHEMT Transconductance Generation Factor Comparison

Transconductance generation factor (TGF) is the proportion of g_m to I_D and is an major parameter for analog applications. TGF determine the available gain. Where g_m stands for gain and Id stands for consumption. A low TGF means that the capacitive load circuit consumes a lot of power due to the reduced input drive capacity. As L_g decreases I_D increases and because this TGF decreases.

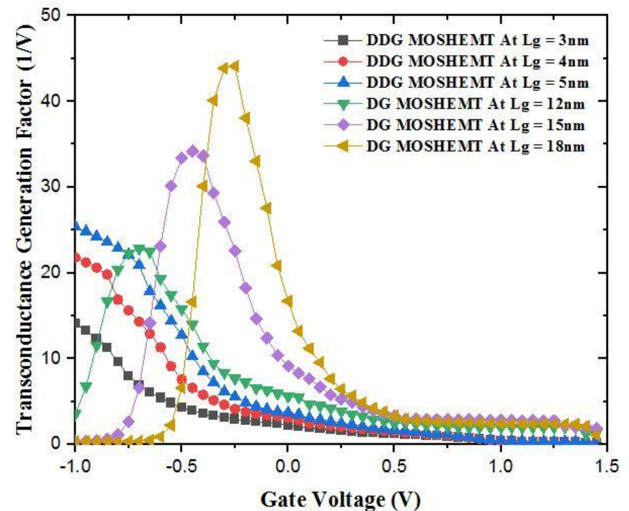

Fig-9: Comparison of TGF of Dual DG and DG MOS-HEMT at [3,4,5]nm and [12,15,18]nm gate length respectively at different gate voltages with 1nm oxide thickness.

Here, we observed that the peak TGF value of DG MOS-HEMT is 44.1V^{-1} at L_g = 18nm and lower value of 22.5V^{-1} at L_g = 12nm , while in Dual DG MOS-HEMT upper TGF value is 25.4V^{-1} at L_g = 5nm and lower value of 14.12V^{-1} at L_g = 3nm. So reduction in gate length is responsible for reduction in TGF and this we observed from Fig.9.

C) Comparison of Intrinsic Gain of both DG and Dual DG MOSHEMT

For circuits like as operational amplifiers, instrumentation amplifiers, and others that call for significant increases, the inherent gain of a MOSHEMT is a crucial number. You can think of intrinsic gain as the product of g_m and Ro.

$$Gain = g_m.R_o \quad \text{Where, } R_o = \frac{1}{g_d} \tag{9}$$

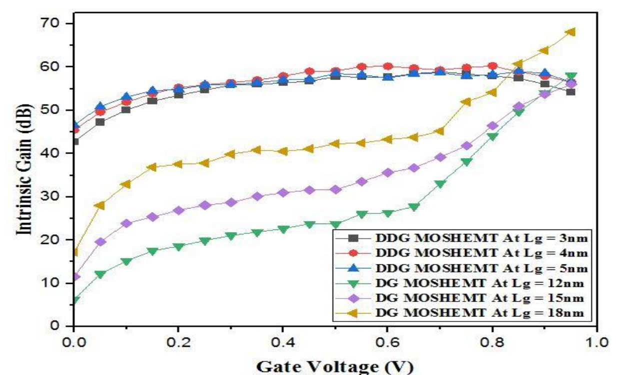

Fig-10: Comparison of Intrinsic gain of Dual DG and DG MOS-HEMT at [3,4,5]nm and [12,15,18]nm gate length respectively at different gate voltages with 1nm oxide thickness.

Here, we observed that the peak gain value of DG MOS-HEMT is 68dB at L_g = 18nm and lower value of 56 dB at

L_g = 15nm , while in Dual DG MOS-HEMT upper gain value is 60.3dB at L_g = 4nm and lower value of 59dB at L_g = 3nm. From above valuation we concluded that the gain of Dual DG MOS-HEMT is bit more than DG MOS-HEMT. As we know how much of gate length is decrease then the intrinsic gain is also decrease and this proposed theory plot graphically in Fig.10.

D) Effect of Energy Band and Surface Potential in AlGaN/GaN Interface

The valence band of the AlGaN barrier approaches the Fermi level at the surface when the thickness of the AlGaN area is raised. This makes it easier for electrons to move from the AlGaN barrier's valence band to the conduction band of GaN, which leads to a concentration of holes at the surface. As a result, at the surface, a positive sheet charge forms, and at the AlGaN/GaN interface, a corresponding negative sheet charge (2DEG) does the same.

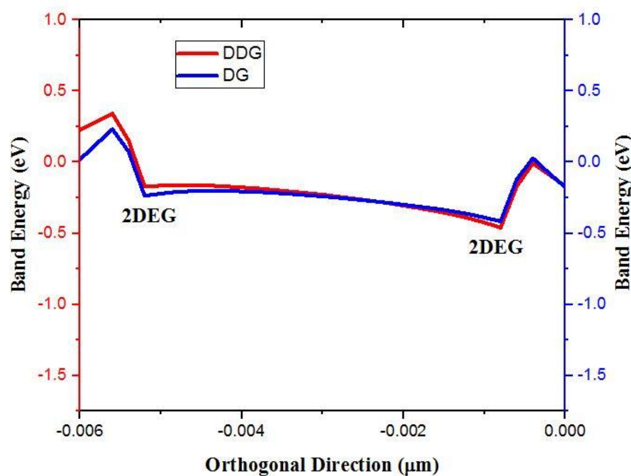

Fig-11: Band structure diagram of the Dual DG MOS-HEMT and DG-MOSHEMT based AlGaN/GaN heterostructure.

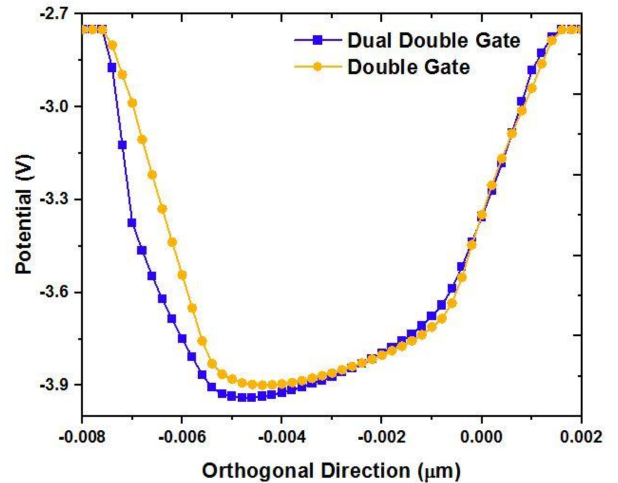

Fig-12: Surface Potential diagram of the Dual DG MOS-HEMT and DG-MOSHEMT based AlGaN/GaN heterostructure.

From above Fig.11&12, the double 2-DEG is present on both side of the AlGaN/GaN interface and it goes below to 0 value and forms corresponding negative sheet charge and the potential of this heterostructure is also comes good.

E) Comparison of Cut-Off Frequency of both DG and Dual DG MOSHEMT

The cut-off frequency (f_T) is a main parameter for high-speed digital applications and for high-frequency amplifier tuning. For downscaling of different gate lengths of both the MOS-HEMTs devices causes high frequency.

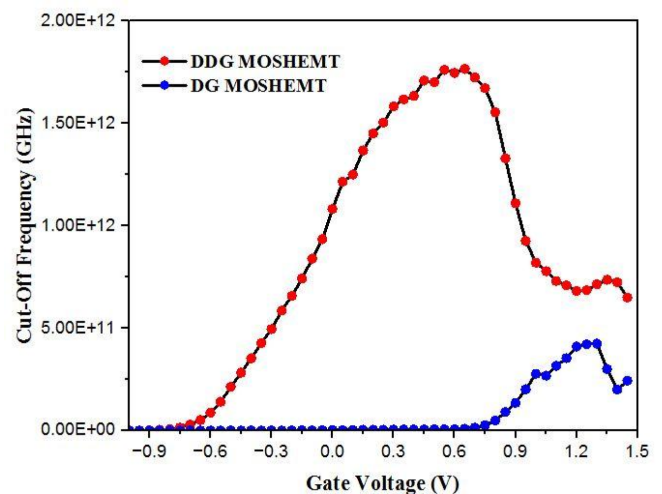

Fig-13: Comparison of Cut-off frequency of Dual DG and DG MOS-HEMT at 3nm and 12nm gate length respectively at different gate voltages with 1nm oxide thickness.

Table-7: Observation of Cut-Off Frequency of 1nm Oxide Thickness with Different Gate Length

L_g	
3nm	***12nm***
1766.4	424.2

Here, we found that the peak f_T value of DG MOS-HEMT is 424.2 GHz at L_g = 12nm, while in Dual DG MOS-HEMT peak value is 1766GHz. So we concluded from TABLE VII. that the downscaling of gate length very important and for this high frequency range it used in modern technologies like in telecommunication sector to prevent interference between different users and it is working at sub-millimeter wave frequencies up to THz range.

4. CONCLUSION

Using Visual TCAD simulation, the Radio Frequency operation of AlGaN/GaN hetero-structure DG and Dual DG MOS-HEMTs is investigated for various types of gate lengths. The newly proposed $Al_xGa_{1-x}N$/GaN Dual DG MOS-HEMT heterostructure for observing various RF parameters with less gate length and compared it to with DG MOS-HEMT's parameters and it has also different gate lengths. In this paper, we observed how a device is more reliable and give better performance by downscaling the gate length (Lg).This simulation results specified that, the $Al_xGa_{1-x}N$/GaN Dual DG MOS-HEMT give more drain current at 3nm gate , while DG MOS-HEMT obtain this at 12nm gate length of 1nm oxide thickness. However, the $Al_xGa_{1-x}N$/GaN MOS-HEMTs require Dual DG formation to control the SCEs flaw brought on by their small electron effective mass and narrow band gap. A greater linearity is achieved by the development of a double 2-DEG at both hetero interfaces, which increases the transconductance with a double-hump characteristic. In this work we took 1nm oxide thickness and observed each at different gate lengths. We found that when gate length (L_g) decreases in the drain current(I_D), trans-conductance (g_m) and cut-off frequency (f_T) increases. We observed the highest drain current i.e.0.009A/um (9mA/um) at 1nm oxide thickness from I_D-V_g characteristic. The peak transconductance value is 7.37 × 10^{-3} S/um at 3nm gate length with minimum oxide thickness and for this g_m value the cutoff frequency is also higher in number i.e. approx 1766GHz (1.7 THz) and for this the potential of using $Al_xGa_{1-x}N$/GaN Dual DG MOS-HEMT is useful device community and for sub-millimeter wave antenna application, at defense sector for communication purpose.

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