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LOW POWER BASED TERNARY HALF ADDER USING FIN TYPE FIELD EFFECT TRANSISTOR TECHNOLOGY

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Abstract - *In this research, we investigate a low-power ternary half adder based on FinFET technology. In this article, FinFET is used to demonstrate a ternary half adder that is low-power, low-leakage, and low-frequency. According to this paper, the latency, peak power distribution, and leakage power of ternary adders with and without Fin Type Field Effect Transistors (FinFETs) are equal. The Fin Type Field Effect Transistor (FinFET) technology offers various advantages over deep submicron transistors. The development of this technology has led to improvements in the intelligence and dependability of all electrical devices. It is possible that this experiment will result in an increase in the average power, energy, and power dissipation.*

Keywords: FinFET, CNTFET, Ternary Adder, HSPICE

1. Introduction

These breakdown points may be minimised by employing a single carbon nanotube that is put in an otherwise typical bulk MOSFET structure, and further reductions in device measurements are being promoted. This is because the utilisation of bulk MOSFETs is becoming increasingly popular. Now is the time for professionals in the disciplines of electronic device design, circuit design, and innovation to concentrate their attention on the future of the semiconductor industry in order to enhance the implementation of the electronic framework. In order to enhance bearer flexibility, a large amount of research and development is being devoted into the fabrication of high-portability transistor channel materials. Some examples of these materials include II-VI semiconductors. Investigations studying the probable benefits of employing nonplanar transistor architectures, such as CNTFETs and multi-gate designs, are still under work at present moment. Research is being undertaken on a variety of novel one-dimensional structures, including carbon nanotubes (CNTs) and other similar structures. Because of its high transporter mobility, carbon nanotubes (CNTs) have emerged as a viable competitor to boost the Si innovation plan in the post-2015 time frame; however, several difficulties still need to be overcome before this can happen. According to the results of the study, next-generation field-effect transistors, also known as CNTFETs, make it feasible to conduct research at both the device and the circuit levels. It will be impossible to make any further progress in silicon-based technology by the year 2020, when the channel length of a MOSFET will have been shrunk to less than 10 nanometre. Because of this, the semiconductor industry is continually on the lookout for cutting-edge discoveries in other materials and technologies that may complement or even replace the innovation that is today based on silicon. Carbon nanotubes (CNTs) have lately surfaced as a potentially helpful material among the many different layouts that have been researched. These architectures include single-electron burrows (SET), quantum cell automata (QCA), rapid single-transition quantum reasoning, and CNTs. In diameter, they generally range from 1 to 3 nm, however they may be many microns long. Their length, though, may be several times that. Carbon nanotubes (CNTs) have the potential to be utilised in the development of a broad range of useful gadgets. Some examples of these devices include low-cost high-quality connections, adaptive Carbon nanotube field-effect transistors (CNTFETs), and single electron penetrating transistors. In mechanical labs and universities (IBM, Intel, Infineon,) as well as educational institutions (schools), various research groups from all over the globe are finally researching CNTFET devices and their practical applications. These organisation may be located all throughout the world (Purdue, Stanford) (Purdue, Stanford,). Utilizing complementary. Although it may be challenging to discover accessible device models that are also suited to particular structure streams, having such models is crucial for the construction of circuits that rely on certain devices. This paper gives a full examination of the vast variety of CNTFETs that are presently accessible as well as various types that have been optimised. We applied publicly available models that were uncomplicated to recreate in order to examine the effect of the parameters on the properties of the device, which enabled us to acquire more accurate findings. Therefore, the CNTFET's current dimension and edge voltage are both influenced by the cylinder width. However, the CNTFET's current dimension is the sole characteristic that is impacted by the contact resistance.

In order to create trustworthy circuits and networks, a circuit planner needs to be able to take into account various aspects at different points in the circuit or network. In this case, the factors being taken into consideration are the lengths of the nanotubes.

In 1989, a "completely double gate FET" was produced, which the designers at the time described to as a "doubled gate SOI framework." This structure contained two sets of gates instead of simply one. This was the very first time that a structure comparable to a Fin Type Field Effect Transistor (FinFET) was shown in its earliest form. This was a historical first. A decline in the short-channel conductivity of planar MOSFETs has been documented throughout the course of the previous 10 years. As a consequence, there has been a surge in interest in fin type field effect transistors (FinFETs) across the same time period. The short-channel performance of Fin Type Field Effect Transistors (FinFETs), as is evident in Figure 1, is better to that of planar MOSFETs, which have the same channel length. Figure 1 displays the conventional configuration of a planar Fin Kind Field Effect Transistor (FinFET), which is a kind of field effect transistor.

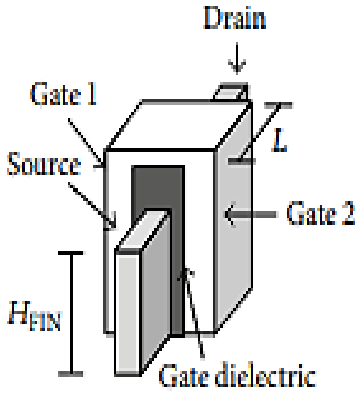

Fig. 1. FinFET Structure

2. Implementation

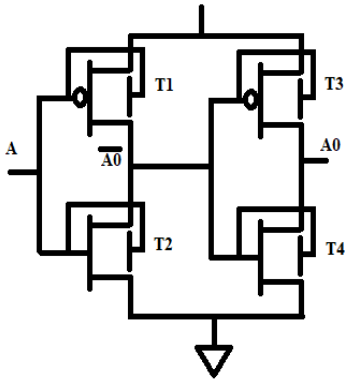

Fig. 2. Ternary Decoder Fin based

The following illustration demonstrates a decoder circuit that is constructed using Fin Type Field Effect Transistors, also known as FinFETs. The input to the decoder circuit is shown by the letter A, while the output of the circuit is indicated by the letter A0. This circuit is responsible for producing the A0 and A0 bars.

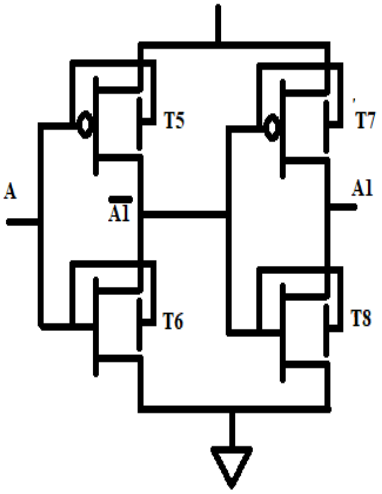

Fig. 3. Ternary Decoder for A

The decoder circuit shown in Fig. 3 is the same one that was shown in Fig. 2, with the exception that in this instance, we are using this circuit to create A1 and A1bar signals rather than only A1 signal.

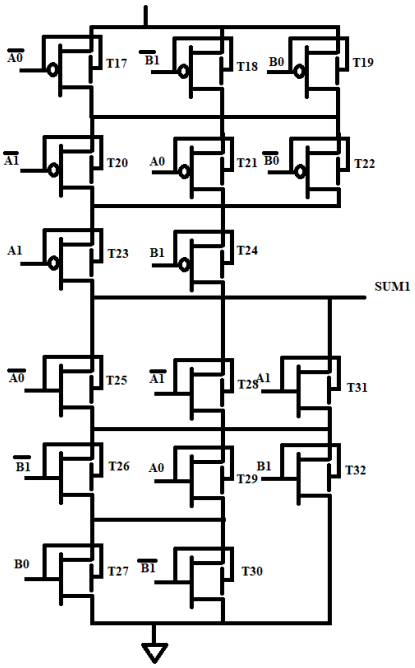

Fig. 4. SUM1 circuit

The circuit for a sum generator is shown in the image that can be seen above; the sum1 algorithm is being used to carry out the implementation, and the output of the circuit is binary.

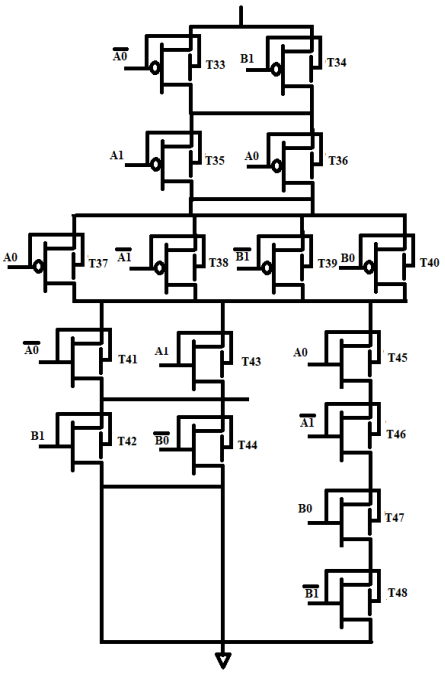

Fig. 5. SUM2 circuit

Figure 5 depicts the sum generator; in this particular instance, we are working on sum2, and the output that we are receiving is binary.

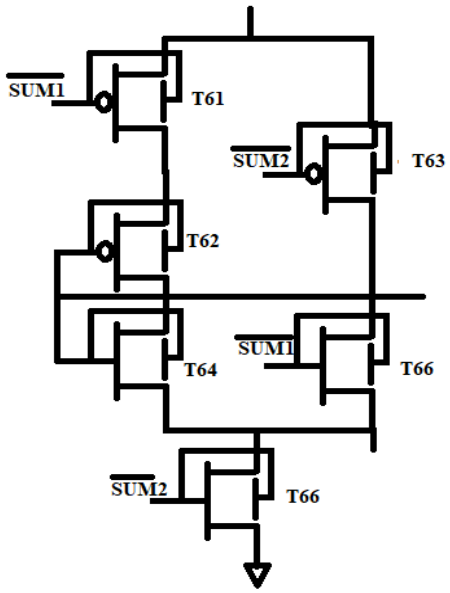

Fig. 6. Sum Output

The circuit for a sum generator encoder can be seen in Figure 6; the output of the encoder is the addition of sum1 and sum2; this adds up to the final ternary output.

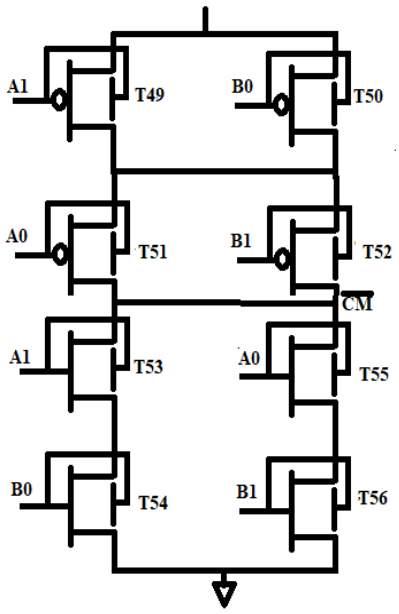

Fig. 7. Carry initial circuit

The circuit for the carry generator Cm is shown in Figure 7. This circuit makes use of the p channel Fin Type Field Effect Transistor (FinFET) as well as the n channel Fin Type Field Effect Transistor (FinFET).

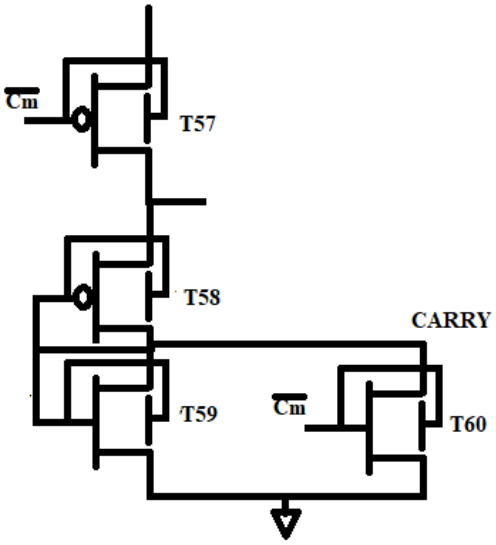

Fig. 8. Carry final circuit

The carry generating circuit is shown in the figure that came before it (Fig. 8); the carry is computed by using the carry encoder circuit (also seen in Fig. 8) and deriving it from Cm.

3. Results

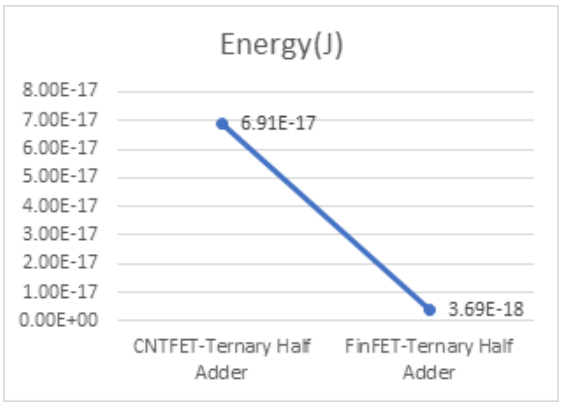

Fig. 9. Energy Result

Figure 9 illustrates the energy that would be produced by the proposed technology. When compared to the ternary adder Fin Type Field Effect Transistor (FinFET), the ternary adder CNTFET has an energy level that is much greater than the energy level of the ternary adder Fin Type Field Effect Transistor (FinFET).

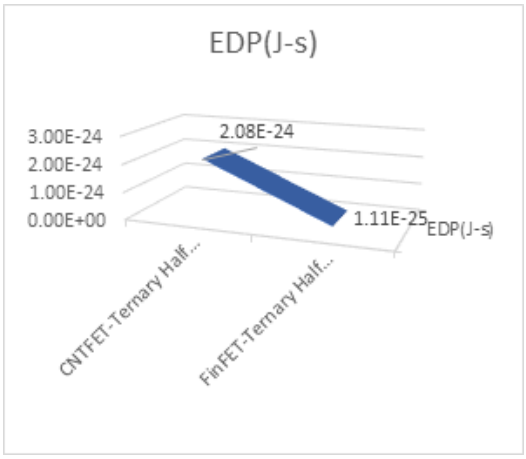

Fig. 10. EDP result

Fig. 10 illustrates the EDP of the system that has been proposed. In this particular example (Figure 10), the EDP in the ternary adder CNTFET is rather significant.

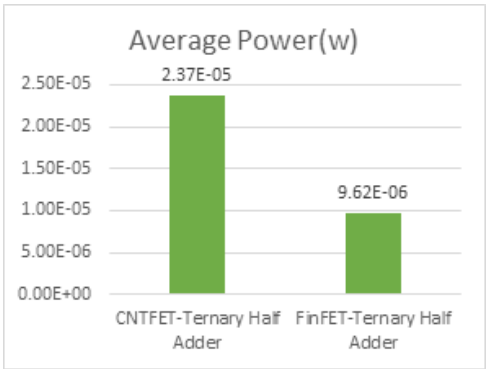

Fig. 11. Average Power results

The recommended system's average power, in addition to the average power, is greater in the ternary adder CNTFET than it is in the ternary adder Fin Type Field Effect Transistor (FinFET), respectively..

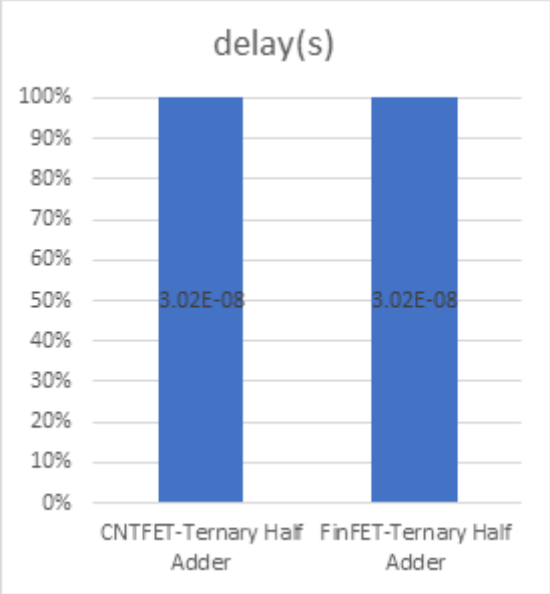

Fig. 12. Delay result

The above graphic demonstrates how long the proposed system will run behind schedule. The table that follows presents a comparison of the ternary adder CNTFET transistor and the ternary adder Fin Type Field Effect Transistor (FinFET) transistor's different parameters. Figure 13 presents the findings of the power dissipation test..

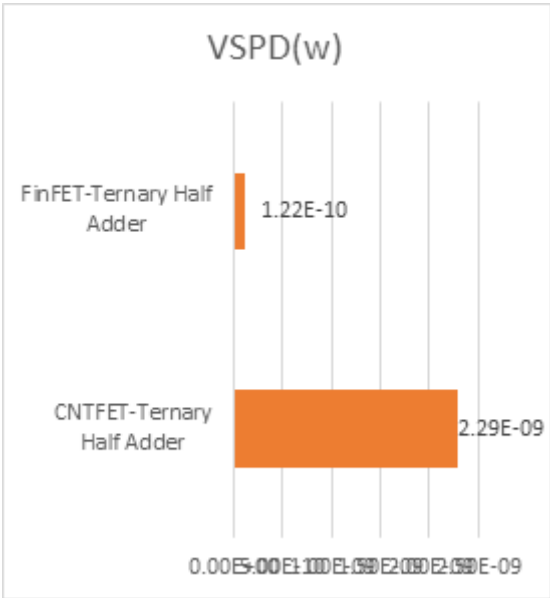

Fig. 13. Power dissipation result

Table 1. Output Results

PARAMETERS	CNTFET-Ternary Half Adder	Fin Type Field Effect Transistor (FinFET)-Ternary Half Adder
Average Power(w)	2.37E-05	9.62E-06
delay(s)	3.02E-08	3.02E-08
VSPD(w)	2.29E-09	1.22E-10
Energy(J)	6.91E-17	3.69E-18
EDP(J-s)	2.08E-24	1.11E-25

4. Conclusion

As a direct result of this, we have created a low-power ternary half-adder by the use of a technology that is known as Fin Type Field Effect Transistor (FinFET). We have used several different technologies, the most known of which is the Fin Type Field Effect Transistor (FinFET) technology. However, we have also utilised many other technologies. The use of the technology known as Fin Type Field Effect Transistor, or FinFET, is what is responsible for the rise in the power, latency, PDP, and leakage power of the ternary half-average adder. As can be seen from the data that was supplied, we are comparing the ternary adder CNTFET to the ternary adder Fin Type Field Effect Transistor (FinFET), and we are doing so by using two distinct circuits. This can be seen since the data was provided. HSPICE is used to do both the simulation of the circuits and their verification with the assistance of Avanwaves..

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