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Electrical Rule Check Verification Methodology For SoC

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Abstract - *Semiconductor industry has continued to make spectacular improvements in the achievable density of very large-scale integrated circuits. In a SoC design flow there are many phases of which verification of full chip SoC plays important role. Despite decades of work, SoC Analog Verification remains a highly expensive and time-consuming component of electronic system development. In today's designs, complex circuit issues such as, floating node and device domain where designs are low power so leakage current and reliability are at most priority . To verify these issues electrical rule checking methodology used to check the robustness of a design at both schematic and layout level against various electrical design rules. In full chip SoC different modules need to follow certain powerup sequence when chip gets powered ,failure in powerup sequence may results in chip starts malfunction or unreliable operation. Hence it is most important to make sure powerup sequence is as expected in product DOS. Powerup sequence analyses carried out using Finesim Powerup Simulation.*

Key Words: **Electrical Rule Check, Floating Node, Device Domain, Insight ERC Analyzer, Finesim.**

1. INTRODUCTION

SoC solutions offer significant benefits while also posing some challenges for designers. The advantages of using SoC solutions include reduced size, lower cost, lower power consumption, and increased performance. However beyond these advantages, design complexity is drastically increased because technological advancements let us integrate a lot of functions into a single chip. SoC designs have become one of the main drivers of the semiconductor technology in recent years .In SoC design flow as show in the figure 1, the design specification is created by a SoC integrator, then the integrator identifies a list of IPs to implement the given specification. These IP cores are either developed in-house or purchased from third party IP vendors [1]. Following the development/acquisition of all IPs, the SoC design house integrates them to generate the RTL description of the entire system. After that SoC integrator synthesizes the RTL description into a gate-level netlist, based on the logic cells and I/Os of a target technology library. The gate-level netlist is translated into a physical layout based on logic cells and I/O geometries. It is also possible to import IP cores from vendors in GDSII layout file format at this step [2].

Basically Electrical rule check (ERC) performed at different levels of analog verification of SoC, but one of them comes after Layout and STA phase. ERC is performed at full chip level to verify the design for primitives been placed in correct power domains and to avoid any functional or reliability issue. ERC is a methodology used to check the robustness of a design both at schematic and layout level against various electronic design rules. It is used to detect the electrical violations that can be missed in analog simulation and to find the circuit problems.

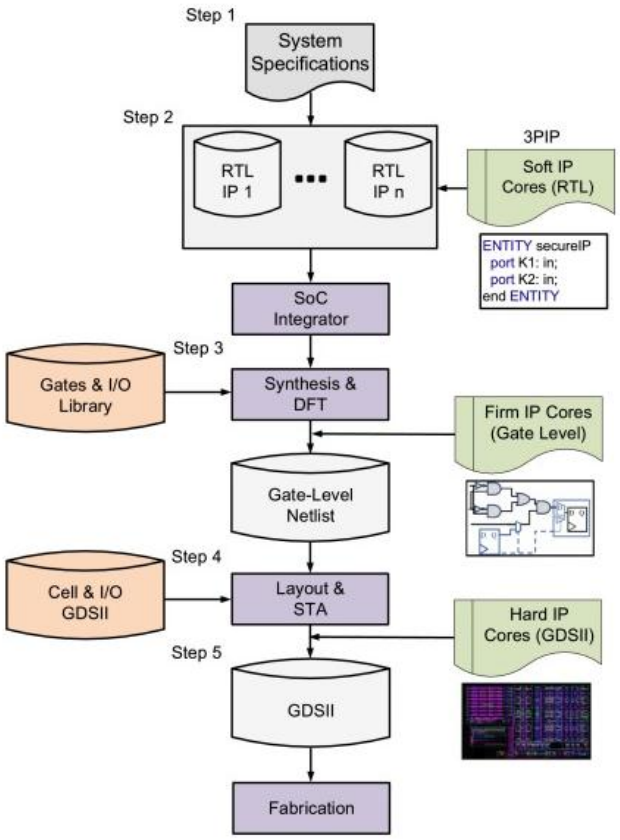

Fig -1: SoC Design Flow

ERC mainly includes two checks they are device domain/power connection and floating node. Now a day's designs are low power and smaller size , because of this complex circuit issues such as floating nodes where leakage current as major drawback of low power devices and power connection where reliability is at most priority, these require

verification techniques that can combine physical and electrical information to understand more complex connectivity and greater design context . Without such checks, designers cannot adequately verify the robustness of a schematic or layout design to ensure that circuits will operate as designed and intended, and that the circuitry is well-protected against potential electrical failures. Powerup sequence of full chip SoC also plays very important role in understanding how different modules of SoC get powered once power supplied to full chip. In full chip different modules need to follow certain powerup sequence when chip gets powered ,failure in powerup sequence may results in chip starts malfunction or unreliable operation .Powerup sequence simulation done using Finesim tool.

2. ERC METHODOLOGY

The main objective of the paper is to create setup additions to an ERC tool through TCL script and perform various checks for full chip level of SoC under device domain and floating node. These checks ensure that no leakage current and reliability issues in a SoC. Finesim powerup simulation is used to analyze powerup sequence of full chip. This simulation ensures all modules responding accurately once power is applied to full chip.

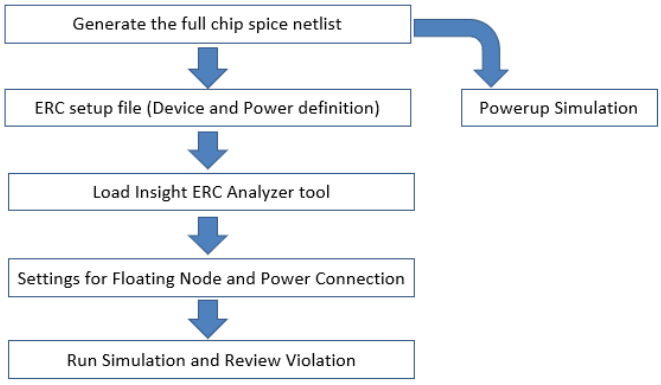

Fig -2: ERC Methodology

The ERC methodology involves mainly six steps as shown in the figure 2. Initially full chip spice netlist is generated by using V2S tool which takes one top level spice netlist and many other include spice/cdl files as input. Then ERC setup using TCL script which contains device domain parameters, power definitions and full chip spice netlist. After that load the Insight ERC Analyzer tool using TCL script. Then power connection and floating node issues having different types of violations based on the project ,setting up the parameters and violations. Once above steps followed run and review the violations .Finally powerup simulation is done by using Finesim tool to understand the powerup sequence of full chip .

2.1 Device Domain and Floating Node Analysis

Device domain/power connection and floating node analysis using ERC simulation with help of Insight ERC Analyzer tool as shown in the figure 3. Device domain is type of violation which creates reliability issues in the modern complex circuit . Verification of these type of violations are at most priority in today's low power devices .Basically there are different types of violations comes under device domain check. Here mentioned only two, firstly FET Vg Over Max means Vg of mosfet is beyond the limit which is undesirable. Secondly FET Vb Wrong means bulk on PMOS is not at or above source/drain which creates leakage current inside the mosfet.

Floating Node is type of violation which creates leakage current leads to serious issues in low power devices. Floating node violations mainly related to absence of pull up and pull-down circuits .There are different types of violations comes under floating node check. Here mentioned only two, firstly Float Constant means floating net on gates of powered mosfets. Secondly Float, Unsafe cell means Unsafe cell, could float if not properly used in circuit.

Fig -3: Insight ERC Analyzer

In this paper above issues are analyzed or examined using Insight ERC Analyzer where it is used to read a netlist and perform Static Electrical Rule Checking. Cadence Virtuoso and Starvisionpro are used to view violation at macro level and full chip level respectively. Finesim is used for powerup simulation to analyze the powerup sequence of full chip which is discussed in the next part.

3. POWERUP SEQUENCE

Power system block controls or manages power supply to the entire full chip. This module mainly contains five sub modules they are analog macros, backup voltage regulator, 1.2-volt core logic unit, internal regulator and finally IO logic. SMOR is one of main modules in analog macro which takes major role powerup sequence. The Supply Monitor Overseer Supervisor (SMOR) , which consists of Power on reset (POR), Bandgap voltage reference (BGR) , Constant Current Reference, PTAT Current Reference, Brown-out and Reset (BOR).This module (SMOR) acts as voltage and current supplier to other analog macros. It works in conjunction with start-up logic (SUL) and

Reset power Management Unit (RPMU) to provide reference and reset to entire system under various power modes. A block level representation of the whole system is given in Figure 4.

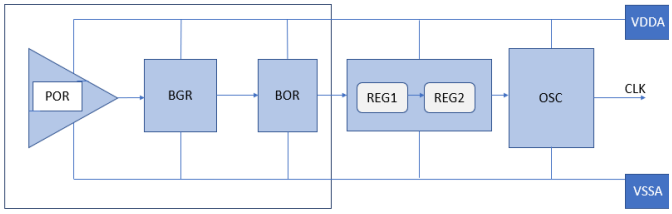

Fig -4: SMOR System

The power sequence is the order in which power is applied and shut down, as well as the time intervals between steps in the sequence. When there are semiconductor devices with different power supply voltages mixed on one board, or when multiple equipment is connected, a power sequence is used. Power sequencing is an essential component of any design, particularly in complex systems with multiple power rails. For example FPGAs, ASICs, PLDs, DSPs, and microcontrollers, require multiple voltage rails to power internal circuitry such as the core, memory, and I/O. These applications necessitate very specific voltage rail power-up and power-down sequencing and supervision to achieve dependable operation, improved efficiency, and overall system health.

4. SIMULATION RESULTS

Following figures are from ERC simulation and Finesim powerup simulations respectively. FET vg over max is one of the violations of Device Domain/Power Connection, where Vg is beyond limits of device .Basically every device or mosfet having some threshold voltage above which break done may happen this leads to reliability issues. From above figure 5. mosfet (MN0) which is 2.5-volt device but gate terminal getting 3.3 volt from the VDDIO RING supply but it's not real violation because 2.5-volt device having thick oxide gate may withstand till 3.3 volt.

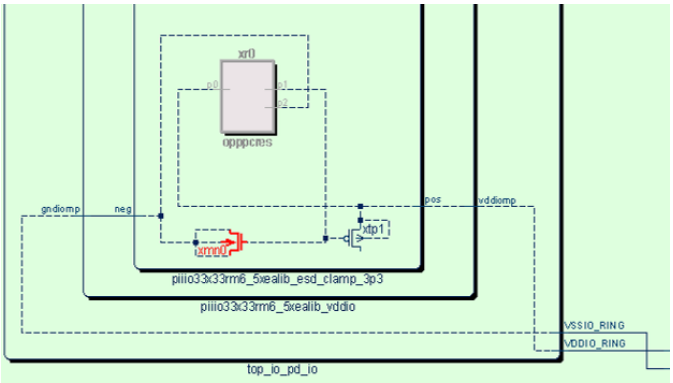

Fig -5: Power Connection Violation

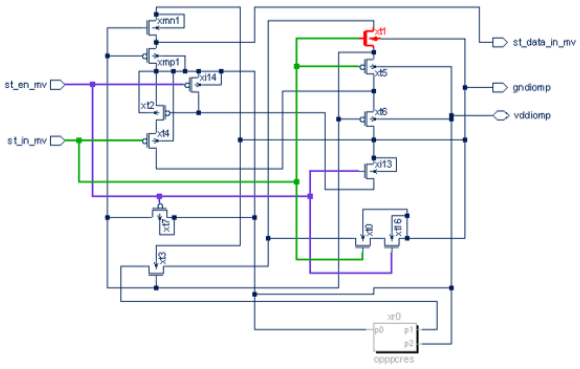

Fig -6: Floating Node Violation

Float Constant (sensitive pins on signal) is one of the violations of floating node where mosfet sensing floating net (unknow voltage net). Basically floating nodes lead to leakage current it's one of the major issues in low power devices. From the figure 6 ,mosfet (T1) having (st_in_mv) signal as gate input and it's floating . T1 mosfet having proper pull up and pull down controlled by (st_en_mv) signal verified using starvisionpro tool. then it's not real Initially power applied to full chip ,once supply reaches the voltage (VTMIN), which is sufficient for a medium voltage digital logic to operate, the POR circuits automatically turn itself ON and starts to monitor the supply voltage with a valid output signal (por _n_mv). Below VTMIN the output of the POR is not valid thus should be ignored. Once valid output signal (por_n_mv) is high leads to release of POR reset automatically enables the bandgap reference sub-module .This block generates either 1.2 volt or 0.8 volt based on the application. After that ready signal comes if and only if output of bandgap reference is stable. Brown Out Reset (BOR) sub-module is enabled due to release of POR reset, and assertion of bandgap reference stable signal automatically enables the BOR circuit. BOR circuits helps if supply voltage falls below some threshold and then generates enable signal which is used as input for next stage.

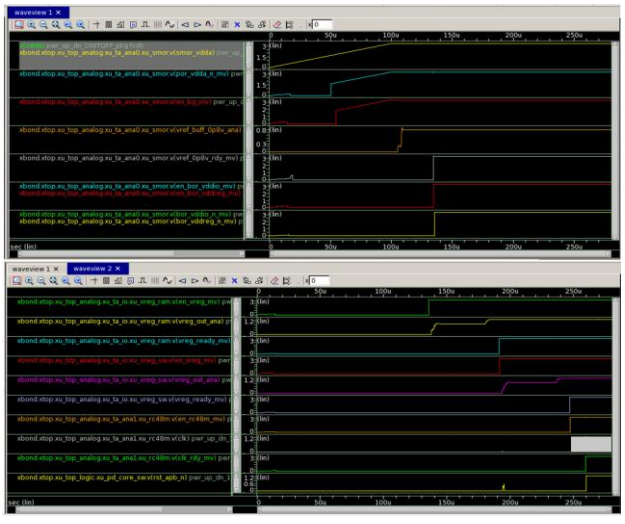

Fig -7: Powerup Sequence of Full Chip

Powerup Sequence of Full Chip Internal regulator one (REG1) generates stable 1.2 volt when BOR is out of reset .Once REG1 output is stable which is given as enable signal for REG2.It also generates 1.2 volt for core logic units. REG2 output is given to oscillator input which generates clock of frequency 48 MHz . Once clock is stable entire system comes out of reset. These steps followed in powerup simulation as shown in the figure 7. So every module in the SMOR flowing the powerup sequence analyzed form the Finesim powerup simulation.

5. CONCLUSION

The device domain/power connection and floating node analysis done using Insight ERC Analyzer .These violations are reviewed with help of analog concept and sometime using simulation of that circuit in cadence virtuoso. Starvisionpro very much help in debugging floating node violations as well as power connection violations at full chip level whereas at macro level cadence virtuoso is best practice .All violations reviewed successfully without any roadblock. Finally powerup simulation using finesim tool to analyze powerup sequence at full chip level of SoC.

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