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DESIGN OF LOW POWER MULTIPLIER

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Abstract - *The novel 32x32 multiplier design using Booth architecture and Vedic architecture is presented in this project. The Booth multiplier, which is the foundation of the Booth architecture, cuts the number of partial products generated in half. Vedic architecture benefits from simultaneous partial product production and adding. The 16x16 Vedic architecture is used to divide the 32x32 multiplicand and multiplier in order to increase the performance of the multiplication. In addition to Vedic design, this new 32x32 signed multiplier also has more benefits than the individual Booth multiplier and Vedic multiplier technique. Compared to a standard 16x16 Booth multiplier, it has a straightforward architecture. This new multiplier makes use of the Carry Select Adder and the Ripple Carry Adder (RCA). CSA to add the product that was partially generated. The performance has increased thanks to the new 32x32 signed multiplier's shorter overall propagation delay. The modern 32x32 multiplier design is more optimized compared to individual ones. This is due to the concurrent usage of Vedic architecture for both the partial product addition and the partial product production by the Booth multiplier. The proposed multiplier is designed using Xilinx ISE and Xilinx Vivado.*

Key Words: **BOOTH MULTIPLIER, VEDIC MULTIPLIER, POWER, DELAY, XILINX ISE, XILINX VIVADO.**

1. INTRODUCTION

Due to the rapid advancement of technology, demand for quick and effective processor units has surged as a result of digital signal processing (DSP). A processor's performance is primarily dependent on the multiplier's performance. High speed, small size, and low power consumption multipliers are increasingly priorities for high performance processors. The design of the multiplier for Very Large-Scale Integration (VLSI) architecture faces a critical issue posed by these three key trade-off parameters.

The new 32x32 combined Booth and Vedic multiplier is implemented using the Booth multiplier architecture and the Vedic multiplier architecture to enhance the performance of multiplication. The number of partial products is almost cut in half by the Booth multiplier, and the signed input is divided for quick multiplication in the Vedic architecture.

Additionally, the partial product addition is crucial in enhancing a multiplier's efficiency.

1.1 PROBLEM STATEMENT

Very large-scale integration (VLSI) circuits with low power consumption are essential for creating small devices with high performance and energy efficient design. The multiplier is crucial in the design of an energy-efficient CPU since it determines the processor's power. Creating a multiplier that operates more quickly and with less power consumption than earlier multiplier models.

2. WORKING

The 16x16 Booth multiplier and 16x16 Vedic multipliers are combined to create a new efficient 32x32 multiplier. Carry select adder and Ripple carry adders are used in this design. The energy efficient proposed multiplier is used in Floating-point multiplier which is an important application.

2.1 Booth multiplier

One such multiplier that scans the three bits at a time is the Booth multiplier, which lowers the number of partial products. Booth encoding conducts numerous multiplication steps simultaneously to speed up the multiplication process.

The fact that an adder subtractor is almost as quick and compact as a basic adder is exploited by Booth's algorithm. Addition and subtraction operations can be skipped if three consecutive bits are the same. As a result, in the majority of instances, Booth Multiplication's related delay is less than that of an Array Multiplier.

By inspecting three bits at once, the Booth multiplier approach decreases the number of adders and, thus, the time needed to produce the partial sums. The booth multiplier's excellent performance has the drawback of being power-hungry. The need for a high number of adder cells, which use a lot of power, is the cause.

16x16 Booth multiplier is used in this design with 16x16 Vedic multiplier.

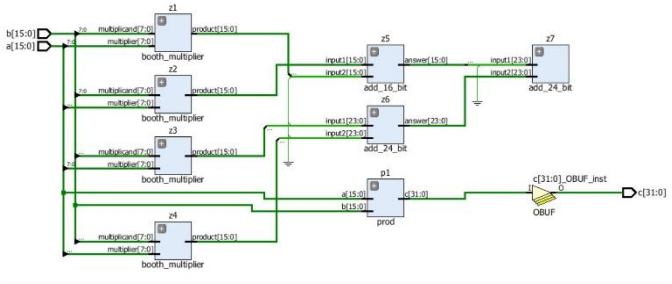

Fig -1: 16X16 BOOTH MULTIPLIER

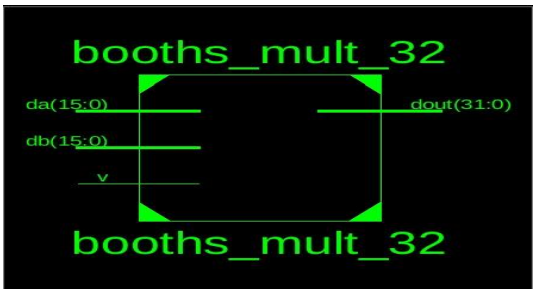

Fig -2: 16X16 BOOTH MULTIPLIERSCHEMATIC

Total Delay = 10.288ns

2.2 Vedic multiplier

Vedic mathematics is used because it simplifies complex computations that are typically seen in traditional mathematics. This is true because it is said that the Vedic equations are founded on the same basic laws that govern how the human mind functions. Based on the Vedic multiplication formulas(sutra), the Vedic multiplier is designed. The multiplication of two numbers has always been done using this sutra. We will use the same principles in the proposed work to make it compatible with the digital hardware.

A universal multiplication formula that works in all situations is the Urdhva Tiryakbhyam Sutra. "Vertically and Crosswise" is what it signifies. The two ends of the line's digits are multiplied, and the resulting sum is added to the carry from before. All outcomes are added to the previous carry when there are more lines in a step. The resultant number's least significant digit serves as one of the result digits, with the remaining digits serving as the carry for the following step. The carry is first assumed to be zero.

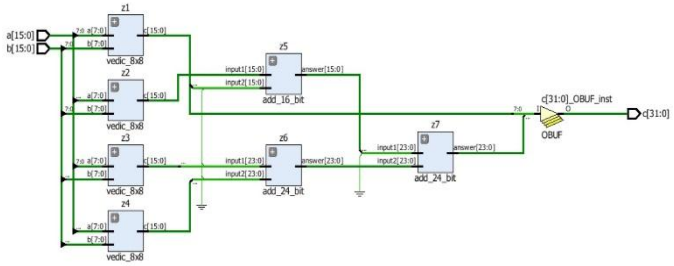

Fig -3: 16X16 VEDIC MULTIPLIER

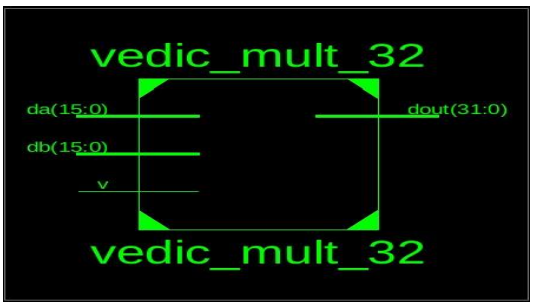

Fig -4: 16X16 VEDIC MULTIPLIER SCHEMATIC

2.3 PROPOSED MULTIPLIER

The new design is designed by combining the Booth architecture and Vedic architecture. The new architecture partition each of the signed value into two block and multiply using Vedic algorithm.

The new design uses two 32-bit booth multiplier and two 32-bit Vedic multiplier. 16x16 Booth multiplier is used to multiply the signed value in each block. Figure shows the first design of 32x32 Combined Booth-Vedic multiplier architecture.

This design uses the CSA to add up the generated partial products. The 32x32 Combined Booth-Vedic multiplier is designed by using four 16x 16 multipliers and two 32 bits CSA and one 64bit CSA. here are four difference condition for the signed multiplication using Vedic architecture. This is the important section to make sure the multiplication is correct.

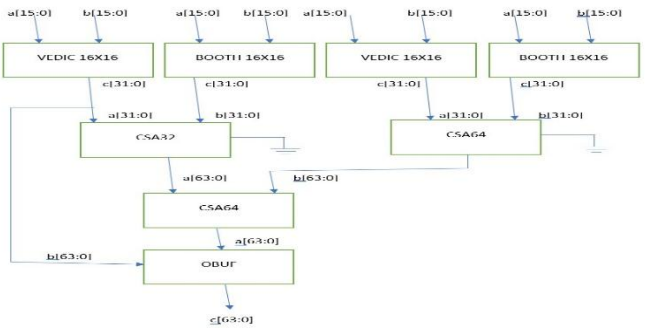

Fig -5: 32X32 COMBINED MULTIPLIER BLOCK DIAGRAM

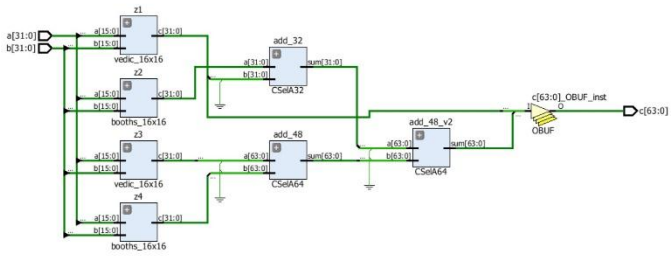

Fig -6: 32X32 COMBINED MULTIPLIER DESIGN

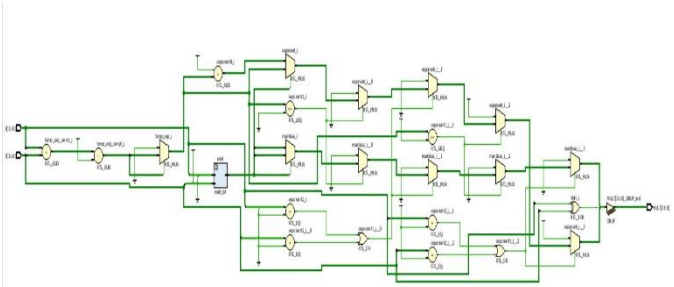

Fig -7: FLOATING-POINT MULTIPLIER DESIGN

3. ADVANTAGES AND APPLICATIONS

ADVANTAGES

- Power usage: When computing large and small numbers, the multiplier's architecture requires less power.
- Workflow speed: A multiplier that is meant to compute large and small numbers more quickly.
- The multiplier has a longer lifespan.
- Cost of operation is reduced. This yields to more production.

APPLICATIONS

FLOATING-POINT MULTIPLIER

A floating-point technique is an additional or different method of describing the number. Computer words (actual numbers on computers) are displayed in real time using the IEEE 754 floating-point format. These days, modern computers represent integers in this manner. This method can be applied to every type of number, including huge, very large, tiny, and extremely small numbers. This technique offers representation for an infinitely large range of numbers. Both signed and unsigned numbers are represented using this format. The accuracy and precision with which the numbers are expressed in this example are very high. This approach represents the number using the scientific method.

In recent years, floating point conversion has been used by all contemporary computers, laptops, computer graphics, modelling systems, DSP chips, and so forth.

The proposed multiplier is used in the floating-point multiplier.

OTHER APPLICAIONS

- FIR filters
- IIR filters
- Fixpoint multiplier
- DCT, DFT, cosine transform etc.
- In image processing applications
- In fast Fourier transforms
- In ALU of microprocessor

4. SOFTWARE REQUIREMENT

Xilinx Vivado Design Suite

The Xilinx software Vivado Design Suite replaces Xilinx ISE with new functionality for system on a chip development and high-level synthesis. It is used for the synthesis and analysis of hardware description language (HDL) designs. The design flow has been completely rewritten and rethought using Vivado (compared to ISE).

Similar to later iterations of ISE, Vivado has an integrated logic simulator. High-level synthesis is another innovation made by Vivado. It uses a toolchain to transform C code into programmable logic.

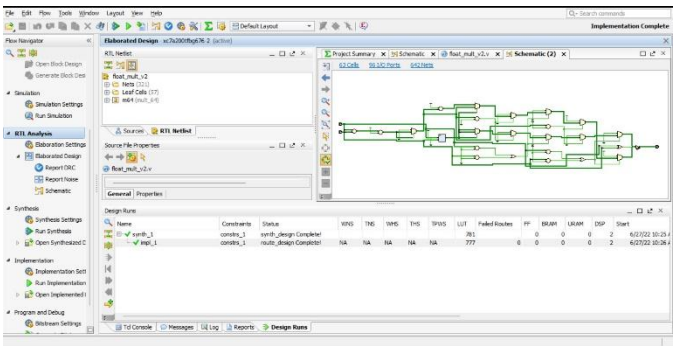

Fig -8: XILINX VIVADO SOFTWARE WORK AREA

XILINX ISE

For the synthesis and analysis of HDL designs, Xilinx ISE (Integrated Synthesis Environment) is a discontinued software tool from the company. It was primarily used to generate embedded firmware for the FPGA and CPLD integrated circuit (IC) product lines from Xilinx. Xilinx Vivado succeeded it in the market. For in-system programming of legacy hardware designs comprising older FPGAs and CPLDs that would otherwise be left orphaned by the replacement design tool, Vivado Design Suite, the most recent edition from October 2013 is still in use. ISE gives developers the ability to synthesize (or "compile") their designs, run timing analyses, go at RTL diagrams, simulate a design's response to various stimuli, and work with the programmer to set up the target device. The Software Development Kit (SDK), the Embedded Development Kit (EDK), and other items are also included with the Xilinx ISE (SDK).

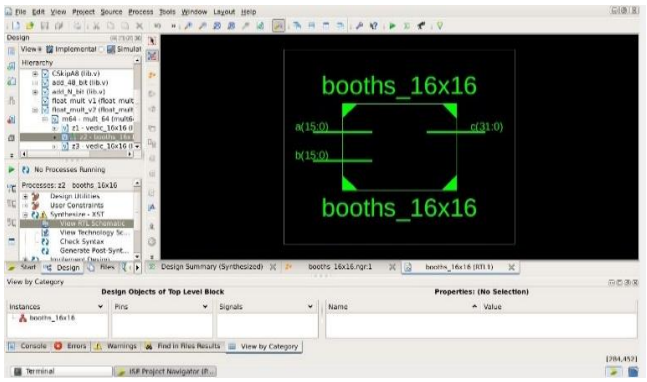

Fig -8: XILINX ISE SOFTWARE WORK AREA

5. RESULTS AND OUTPUT ANALYSIS

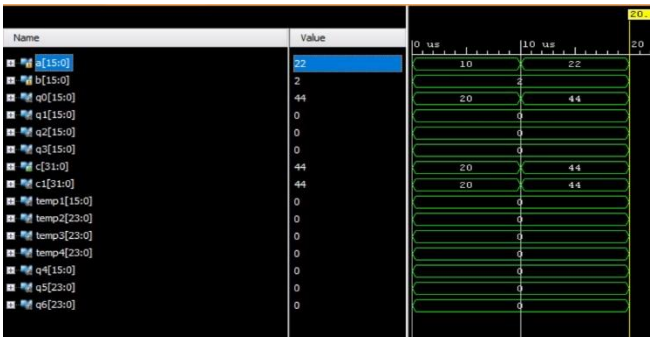

Fig -9: 16X16 BOOTH MULTIPLIER OUTPUT

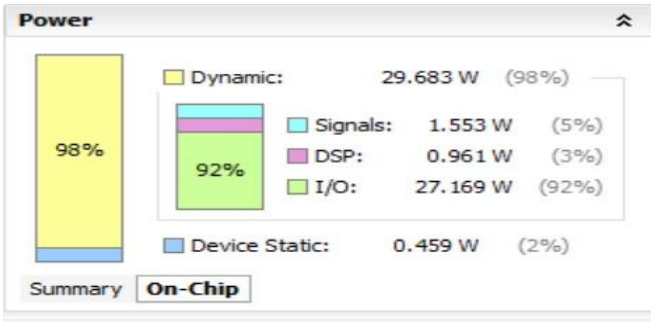

Fig -10: 16X16 BOOTH MULTIPLIER POWER ANALYSIS

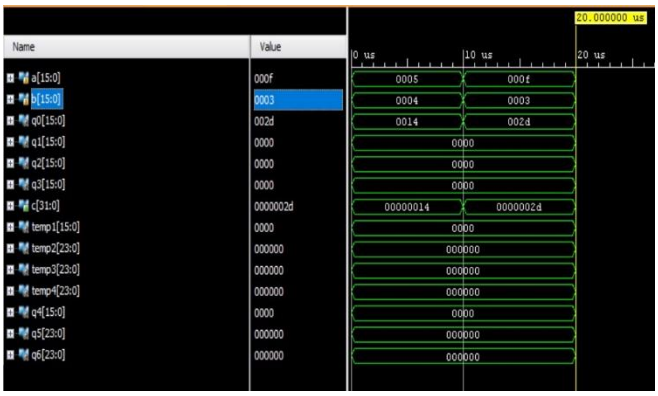

Fig -11: 16X16 VEDIC MULTIPLIER OUTPUT

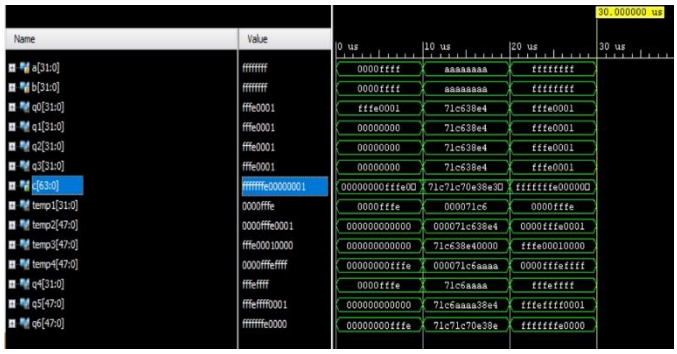

Fig -12: 16X16 VEDIC MULTIPLIER POWER ANALYSIS

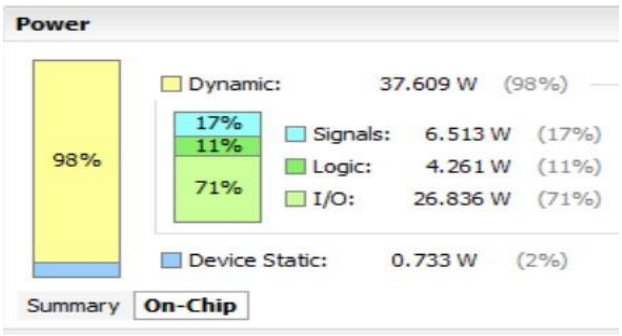

Fig -13: 32X32 COMBINED MULTIPLIER OUTPUT

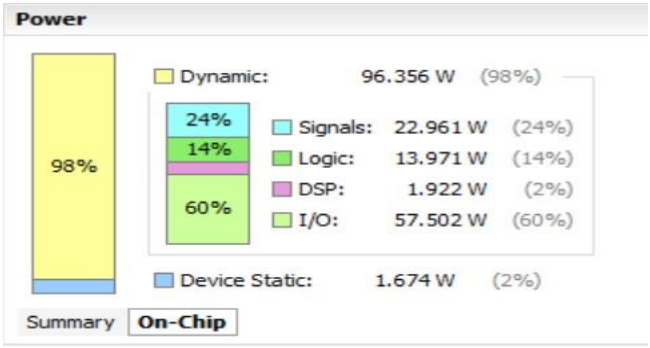

Fig -14: 32X32 COMBINED MULTIPLIER POWER ANALYSIS

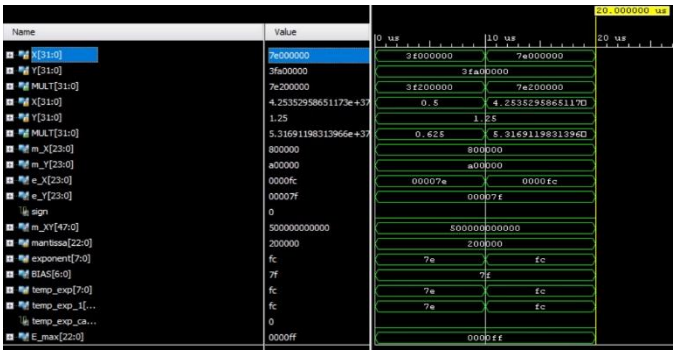

Fig -15: FLOATING-POINT MULTIPLIER OUTPUT

5. CONCLUSION AND FUTURE SCOPE

CONCLUSION

Using Xilinx Vivado and Xilinx ISE software, Booth-Vedic multipliers have been conceived, designed, simulated, and tested for functionality in the 32x32 multiplier. Two 16x16 multipliers were created, and their power usage and processing times were compared to those of a 32x32 combined multiplier. These were created in Xilinx Vivado utilizing carry select adders and ripple carry adders. The simulations are carried out using Xilinx and Vivado Tools, and the schematics are created using Xilinx and Vivado. It is taken the time summary (Speed) and power summary. The 32x32 combined multiplier uses less energy and operates more quickly. The latency and energy usage barely increase as the number of bits rises.

FUTURE SCOPE

Energy-efficient design is crucial in daily life, and as the number of bits increases, multiplication of numbers will become more and more efficient. With the addition of enhanced methodologies, the proposed multiplier's power and speed are further decreased and raised, respectively.

To make things or programs easier to integrate into systems, everyone wants them to be lighter these days. As a result, new ways will be implemented in the future to make the developed design considerably smaller. This will be useful for situations requiring less weight. In a key working condition, the lifespan of the multiplier is very significant, thus in the future, the required approaches will be incorporated into this project and the lifetime of the generated multiplier will be further improved.

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