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DESIGN OF 8-BIT COMPARATORS

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Abstract - *The purpose of this paper is to study different types of comparators as they are used in many electronic circuits to find the threshold levels of voltages or currents. The comparators output will give highest and lowest numbers among the applied inputs. The proposed comparators here use the subtractor as we easily say whether the value is greater or lesser based on the borrow generated. The software used to design these comparators is Xilinx Vivado. The results of various comparators designed are compared in terms of their power, number. of cells etc., The purpose of this paper is to study different types of comparators as they are used in many electronic circuits to find the threshold levels of voltages or currents. The comparators output will give highest and lowest numbers among the applied inputs. The proposed comparators here use the subtractor as we easily say whether the value is greater or lesser based on the borrow generated. The software used to design these comparators is Xilinx Vivado. The results of various comparators designed are compared in terms of their power, number. of cells etc.,*

Key Words: **PE - Processing Element; CBDC - Conventional Bit-wise Data Comparator; Design of Borrow Look Ahead Data Comparator (BLAC); Design of Mux Based Data Comparator (MDC).**

1. INTRODUCTION

The comparators are the devices that are used in the electronic circuits to find the threshold levels to give an input and also to compare the results of output with some predefined value to check whether the output is at expected level or not. The basic comparator is a conventional bit-wise comparator that compare the bits and gives the result as one of the numbers is greater or less or equal to the other. The comparators uses subtractor as one of the processing element. Mux is also used in this comparator design to give the outputs depending on the borrow from the subtractor. In this paper we have designed different types of data comparators that are used in various circuitry like Null-Detector, Zero-Crossing Detector, Relaxation Oscillator, Level Shifter, Analog to Digital Converters, Window Detectors, BLDC Operating Motors, Switching Power Regulators and also in Peak Detectors.

They are mainly

1.Conventional Bit-wise Comparator.

2.Borrow Look Ahead Comparator.

3.Mux-Based data Comparator.

2. COMPARATOR DESIGN

The design of comparators involves the designing of processing elements used in it and mux interface at the output of these cascaded processing elements. The design of comparators is shown below.

2.1.DESIGN OF CONVENTIONAL BIT-WISE COMPARATOR

This traditional data Comparator employs the operation similarly to a word Comparator. As a processing element, a 1-bit magnitude comparator is used. To implement 8-bit comparator, 8 processing elements of 1 bit comparator are considered. All the 3 possible ways are a>b, a<b, and a=b represented as the outputs.

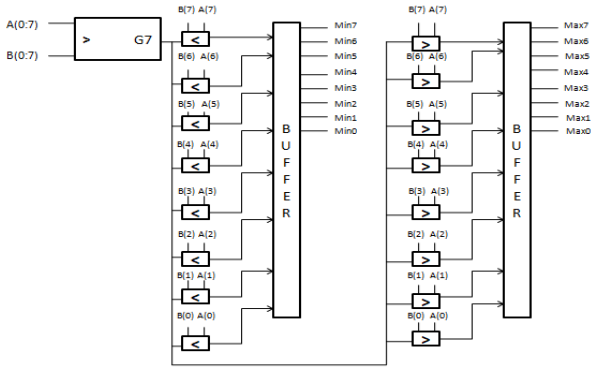

Fig 2.1 Schematic of the Conventional Bit-Wise Comparator

The operation of the comparator is shown by a tabular model to understand it's working in a easy way. When the inputs meet the condition then the values in the table are highlighted.

Table -1: Output of conventional Bit-wise comparator

A	B	A<B	A>B	A=B
00000101(5)	00000011(3)	0	1	0
00000011(3)	00000101(5)	1	0	0
00000101(5)	00000101(5)	0	0	1

2.2. DESIGN OF BORROW LOOK AHEAD COMPARATOR (BLAC)

Borrow look ahead logic data comparator eliminates the borrow dependency problem. An 8-bit comparator that generates a carry that is independent of the preceding stage using Borrow Look Ahead Select Logic (BLAC) instead of logic circuits, as seen in the equations below. The higher and lower value of two numbers will be found using this carry. The borrow look ahead select logic structure is mostly used to eliminate carry dependencies that occur during the preceding steps.

Consider the basic borrow equation of a complete subtractor in equations to understand how BLAC works. Let' s say x and y are the two 8-bit inputs, and Ci stands for initial carry (which is the first bit).

Co = ((not x) and y) or ((not x) and C_I) or (y and C_I)

Gi = (not x_I) and y_I

Pi = x_I xor y_I

C(i+1) = G_I + (not P_I) C_I

i = 0 C0 = G0

i = 1 C1 = G1 + P1G0

i = 2 C2 = G2 + P2G1 + P2P1G0

i = 3 C3 = G3 + P3G2 + P3P2G1 + P3P2P1G0

I=4 C4 = G4 + P4G3 + P4P3G2 + P4P3P2G+ P4P3P2P1G0

i=5 C5 = G5 + P5G4 + P5P4G3 + P5P4P3G2 +P5P4P3P2G1 + P5P4P3P2P1G0

i=6 C6 = G6 + P6G5 + P6P5G4 + P6P5P4G3+ P6P5P4P3G2 + P6P5P4P3P2G1 + P5P4P3P2P1G0

i = 7 C7 = G7 + P7G6 + P7P6G5 + P7P6P5G4+ P7P6P5P4G3 + P7P6P5P4P3G2 + P7P6P5P4P3P2G1 + P7P6P5P4P3P2P1G0

By using the above equations, a borrow look ahead logic is generated and it will perform the comparison operation.

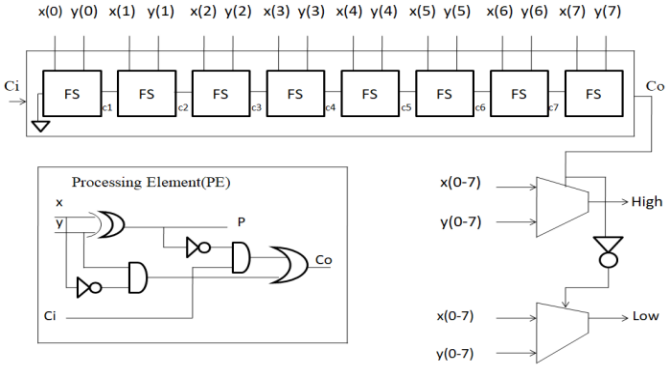

Fig 2.2 Schematic of the Borrow look ahead data comparator

2.3 DESIGN OF MUX BASED COMPARATOR

In this comparator the elements OR gate, AND gate, and Multiplexer make up the Processing Element (PE). The care should be taken about the borrow because it determines the operation of comparison. The data comparator requires a borrow generation circuit. The processing element has been constructed.

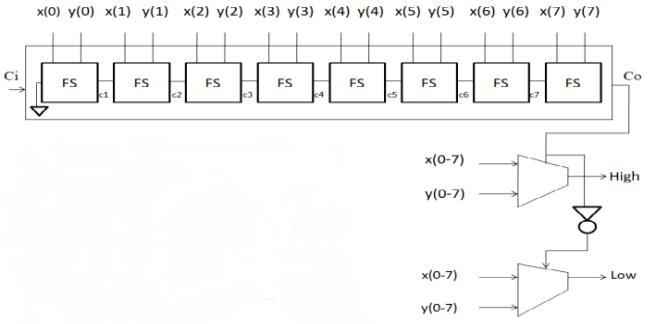

Fig 2.3 Schematic of the Mux Based data comparator

Any one of the inputs will operate as a selection line in the comparator, and the data will be formed by the other two inputs. In the selection line, a zero will select the outcome of two inputs "OR" operation a one will select the outcome of two inputs "AND" operation. Based on the selection line (third input) the borrow is chosen. The comparator uses the parallel pipe-lined architecture which makes it consumes lesser number of steps and power. The comparator operation can be implemented as a subtractor and the borrow generation is facilitated using this multiplexer - based approach.

3. SIMULATION RESULTS

The stimulation results of the designed comparators are discussed in this section along with the comparisons of power and area of consumption among them.

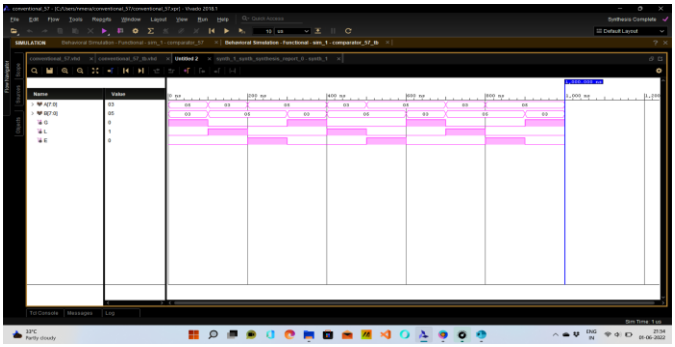

Fig 3.1 Output of Conventional type comparator

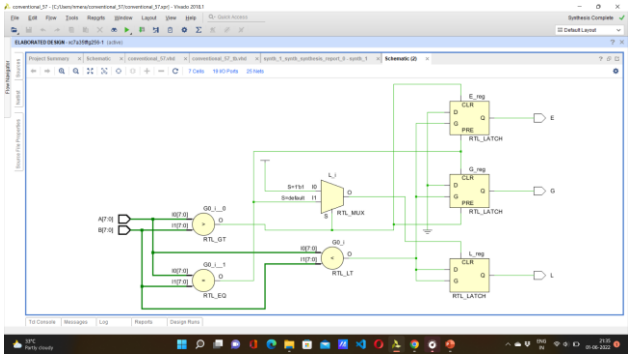

Fig 3.2 RTL Schematic of conventional type comparator

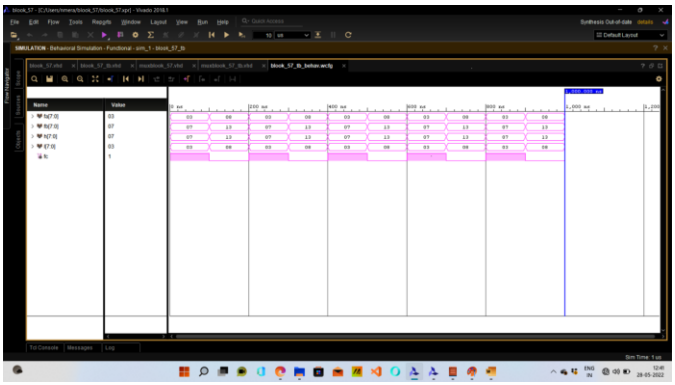

Fig 3.3 Output of Borrow look ahead data comparator

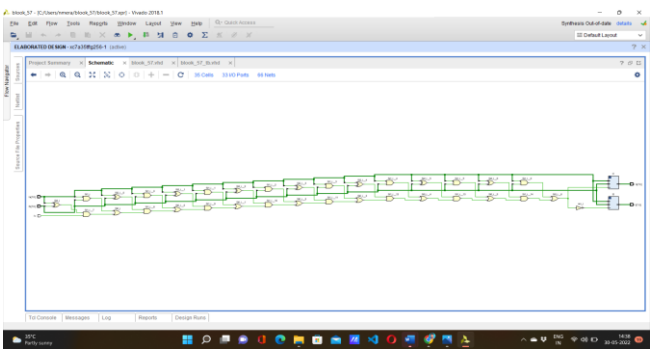

Fig 3.4 RTL output Schematic of Borrow look ahead data comparator

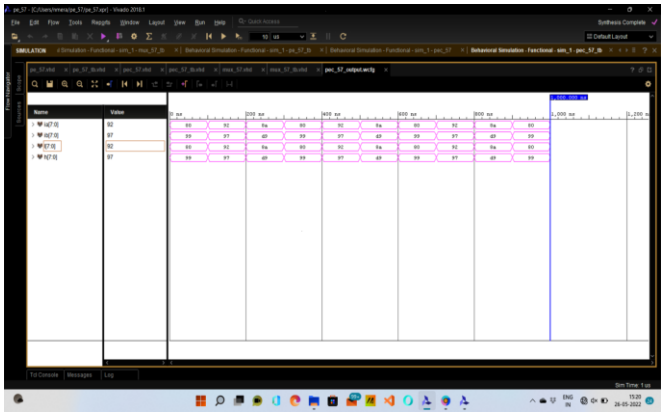

Fig 3.5 Schematic of Mux based comparator

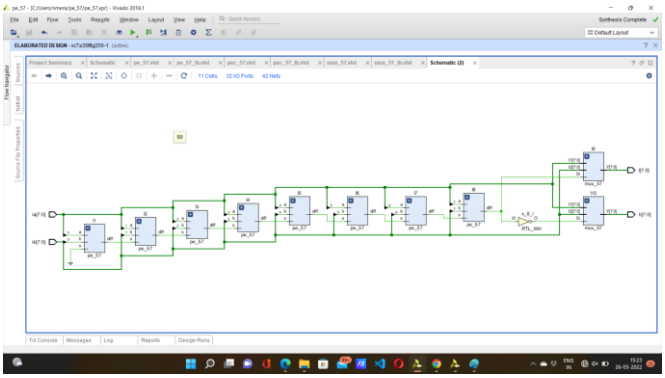

Fig 3.6 RTL output of Mux based data comparator

The outputs of the above comparators are simulated using the Xilinx software and the power consumption by each comparator is compared with each other and also the number of cells that is the number of basic gates used in each comparator is compared based on that the comparator is used.

Table -2: Comparison of Data comparators

Comparator	Power	No.of cells
Conventional Bit-wise comparator	0.101 w	55
Borrow look Ahead data comparator	0.071 w	46
Mux Based data Comparator	0.097 w	55

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