International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 09 Issue: 06 | June 2022 www.irjet.net p-ISSN: 2395-0072

MODIFIED CARRY SELECT ADDER WITH BKA AND MGDI TECHNIQUE

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Abstract -*In the area of VLSI design, summing circuits are one of the most widely used entities in processor data path architecture. Therefore, the performance of a processor is greatly influenced by the action of the resident adders. With the advances in VLSI technology, research works are emerging on designing architecture with low power consumption, high speed, less area, or a combination of them. The thing is no existing adders can fulfill all these 3 criteria. Here we are implementing a modified carry select adder with Brent Kung adder using the modified gate diffusion input technique. A carry select adder consists of multiple pairs of Ripple carry adders which give it the most complex design and longer computation time and thus the performance of the CSA will dropdown. Hence, we replaced RCA with BKA which is a parallel prefix adder that has the best performance till now. So,with this replacement, the performance of the CSA gets improved but the area consumption and the power consumption will be increased. For that, we are using the MGDI technology. MGDI is the latest technique that reduces the number of transistors and thereby the area and power consumption. Therefore, all three criteria are satisfied in this modified CSA adder.*

***Key Words*:CSA, BKA, MGDI, Parallel prefix adder, Area, Power, Delay**

1. INTRODUCTION

Adders are the fundamental building blocks of digital circuit design. Adders are the elementary blocks in various data processors, so if the adder is an inefficient one then it will affect the overall performance of the processor. Hence, the adder must be efficient and good in performance. The three major parameters that affect the performance of an adder are area, delay, and power. No existing adders satisfy all these 3 criteria. Conventional adders such as RCA, CLA, CSA, etc. are not much efficient to meet the requirements of the new technology. Therefore, in current technology, the parallel prefix adders are the fastest adders with better performance. Even though chip area and power consumption are less, high-speed addition of large numbers is possible. Primitive carry select adder consists of multiple pairs of RCAs which gives it a more complex design and longer computation time, this makes the CSA low in performance. Here we replace these RCAs with BKAs which is a parallel prefix adder. To make the adder area-efficient we introduce MGDI technology, which effectively reduces the number of transistors.

1.1 Preliminary background

Parallel prefix adders are one of the most high-performance adders with less design complexity. In a parallel prefix adder, the computation of carry occurs simultaneously. This parallel computation of carries makes it fastest in its performance. There are three main stages for the computation. They are the pre-processing stage, carry generation stage, and post-processing stage. In preprocessing, the computation of generate and propagate signals of corresponding pairs of inputs occurs. The equations of generate and propagate signals are given below:

$$pi = ai \oplus bi \quad (1)$$

$$gi = ai \,.\, bi \quad (2)$$

The carry generation stage includes the computation of carries corresponding to each pairs of input bits. The equation for carry generation is as follows:

$$pi : j = pi : k \,.\, pk\text{-}1 : j \quad (3)$$

$$gi : j = gi : k + (pi : k \,.\, gk - 1 : j) \quad (4)$$

The post-processing stage includes the computation of the final sum bits. The equation for the post-processing stage is as follows:

$$si = pi \oplus ci\text{-}1 \quad (5)$$

A. Pre-processing stage

Thepre-processing stage is the first stage in the parallel prefix adder. It includes the computation of pi and gi signals as shown in equations (1) and (2).

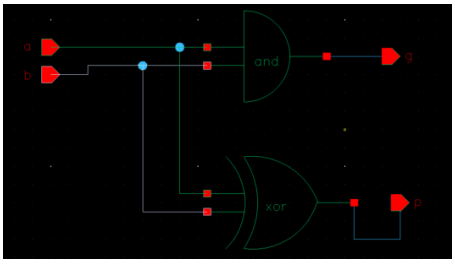

Fig-1: Pre-processing stage

B. Carry generation stage

In this stage, carry computation occurs. The carry signal generated from one stage will proceed to the next stage and this process continues for all other stages. The equation for the computation is shown in equations (3) and (4).

Black cell: Black cell performs the computation of both propagate and generate signals. It is a combination of both grey cells and AND gate.

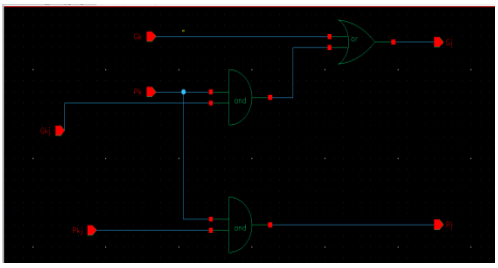

Fig-2: Black cell

Grey cell: Grey cell computes the generate signals which are used in the computation of sum bits in the post-processing stage. It is a combination of AND and OR gates.

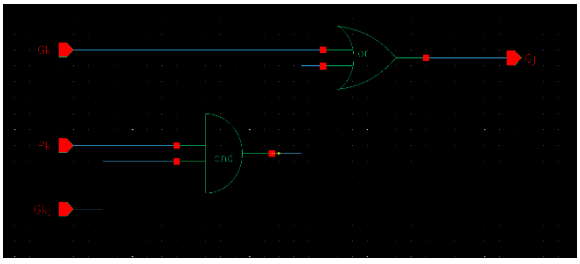

Fig-3: Grey cell

Buffer cell: A buffer cell is used to balance the loading effect. It is a combination of NOT gates in series. It also strengthens electronic signals.

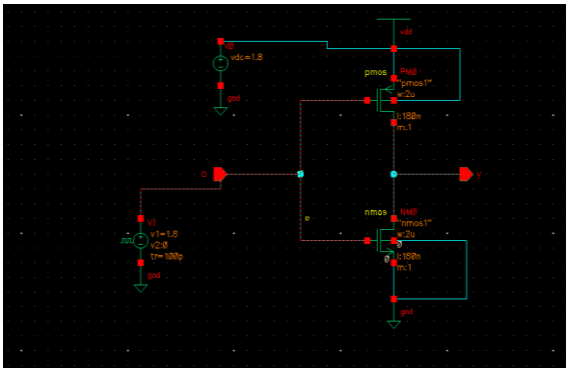

Fig-4: Buffer cell

These three cells combine to form the carry generation stage. The diagram of the carry generation block is as follows:

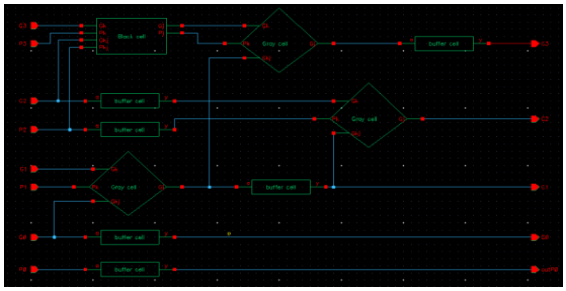

Fig-5: Carry generation stage

C. Post-processing stage

This is the final stage in the parallel prefix adder computation. In this stage, the final sum bits are obtained. The procedure to obtain the final sum bits are shown in equation (5).

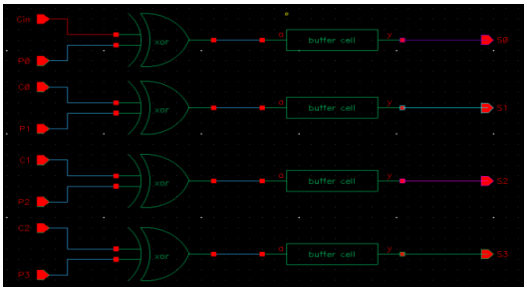

Fig-6: Post-processing stage

1.2 DESIGN METHODOLOGY

A simulation study of a 16-bit modified carry select adder using the cadence virtuoso tool is developed by following the steps shown below:

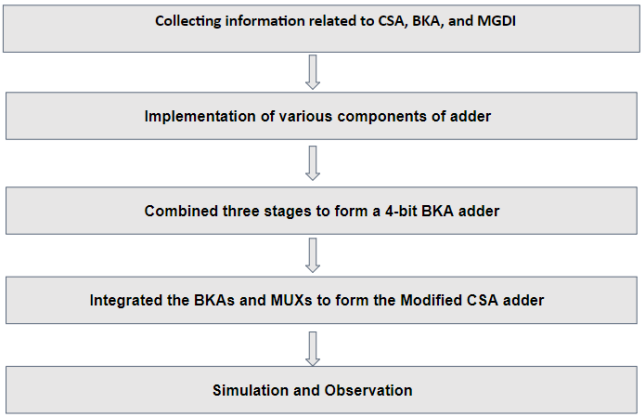

Fig-7: Flowgraph

A. Basic logic gates

The basic logic gates are the fundamental building blocks of any digital circuit. There are seven basic logic gates among all of them we use the three logic gates such as AND, OR, and XOR. All these gates are implemented using the MGDI technique which in turn reduces the number of transistors in each gate. Hence, the area consumed by each gate will be less than the CMOS logic.

AND gate: The AND gate which is implemented by CMOS technology will be having at least a set of 6 transistors but the AND gate that we implement by MGDI technology needs only 2 transistors which means we can save up to 4 transistors in a single AND gate. We need plenty of AND gates in our design of an adder so this reduction is very significant according to us. The transistor-level diagram of AND gate using the MGDI technique is shown below:

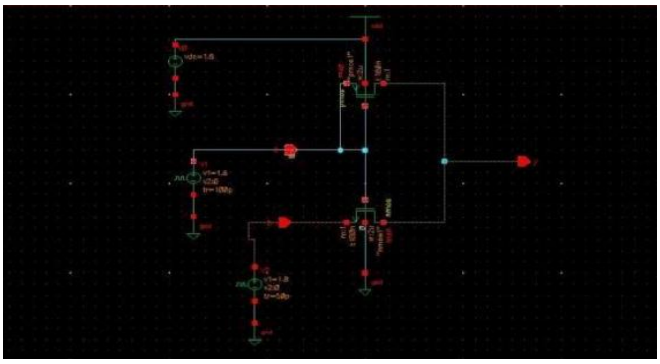

Fig-8: AND gate

OR gate: The same is applicable for OR gate also, a CMOS logic OR gate structure requires 6 transistors but an MGDI OR gate needs 2 transistors for its working.

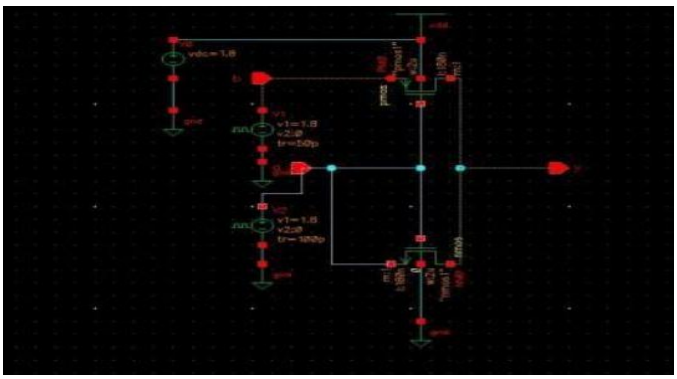

Fig-9: OR gate

XOR gate: In the case of the XOR gate, we need only 3 transistors for its working by MGDI technique, the same xor should need a 6-transistor setup to work in a CMOS technique. so, in a xor gate also we saved up to 3 transistors.

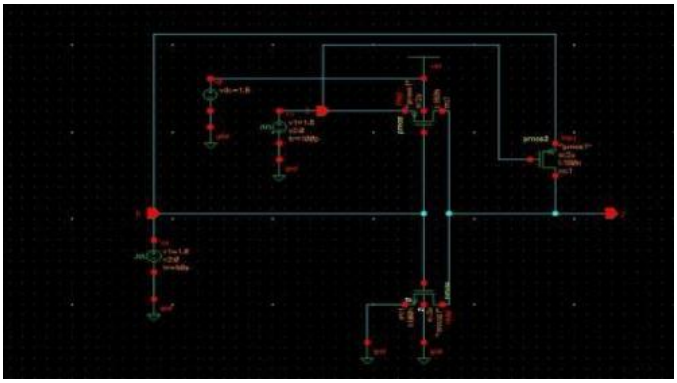

Fig-10: XOR gate

2. BRENT KUNG ADDER

Brent kung adder is a fastest adder among all the parallel prefix adders. It has a very simple design architecture and wiring complexity is very less. It has three intermediate stages from input to output, they are pre-processing, carry generation, and post-processing. . Parallel prefix adders are a unique class of adders that are more efficient in their work than all other primitive adders and they are based on generating and propagating signals. In our proposed BKA model we implemented each stages of BKA using MGDI technique. Thus the number of transistors required is very less compared to the CMOS technique. Hence the area consumption is reduced. In BKA the critical path is very less, since it is a parallel prefix adder thus the delay will be very less.

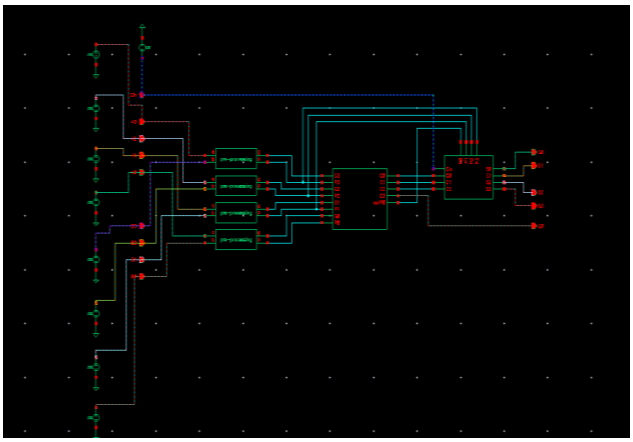

Fig-11: 4-bit BKA

3. MULTIPLEXER

Multiplexers are structural blocks that select between multiple input signals. A multiplexer has multiple data inputs in1, 2, …N, a select line sel, and a single output signal out. The value of the select line determines which input signal should be shown on the output. The muxes used here in this project are 2:1 muxes. That means there

will be two input signals to select between (in0 and in1) and the select line will be a single bit. If the select line is 0, then the output signal is in0. If the select line is 1, then the output signal will be in1.In this project, we use the mux to select the zero carry or one carry sum from the BKAs. Here we use several pairs of muxes for this work. This is a very significant step in the addition calculation of our modified CSA. Mux will select the desired output from one of the adders and will output it, which is the final sum output of our modified CSA.

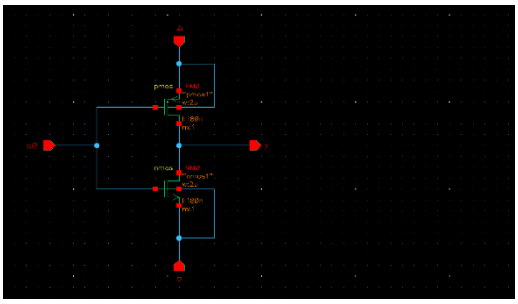

Fig-12: 2:1 Multiplexer

4. CARRY SELECT ADDER

Carry select adder is one of the oldest but still most relevant basic adder. Its non linear dependency for the calculation of the carry output makes it distinct and most used principle in modern adders. CSA will calculate the output for carry for all possible inputs ie; logic input 1 and 0. The calculation for possible input is done by using adders. Multiplexer is used to select between the generated possible outputs. Hence it is clear that CSA does not have to wait to generate output, this makes this adder one of the fastest adder.

5. PROPOSED ADDER

The modified carry select adder we implemented has differences from the original carry select adder in 2 areas, that are, RCAs are replaced with BKAs which are one of the most high-performance adders existing. In carry select adder always 2-bit RCAs are used but here we efficiently used 4-bit BKAs. The second difference is in the usage of multiplexers, multiplexers are placed in a different way in the implementation. Carry Select Adder uses a pair of Ripple Carry Adders (RCA) for Cin=0 and for Cin=l but as we know the performance of RCAs is not that excellent and RCAs create a much large delay for higher bit calculations, so in this project, we replace these RCAs with BKAs which is one of the most efficient and fastest parallel prefix adders existing. But as we know by replacing RCAs with BKAs we can only satisfy the performance need of our new adder, our strategy is to form a new adder with excellent power, performance, and area consumption. So, we have to minimize the area consumption for that here we use the MGDI technology or the modified gate diffusion input technology. This technology is all about the reduction of the number of transistors from the gate level. By using just 2 transistors we can build each of the gates which helps us in a great area reduction. So, by such a reduction in the number of transistors, the power consumption will also be significantly reduced and thus we satisfied all the three factors for an efficient adder.

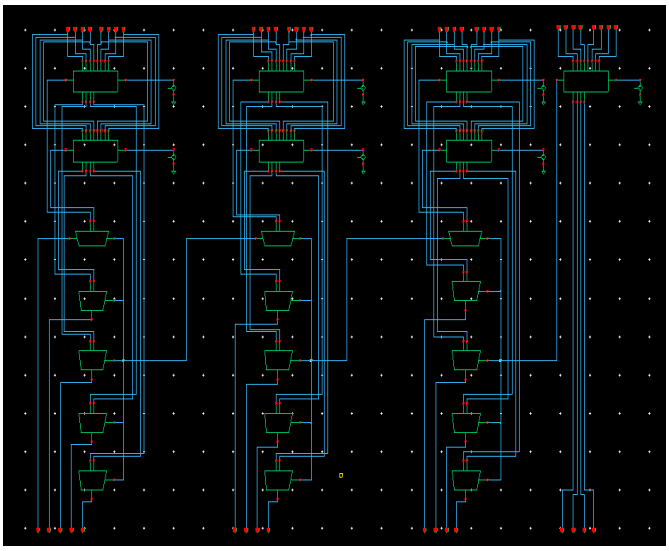

Fig 5.1. Modified Carry Select Adder

6. RESULT AND DISCUSSION

Conventional Carry Select Adder consists of ripple carry adder. Brent Kung adder has reduced delay as compare to ripple carry adder. We use tree structure from in Brent Kung adder to increases the speed of arithmetic operation.

The project performs in EDA Tool, Cadence Virtuoso. One of the three parameters, Area is also calculated in this tool. The graphical representation of comparison of area in conventional CMOS logic and by using MGDI technique is shown in fig. 6.1

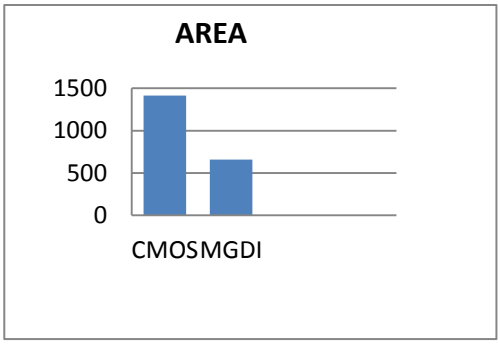

Fig 6.1: Comparison of area between CMOS and MGDI technique in Cadence Virtuoso tool

The result analysis shows that MGDI technique shows better results than the conventional CMOS logic in terms of area.

Power and delay is other design parameter. Power consumption and delay of this circuit is calculated in Cadence Virtuoso. . The graphical representation of comparison of power consumption and delay in conventional CSA and CSA with BKA is shown in fig 6.2. The result analysis shows that CSA with BKA shows better results than the conventional CSA in terms of Power consumption and delay.

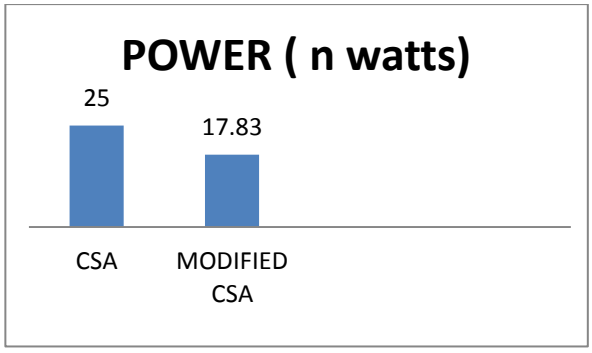

Fig 6.2: Comparison of power between CSA and modified CSA in Cadence Virtuoso tool

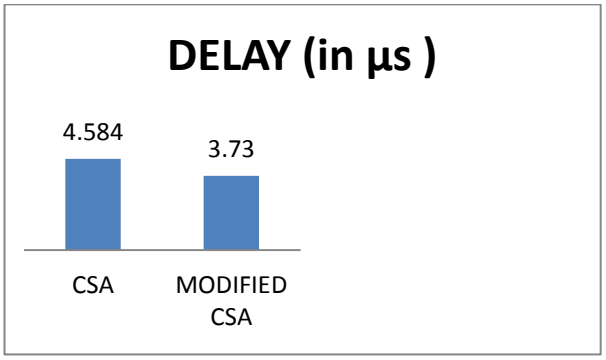

Fig 6.3: Comparison of delay between CSA and modified CSA in Cadence Virtuoso tool

6. CONCLUSIONS

IC design has always sought the best possible performance on IC development in terms of speed, power consumption, and area. This study paper found that incorporating the MGDI technique in any design can reduce the area of the circuit to a most satisfying extent. This work may also be expanded to a larger number of bits. With the advent of parallel prefix adder, the latency and power consumption of various adder designs are lowered. Brent Kung adder is chosen because parallel prefix adders produce quick results. When compared to conventional CSA adder architectures, the calculated results show that BKA Carry Select Adder is better in terms of power consumption and high speed, and can be used in various adder applications such as multipliers, to execute different Digital Signal Processing algorithms such as Finite Impulse Response, Infinite Impulse Response, and so on.

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