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Implementation and Comparative Analysis of 2x1 Multiplexers Using Different Dynamic Logic Techniques

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Abstract - *VLSI designers' major goal in today's technological environment is to optimize power, time delay, and area. Minimizing power consumption and time delay using traditional VLSI design approaches is a challenging work for designers. This can be avoided by transitioning to a new technological age, i.e., by shifting from conventional CMOS design to Dynamic Style of design. This paper discusses about the implementation of 2x1 Mux using various Dynamic Logic Techniques and their comparative analysis are observed using Mentor Graphics Tools with 130nm Technology. This paper also discusses Schematic Design, Output Waveforms, and Delay Calculations for both Single gated and Double gated logics, as well as the various design techniques such as Conventional CMOS Logic, Pseudo NMOS Logic, Complementary CMOS (C2 MOS) Logic, Domino Logic, and Low Power Feed Through (LPFTL) Logic.*

Key Words: VLSI Design, CMOS, Dynamic Gate, Pseudo NMOS, C2MOS, LPFTEL, Mentor Graphics.

1.INTRODUCTION

Since the previous decade, VLSI engineers have taken a consistent approach to the development of various devices that consume less power, run at high speeds, and take up less space. Because low-power portable gadgets are so important to consumers in today's society. Designers face a hurdle in building a device that meets all of the customers' needs while considering all of these factors. Traditional design strategies are insufficient for creating an efficient system. As a result, various advanced design techniques are required to provide users with a better experience.

2.OVERVIEW OF 2X1 MULTIPLEXER

A multiplexer is a digital device that has N select lines, 2 power N input lines, and one output. At an instant depending upon the control signal at the select line only one input line is selected. Multiplexer is also known as a many to one digital switch. A simple 2x1 Mux module and its truth table is shown in the Fig. 1 below and Table 1 respectively.

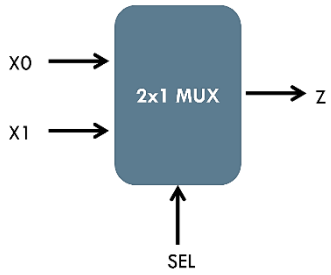

Fig-1: Generic Diagram 2×1 Multiplexer.

Table -1: Truth Table of 2x1 Multiplexer.

SEL	X0	X1	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

3.ANALYSIS OF DESIGN STYLES FOR IMPLEMENTATION OF 2X1 MULTIPLEXER

A total of ten different design styles are being implemented, simulated, and compared in this paper which are CMOS logic, COMS logic with Double Gate, Pseudo NMOS logic, Pseudo NMOS logic with Double Gate, C2MOS logic, C2MOS logic with Double Gate, Domino logic, Domino logic with Double Gate. LP FTL logic, and LP FTL logic with Double Gate. All Multiplexers are designed using Field Effect Transistors.

3.1 Conventional CMOS Logic

In conventional CMOS logic, two networks (Pull-Up Network and Pull-Down Network) are coupled at one output node. PMOS devices make form a Pull-Up Network, whereas NMOS devices make up a Pull-Down Network. When the Pull-Down Network is turned ON, the output is connected to the ground (Logic 0), and when the Pull-Up Network is turned ON, the output is connected to the VDD (Logic 1). A generic

representation of conventional CMOS logic is as shown in Fig. 2.

Analysis of power consumption and time delay are performed in mentor graphics 130nm technology. Fig.3 and Fig. 4 represents the Schematic representation of single gated and double gated Conventional CMOS Logic 2x1 Multiplexer respectively. Power consumption and time delay observed by this schematic design are tabulated in Table II under results section.

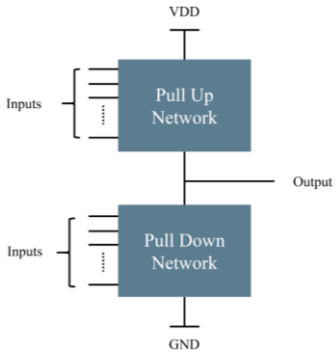

Fig-2: Module representation of Conventional CMOS Logic.

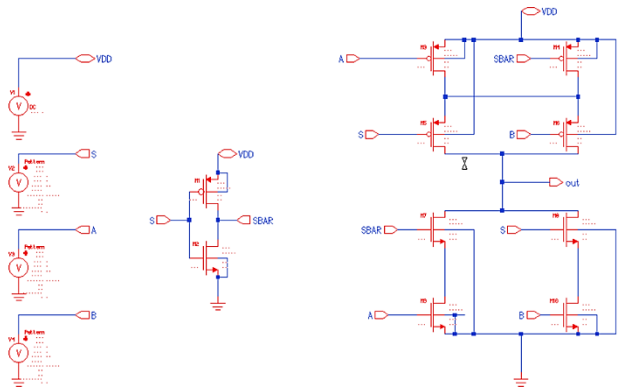

Fig-3: Schematic representation of Conventional CMOS Logic 2x1 Multiplexer.

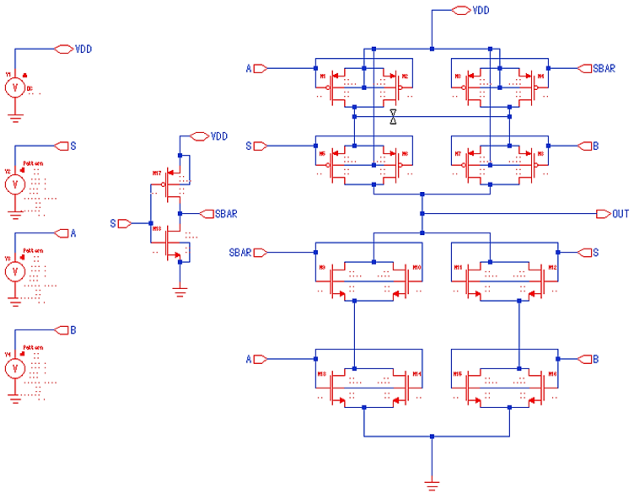

Fig-4: Schematic representation of Conventional CMOS Logic Double Gated 2x1 Multiplexer.

3.2 Pseudo NMOS Logic

A Pseudo NMOS logic design also consists of Pull-Up Network and Pull-Down Network connected at output node. But in case of Pseudo NMOS logic Pull-Up Network is always a PMOS device whose gate terminal is connected ground. And the Pull-Down Network remains same as Conventional CMOS logic. A generic representation of Pseudo NMOS logic is as shown in Fig. 5.

Compared to CMOS logic Pseudo NMOS logic consist of fewer transistors. Only (N+1) FETs are required for N input logic. Since the grounded gate at Pull-Up Network, the pFET has been biased active. Schematic representation of single gated and double gated Pseudo NMOS Logic 2x1 Multiplexer are as show in Fig. 6 and Fig. 7 respectively.

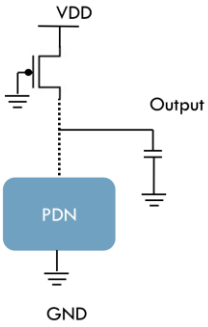

Fig-5: Module representation of Pseudo NMOS Logic.

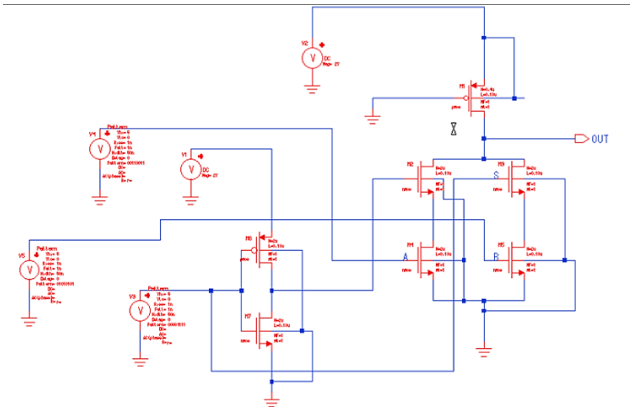

Fig-6: Pseudo NMOS Logic Schematic Diagram for 2×1 Multiplexer.

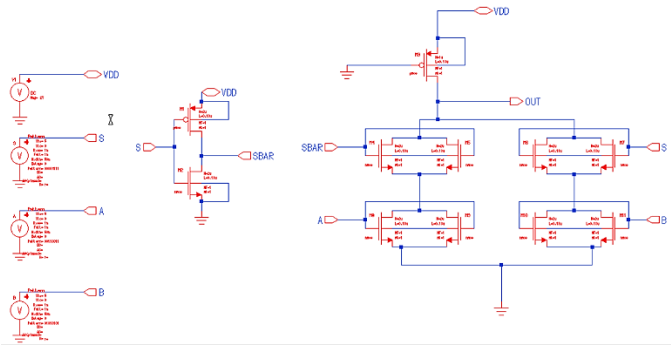

Fig-7: Pseudo NMOS Logic Schematic Diagram for Double Gate 2×1 Multiplexer.

3.3 C2MOS Logic

C2MOS (C Square MOS) stands for Clocked CMOS logic. C2MOS logic is essentially a modification of static CMOS logic, with an additional PMOS transistor whose gate terminal is connected to the Complimented Clock signal (CLK_bar) and an NMOS transistor whose gate terminal is connected to the actual Clock signal (CLK). Like static CMOS logic Pull-Up Networks are made up of PMOS transistors, whereas Pull-Down Networks are made up of NMOS transistors, CLK_bar and CLK are complementary clock signals that should preferably not overlap. Fig. 8 represents the basic structure of C2MOS logic.

When CLK=1 and CLK_bar=0 both Mn and Mp transistor are in ON state, since both the transistors are ON that implies there is short circuit between Pull-Up and Pull-Down Network, hence current starts flowing which offers a low impedance and the network is now reduced to static CMOS circuit. Depending up on the inputs circuit will generate output either Logic 1 or Logic 0.

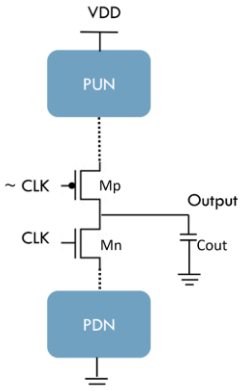

Fig-8: Basic Structure of C2MOS Logic.

When CLK=0 and CLK bar=1 Since both Mn and Mp transistors are turned OFF, the Pull-Up and Pull-Down Networks are separated from the output node. As a result, inputs have no influence on the output node, which is now in a high-impedance state. Until CLK=1, the output is stored on the capacitor Cout. Schematic representation of both single gated and double gated C2MOS Logic 2x1 Multiplexer are as show in Fig. 9 and Fig. 10 respectively.

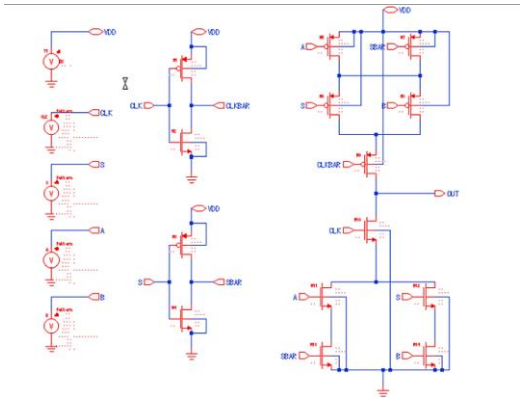

Fig-9: C2MOS Schematic Diagram for 2×1 Multiplexer.

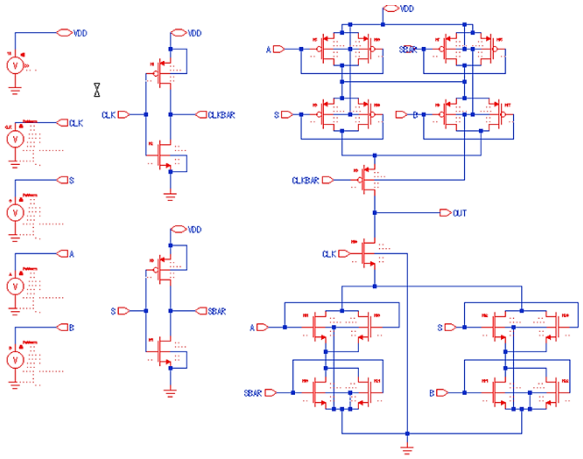

Fig-10: C2MOS Schematic Diagram for Double gate 2×1 Multiplexer.

3.4 Domino Logic

Domino logic is a design style that eliminates the cascading problem observed in dynamic CMOS logic. In a domino CMOS logic, a dynamic CMOS logic has been cascaded with a static CMOS inverter. A basic structure of Domino logic is as shown in Fig. 11.

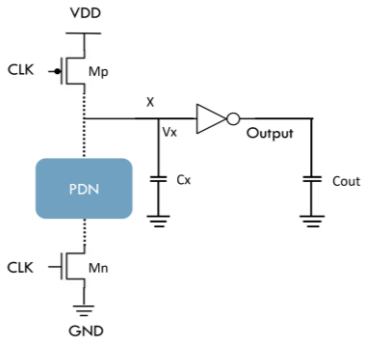

Fig-11: Basic Structure of Domino Logic.

Regardless of the inputs in the Pull-Down Network, when CLK=0, pre-charge transistor Mp is switched ON and evaluation transistor Mn is turned OFF. Cx capacitor pre-charges to VDD at node X, thus Vx=VDD. This value of Vx is now applied to a static CMOS inverter, resulting in Vout=0v at the inverter's output.

When CLK=1 pre-charge transistor Mp is switched OFF and evaluation transistor Mn is turned ON. Now if the Pull-Down Network is OFF, then pre-charge voltage of Vx=VDD will be retained on Cx capacitor and Vout=0v will be retained on Cout. If the inputs are such that Pull-Down Network is ON, then Cx discharges to 0V via Pull-Down Network and Mn transistor, therefore Vx=0V. Node X is conditionally discharged to ground based on Pull-Down Network. A discharge of Cx results in a output of Vout=VDD (Logic 1). Schematic representation of both single gated and double gated Domino Logic 2x1 Multiplexer are as show in Fig. 12 and Fig. 13 respectively.

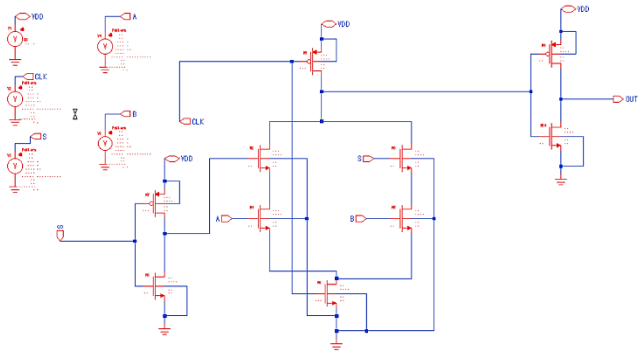

Fig-12: Domino Logic Schematic Diagram for 2×1 Multiplexer.

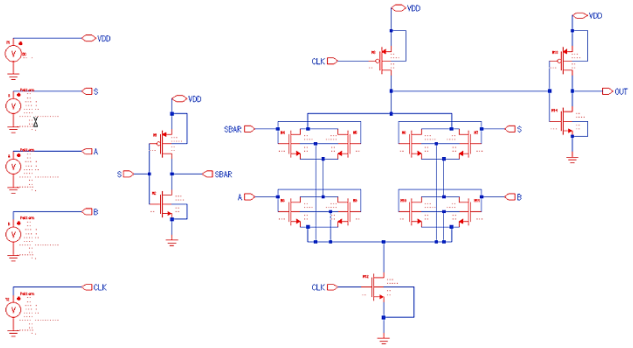

Fig-13: Domino Logic Schematic Diagram for Double gate 2×1 Multiplexer.

3.5 Low Power Feed Through (LPFT) Logic

LPFTL was proposed to enhance domino logic performance. Domino logic had various restrictions, which were eliminated in FTL. A Pull-Down Network, a PMOS load transistor P1, and a reset transistor N1 are used in circuits design. Inputs are applied at the Pull-Down Network. Clock signal is connected to the gate inputs of load transistor P1 and reset transistor N1. A basic structure of LPFTL is as shown in Fig. 14.

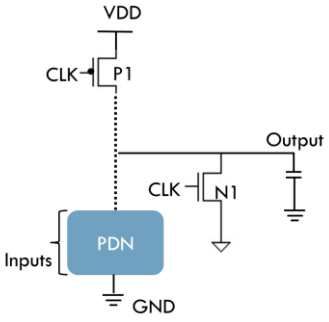

Fig-14: Low Power Feed Through Logic Design Representation.

The circuit operates in two stages: reset and evaluation. The clock is high during the reset phase, therefore load transistor P1 is turned OFF and reset transistor N1 is turned ON, and the output is reset to a low logic level. The load transistor P1 is ON and the reset transistor N1 is OFF throughout the evaluation phase, and the output either charges to logic high or remains at logic low depending on the inputs to the PDN block. Schematic representation of both single gated and double gated LPFTL 2x1 Multiplexer are as show in Fig. 15 and Fig. 16 respectively.

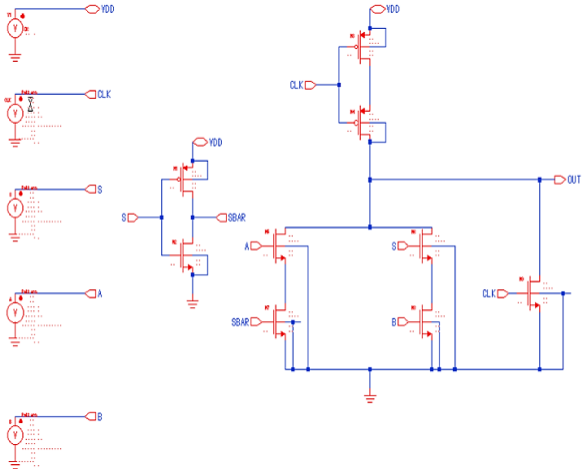

Fig-15: LPFTL Schematic Diagram for 2×1 Multiplexer.

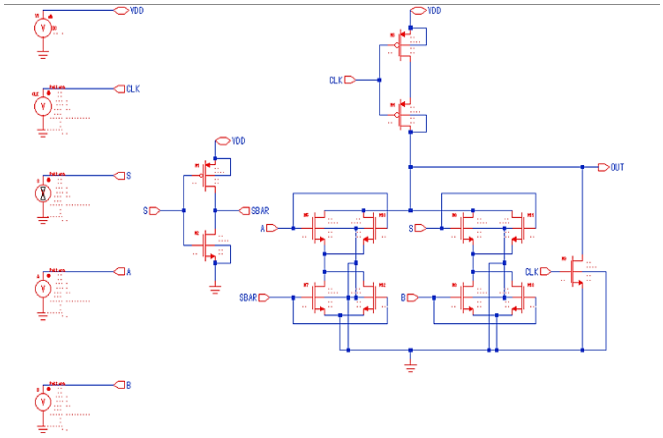

Fig-16: LPFTL Schematic Diagram for Double gate 2×1 Multiplexer.

4.RESULT

In this section results of various design styles are being simulated, observed, and tabulated in the Table II. Also, the plot with respect to Power Consumption and Time Delay are depicted in Fig. 37 & Fig. 38.

Fig. 17, 19, 21, 23, 25, 27, 29, 31, 33, & 35 shows the output waveform for conventional CMOS, Double gated CMOS, Pseudo NMOS, Double gated Pseudo NMOS, C2MOS, Double gated C2MOS, Domino, Double gated Domino, LPFT, & Double gated LPFT logic 2X1 Multiplexer respectively. Fig. 18, 20, 22, 24, 26, 28, 30, 32, 34, & 36 shows the Time delay observed for conventional CMOS, Double gated CMOS, Pseudo NMOS, Double gated Pseudo NMOS, C2MOS, Double gated C2MOS, Domino, Double gated Domino, LPFT, & Double gated LPFT logic 2X1 Multiplexer respectively.

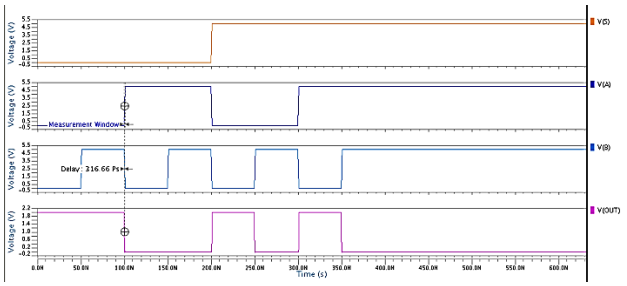

Fig-17: Output waveform for conventional CMOS logic 2x1 MUX.

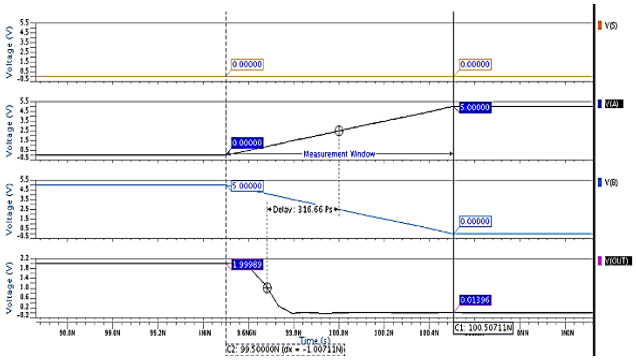

Fig-18: Time delay observed for conventional CMOS logic 2x1 MUX.

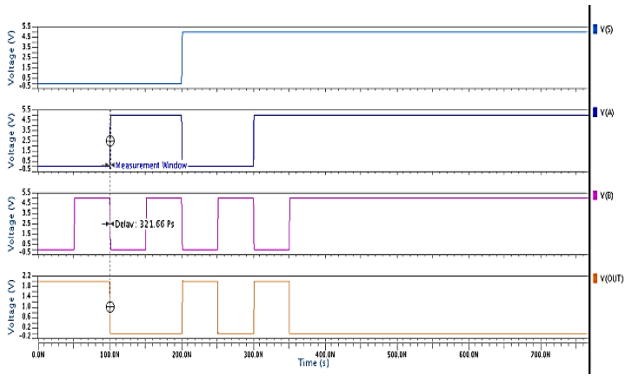

Fig-19: Output waveform for double gated CMOS logic 2x1 MUX.

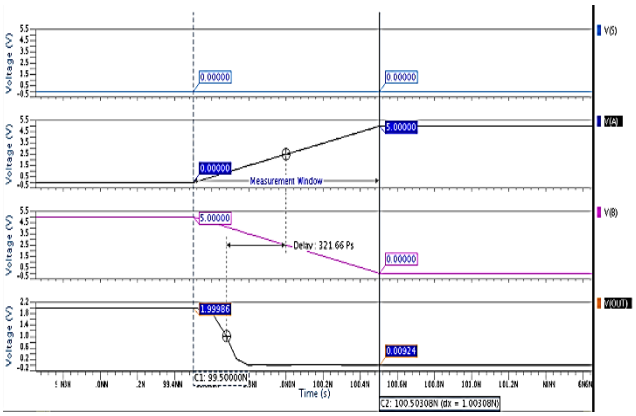

Fig-20: Time delay observed for double gated CMOS logic 2x1 MUX.

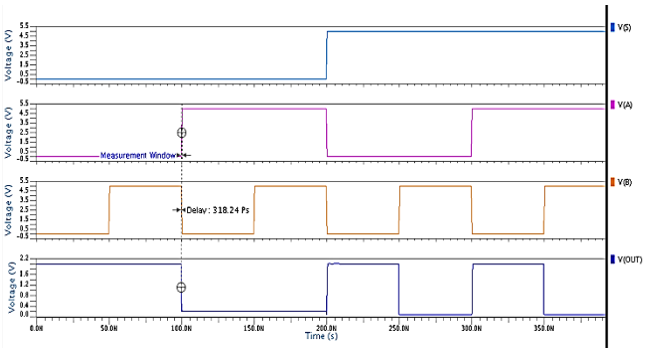

Fig-21: Output waveform for Pseudo NMOS logic 2x1 MUX.

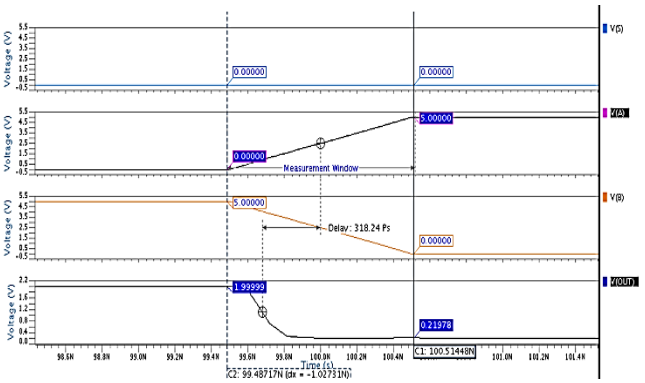

Fig-22: Time delay observed for Pseudo NMOS logic 2x1 MUX.

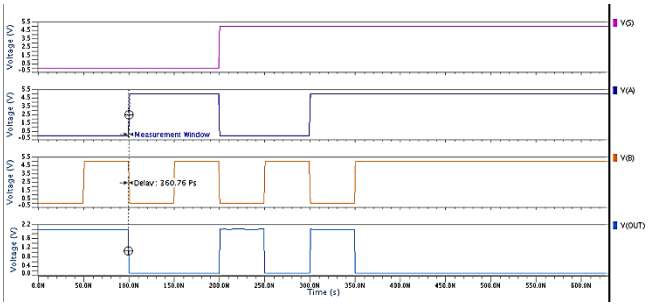

Fig-23: Output waveform for double gated Pseudo NMOS logic 2x1 MUX.

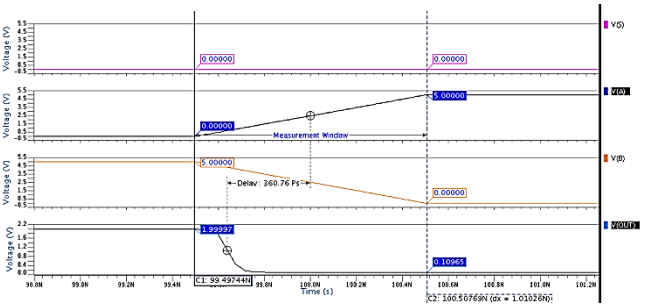

Fig-24: Time delay observed for double gated Pseudo NMOS logic 2x1 MUX.

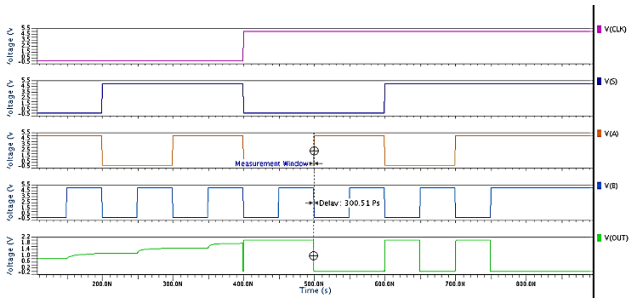

Fig-25: Output waveform for C2MOS logic 2x1 MUX

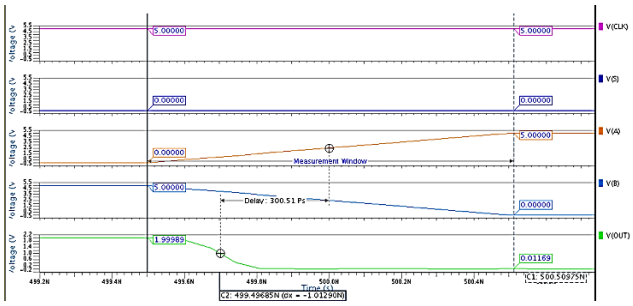

Fig-26: Time delay observed for C2MOS logic 2x1 MUX.

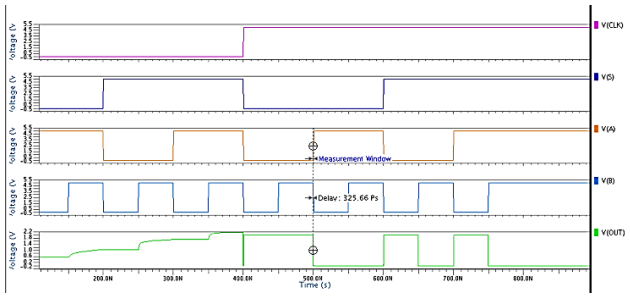

Fig-27: Output waveform for double gated C2MOS logic 2x1 MUX.

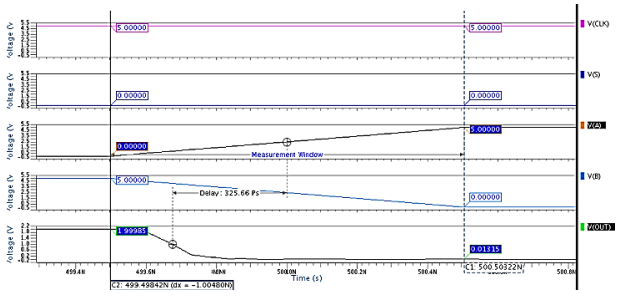

Fig-28: Time delay observed for double gated C2MOS logic 2x1 MUX.

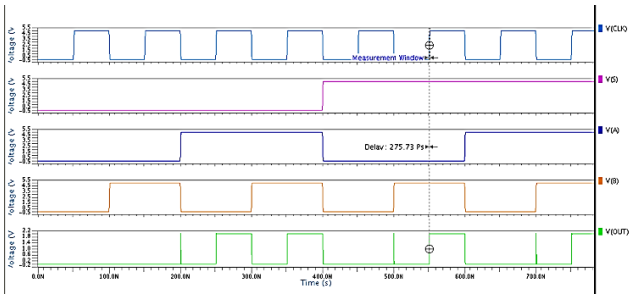

Fig-29: Output waveform for Domino logic 2x1 MUX.

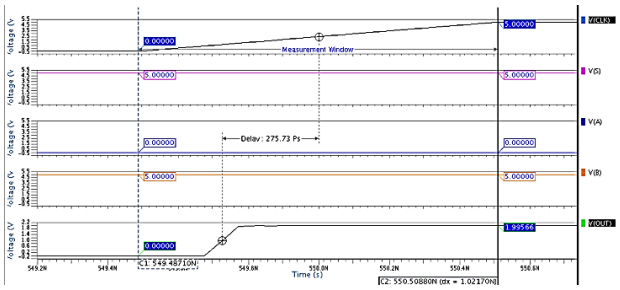

Fig-30: Time delay observed for Domino logic 2x1 MUX.

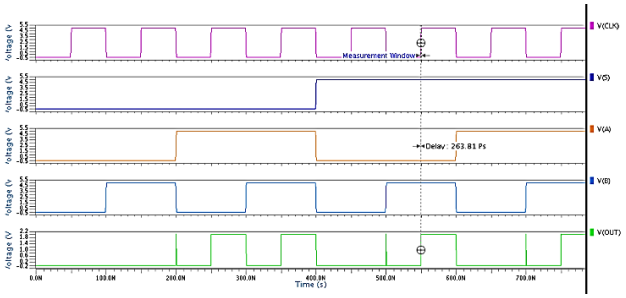

Fig-31: Output waveform for double gated Domino logic 2x1 MUX.

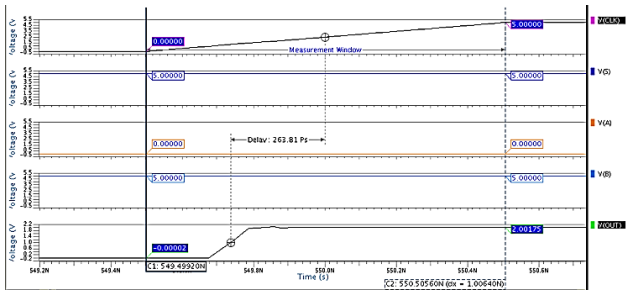

Fig-32: Time delay observed for double gated Domino logic 2x1 MUX.

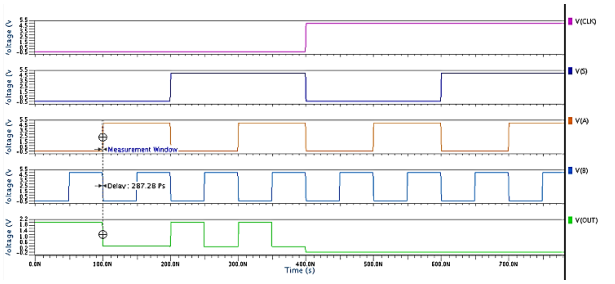

Fig-33: Output waveform for LPFTL 2x1 MUX.

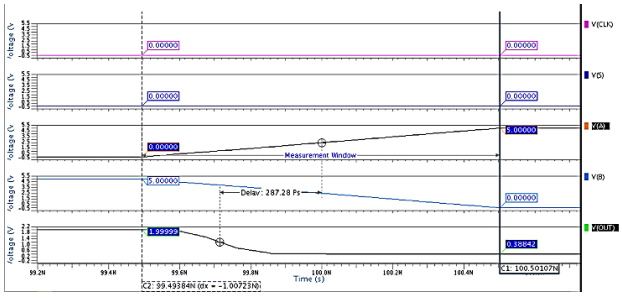

Fig-34: Time delay observed for LPFTL 2x1 MUX.

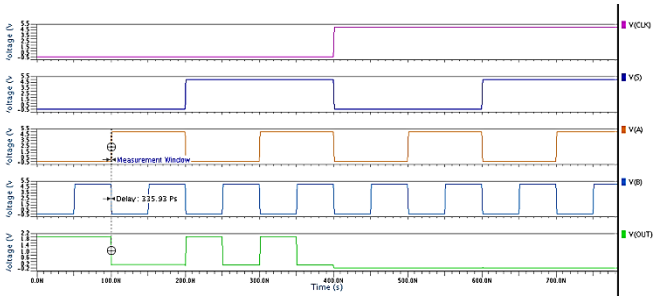

Fig-35: Output waveform for double gated LPFTL 2x1 MUX.

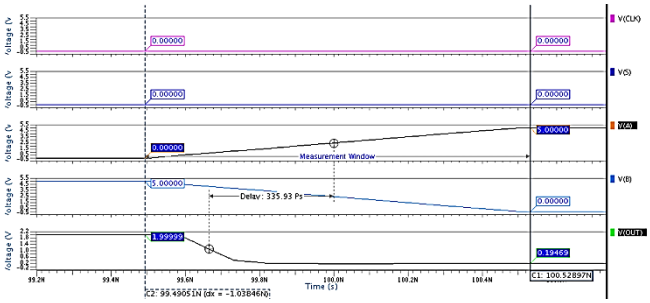

Fig-36: Time delay observed for double gated LPFTL 2x1 MUX.

Table -2: Observed Results Of 2x1 Multiplexer Using Different Design Styles

Sl. No.	Design	Power (nW)	Delay (pSec)
1	CMOS	6.1226	316.66
2	CMOS DG	25.466	321.66
3	Pseudo NMOS	22.464	318.24
4	Pseudo NMOS DG	25.4663	360.76
5	C2 MOS	6.7718	300.51
6	C2 MOS DG	6.901	325.66
7	DOMINO	4.7061	275.73
8	DOMINO DG	4.7818	263.81
9	LP FTL	9.8491	287.28
10	LP FTL DG	13.5072	335.93

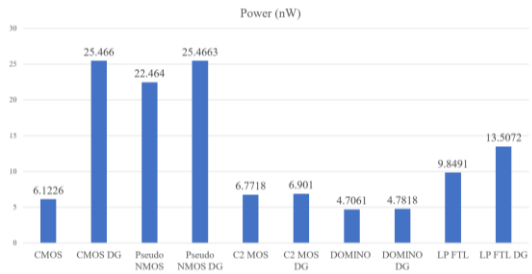

Fig-37: Plot of Power in nW for different Design Styles.

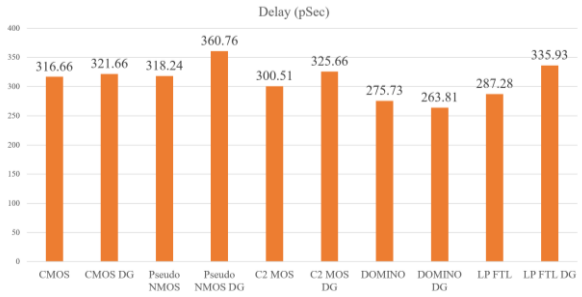

Fig-38: Plot of Delay in (pSec) for different Design Styles.

4.RESULT

Implementation and Comparative Analysis of 2x1 Multiplexers Using Different Dynamic Logic Techniques is focused on designing and simulation of 2x1 Multiplexer using design techniques such as Conventional CMOS Logic, Pseudo NMOS Logic, C2MOS Logic, Domino Logic, and LP FTL Logic using Mentor Graphis 130nm technology environment and to analyse the effective logic for implementation of 2x1 Mux [1].

On successful simulation of the design, results are plotted and tabulated as shown in Fig. 37 & Fig. 38 and Table II. By this evidence implementation of 2X1 Mux using Domino Logic yields Low Power (i.e., 4.7061nW in single gated design and 4.7818nW in double gated design) and Less Time Delay (i.e., 275.73pSec in single gated design and 263.81pSec in double gated design) when compared to other Design Styles.

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