International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 09 Issue: 05 | May 2022 www.irjet.net p-ISSN: 2395-0072

Modeling of DDR4 Memory and Advanced Verifications of DDR4 Memory Subsystem

Pavan G[1], V Siddeswara Prasad[2]

[1] Dept. Of E&IE, Siddaganga Institute of Technology (SIT), Tumkur, India.
[2]Professor, Dept. Of E&IE, Siddaganga Institute of Technology (SIT), Tumkur, India.

Abstract - *In today's computer world, it is very necessary to improve the speed in most electronics devices. People are very much fascinated over new technologies. To fulfil the need of customers, it is a challenge to system designers when it comes to keeping up with speed. In choosing an optimal system, memory plays a vital role in the performance and reliability of system. Memory modules are important components of many very large-scale integration (VLSI) designs. Presently in the market Double Data Rate 3rd Generation (DDR3) and Double Data Rate 4th Generation (DDR4) Synchronous Dynamic Random-Access Memory (SDRAM) are often seen but their memory storage array implementation is not directly available to the user. The aim of the project is to develop a DDR4 memory model using system Verilog that fulfils the specifications of JEDEC Specs given by Solid State Technology Association. The memory model is built with improvisation in its efficiency in terms of data rate when compared to its previous generation. Since the present DDR4 memory model of different companies are confidential (encrypted format), user cannot access it directly. So, modelling of DDR4 memory model helps the user to obtain the decrypted form of DDR4 memory model and helps in further upgradation according to requirements. The tools used for the project are Modelsim 6.3g-p1 and Questasim. The implementation includes DDR4 memory modelling using the System Verilog, verification with Xilinx memory controller. Comprehensive simulations of all scenarios including bypass (Read Write of the same address, on the same cycle) will be performed followed by sequential equivalent checking versus an existing model using the Modelsim tools.*

Key Words: DRAM, DDR3, DDR4, Verilog, FPGA.

1.INTRODUCTION

Most electronics systems use memory components either for storing executable software or for storing data, and therefore the availability of accurate memory models is fundamental to most functional verification strategies. Making these models available in proven, standards-based libraries is essential. Developments in VLSI technology are driven by the never-ending demand for faster processors. Faster processors need faster memory. On chip memory is built using the same technology as the processor but is limited in size [1]. Many microcontrollers have few kilo bytes to few hundred kilo bytes of on chip RAM. However, this memory is hardly sufficient for resident operating system and associated programs. Applications on such devices will need large external RAM. Most of the contemporary data is in the form of images, sound, real time signals, etc. which require very large memory to store and operate. Using Gigabytes of RAM is not very uncommon in current processor scenario [1].

To facilitate system integrators to build such systems, standardization of device interfaces is a necessity. Some of the standard memory interface technologies are SDRAM, RDRAM, DDR SDRAM, etc. There have been several advancements in DDR SDRAM technologies. The earliest SDRAM modules had a clock frequency of 133 MHz [2]. DDR doubled the transfer rate and worked at double the frequency, at 266MHz.

Recent technologies support DDR SDRAM running at 1.6 GHz [2]. While the latest memory technologies are used in high end processors, embedded systems rely on DDR2 running at 266 MHz [3]. DDR family has a common hardware interface. So, it is easy to modify an existing interface hardware to match any other member of the DDR family as shown in Table 1.

Table -1: Comparison of DDR4 With Previous Generation

Parameters	DDR1	DDR2	DDR3	DDR4
Operating Voltage	2.5V	1.8V	1.5V	1.2V
RAM Internal Clock Frequency (MHz)	266-400	533-800	1066-1600	2133-3200
Clock Frequency (MHz)	133-200	266-400	533-800	1066-1600
Bits per cycle	2	4	8	8

1.1 Objective of the Project

The main aim of the project is to build a DDR4 Memory Model using system Verilog to improve the efficiency in terms of data rate when compared to its previous generation. Since the present DDR4 is of encrypted form, which cannot be altered by a user according to their requirements. So, the main objective is to decrypt the DDR4 with reference to DDR3 according to the JEDEC Spec of DDR4 with the help of software tool Modelsim which helps to design a fastest

memory model with high speed and less power consumption. Verification of DDR4 memory model includes comparison of data rate in terms of delay with respect to its previous generation DDR SDRAM.

2. LITERATURE SURVEY

Large-scale research is being done in the field of memory technology to increase the efficiency of memory modelling. This effort has not always been successful because, during the fabrication process, the densely packed memory structures can experience defects. Therefore, it is not suitable to test the memory modules once they are packed. Functional verification of a module along with testing, makes sure that the design works the way it has been designed to perform.

Manikandan Sriram and Mohan Dass have briefly explained theory of the memory model in [2]. A layered test bench has been designed using Universal Verification Methodology (UVM), a standardized class library, which has increased the reusability and automation of the existing design verification language, System Verilog [2].

Prajakta Chandilkar and Dr. Uday Wali have explained about the implementation of finite state machine (FSM) of DDR2 SDRAM module [1].

DDR2 model can be referred to as the basic model for hardware design of other upgraded memory modules. The basic operations such as READ WRITE, and a high-level picture of SDRAM sub systems, is very necessary to understand the basic concept of DDR4 memory model physical structure [1].

Table -2: Read Operation in Both Burst Length Of 4 And 8

Read (A2, A1, A0)	Index starting point
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

DDR3 SDRAM is internally configured as an eight-bank DRAM. To achieve high-speed operation, it uses an 8n prefetch architecture to. A single read or write operation for the DDR3 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins. Read and write operation to the DDR3 SDRAM are burst oriented: start at the selected location with respect to write operation and continue for a burst length of eight or a chopped burst of four in a programmed sequence. Operation begins with an Active command, which is then followed by a read or Write command. The read operation starts with an address corresponding to A2, A1, A0 as shown in Table 2. The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto pre-charge command is to be issued (via A10), and select BC4 or BL8 mode if enabled in the mode register. Prior to normal operation, the DDR3 SDRAM must be powered up and initialized in a predefined manner.

3. SYSTEM OVERVIEW

Block diagram of the complete system is shown in Figure 1 and the pin diagram of DDR4 memory model is given in Figure 6.

DDR4 functional diagram consists of Control logic which controls the overall operations of DDR4, where the Mode Register Set (MRS) command is used to update the control registers. Control registers are used to store parameters related to communication protocol, address mode, refresh rate, command pipeline, data buffering etc. Here the storage elements are memory bank arrays, that consists of multiple numbers of rows and columns. DDR4 consists of four banks i.e., two banks per bank group as shown in Figure 2. On power-up, the ZQ calibration is initialized through ZQCL command as shown in Figure 3. At the same time DQ calibration control block is enabled to reset the DRAM values as shown in Figure 4. Mode Registers can be programmed according to the operations to be performed on the memory model. The pin mapping in the MRS is given in Figure 5 where the RAS-n, CAS-n, WE-n controls the different operations according to the functional table shown in Table 3. Operations begins with the Active command which is used to select the bank and row to be accessed, where BA [1:0] select the bank, and A [17:0] select the row by using Row and Column decoder. MRS programming is done after RESET, which is then followed by WRITE or READ command, after read/write pre-charge command should be issued which ensures that the data is written or read in a memory.

The few scenarios to be checked in any DRAM during operation are:

1. Write and Read to memory location: Perform write to any memory location, read from the same memory location, read data should be same as written data.

2. Write and Read to all memory location: Perform write and read operation to all the memory locations.

3. Default memory value check: Before writing any locations check the default memory value, do read operation to get default values as hFF.

4. Reset in Middle of Write or Read Operation: Apply reset in between write or read operation and check for default values present in memory. (After writing to few locations apply the reset and perform read operation, to get default memory location value hFF.

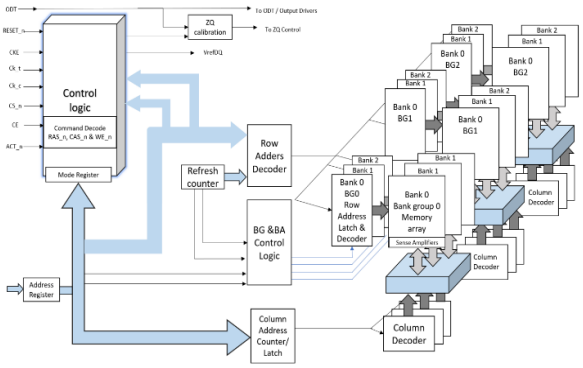

Fig-1: Functional Block Diagram of DDR4.

4. MEMORY MODEL SPECIFICATION

4.1. Memory Bank Array

Memory bank is a logical storage unit of memory which contains the address provided by the user, where this logical address is converted to a physical address before it is given to DRAM. The physical address is made up of Bank Group, Bank, Row, Column where the size of the memory bank is determined by bits in a column and rows. Row column organization of the bank is configured using MRS commands. DRAMs are classified as x4 to x16 based on this column width as shown in Figure 2. The width of DQ data bus is same as the column width. So, DRAMs are classified based on the width of the DQ bus.

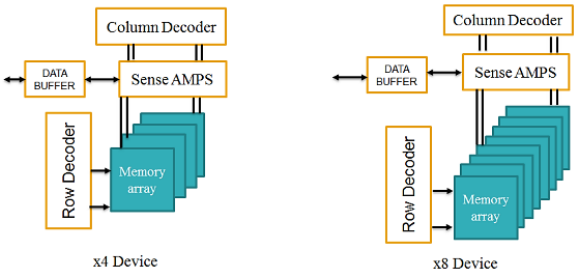

Fig-2:Memory Bank Array.

4.2. Data Buffer

Data buffer is used to temporarily store the data, while it is moving between controller and the memory. DQ is a bidirectional data bus which can be used to read a data from a given address location or write a data to a given address location.

4.3. ZQ Calibration

ZQ Calibration is related to the data pins [DQ] where DQ pin is bidirectional. When a ZQCL command is issued during initialization, the DQ calibration control block is enabled and an internal comparator within the DQ calibration control block tunes the p-channel devices using VOH [0:4] until the voltage is exactly VDDq/2. At this point the calibration has been complete and the VOH values are transferred to all the DQ pins.

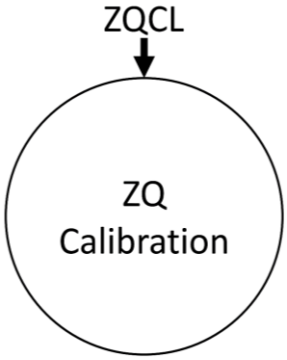

Fig-3: ZQ Calibration

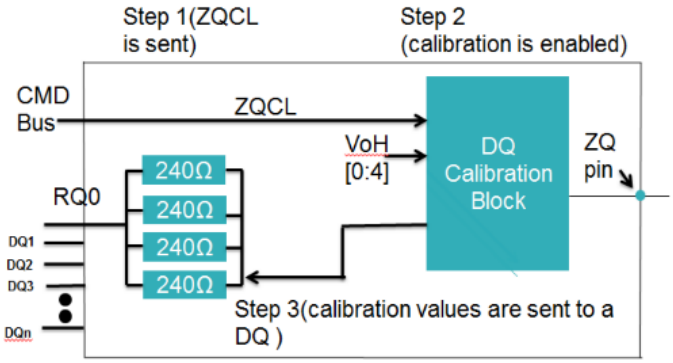

Fig-4: DQ Calibration.

4.4. Mode Register

For application flexibility, various functions, features, and modes are programmable in seven mode registers (MRn) provided by the device as user defined variables that must be programmed via a MODE REGISTER SET (MRS) command. Because thedefault values of the mode registers are not defined, contents of mode registers must be fully initialized and/or re-initialized; that is, they must be written after power-up and/or reset for proper operation. The contents of the mode registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued.

ADDRESS BUS	BG1	BG0	BA1	BA0	A17	RAS_n	CAS_n	WE_n	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
MODE REGISTER	21	20	19	18	17	-	-	-	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Fig-5: Address pin mapping.

4.5. Pin Description

Pin configuration is shown in Figure 6 and each pin carry its own functionality; the functions are as follows:

- Clock (CKt CKc): CKt and CKc are differential clock inputs, where all address and control input signals are sampled at the positive edge of CKt and negative edge of CKc.
- Clock Enable (CKE): It activates all the input signals. Chip Select (CSn): All commands are masked when CSn is registered HIGH.
- Activation Command Input (ACTn): Activation command being entered along with CSn, which activates the DRAM.
- Command Inputs (RASn/A16. CASn/A15. WEn/A14): RASn/A16, CASn/A15 and WEn/A14 define the command being entered for different memory operations. Those pins have multi-function.
- Bank Group Inputs (BG0 - BG1): BG0 - BG1 define to which bank group an Active, Read, Write or Pre-charge command is being applied. BG0 also determines which mode register is to be accessed during an MRS cycle.
- Address Inputs (A0 - A17): Provide the row address for ACTIVATE Commands and the column address for Read or Write commands to select one location out of the memory array in the respective bank.
- Active Low Asynchronous Reset (RESETn): Reset is an active LOW pin which is active during normal operation when it is LOW, and inactive when it is HIGH.
- Data Strobe input / Output (DQS): The Data strobe is essentially a data valid flag. Read data are edge-aligned, write data are cantered aligned.

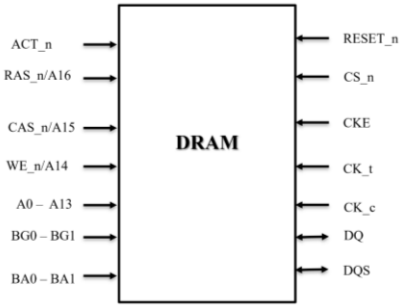

Fig-6: DDR4 memory model pin diagram.

5. STATE TRANSITION DIAGRAM

State diagram describes the state transition diagram for DDR4 SDRAM. There are 10 states. They are Initialization, Idle, Refresh, MRS, Active, Writing, Reading, Pre-charge. command sets to be issued includes RES, REF, ACT, WRITE, READ, PRE and NOP. The different operations can be performed on DDR4 by altering RAS bar, CAS bar, WE bar respectively as shown in Table 3.

Table -3: Functional Table for DDR4 SDRAM

Command	RAS bar	CAS bar	WE bar
NOP/Idle	H	H	H
Read	H	L	H
Write	H	L	L
Pre-charge	L	H	H
Refresh	L	L	H
MRS	L	L	L

5.1. Reset and Initialization Procedure

To ensure proper device function, the power-up and reset initialization default values for the following MR settings are defined as:

- Gear-down mode (MR3 A [3]): 0 = 1/2 rate
- Per-DRAM addressability (MR3 A [4]): 0 = disable
- Maximum power-saving mode (MR4 A [1]): 0 = disable
- CS to command/address latency (MR4 A [8:6]): 000 = disable
- CA parity latency mode (MR5 A [2:0]): 000 = disable
- Hard post package repair mode (MR4 A [13]): 0 = disable.

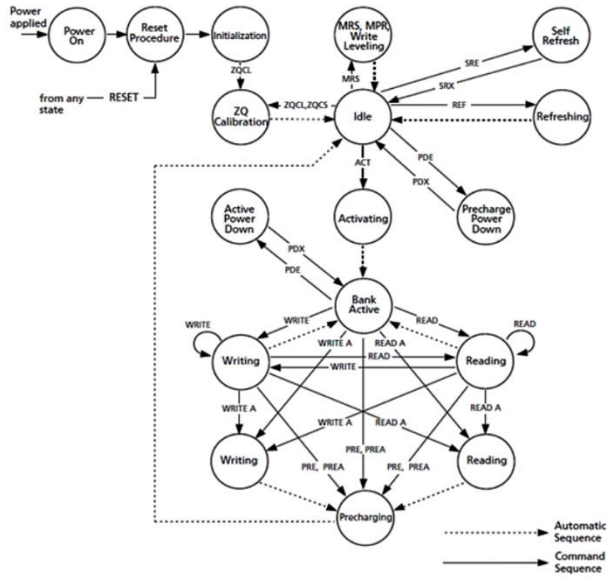

Fig-7: State transition diagram for DDR4 SDRAM.

5.2. Power-Up and Initialization Sequence

The following sequence is required for power-up and initialization:

1. Apply power. RESETn must remain below 0.2 VDD for a minimum of 700s when supplies have ramped up to a valid stable level. CKE is pulled LOW whenever RESETn is de-affirmed (minimum 10ns time). The ramp time of the power voltage from 300mV to VDD, VDD must be greater than or equal to VDDQ and 0.3 (VDD-VDDQ). VPP must be always equal to or higher than VDD. After the VDD went off. RESETn must go high within 10 minutes of VDD ramping up to a stable level. After RESETn goes high, the initialization sequence must be started within 3 seconds.

2.Wait for another 500s but no longer 3 seconds until CKE becomes active after RESETn is de-affirmed. The device will initialize internal state during this time; this will be done regardless of external clocks.

3.Before CKE becomes active, clocks (CKt, CKc) must be started and stabilized for at least 10ns or 5 tCK (whichever is bigger). Since CKE is a synchronous signal, the appropriate setup time must be met to clock (tIS). A DESELECT command must also be recorded at the edge of the clock.

4.Wait a minimum of RESET CKE EXIT time before issuing the first MRS command to load the mode register after CKE is registered HIGH (tXPR = MAX (tXS, 5 tCK).

5. Issue MRS command to load MR3, MR6, MR5, MR4, MR2 and MR1 with all application settings, wait tMRD.

6. Issue MRS command to load MR0 with all application settings, wait tMOD.

7. Issue a ZQCL command to start ZQ calibration.

8. Wait for tDLLK and tZQinit to complete.

Once the DRAM has been initialized, if the DRAM is in idle state longer than 960ms, either (a) REF commands must be issued within tREFI constraints (posting permit specification) or (b) CKE or CSn must switch once within each 960ms idle time interval. On power up, the DDR4 module is in the Idle state which means no operation is being performed or scheduled. It is generally during such periods that auto refresh works in the background to keep the memory contents stable. On power up, pre-charge command is applied to the memory module. If pre-charge command is issued during normal usage, open row of the active bank is deactivated, and the new bank is activated. Therefore, the data before and after the pre-charge command will not be consistent. Once all banks are pre charged, the memory module enters idle state. Then an MRS command should be issued to enable different control signal of DDR4, e.g., DLL reset, burst length, and burst Mode etc. Next a Refresh command should be issued. This command is used to refresh data in selected bank. This command opens a specific memory array bank. You can read or write the memory at this point. Initially, before reading, memory should be written. But this is not true for other memory types, such as flash RAM. To deactivate the current open bank and return the device to idle state, pre-charge command should be issued at the end.

6. SYSTEM SOFTWARE

Designing of DDR4 is done by System Verilog, the operations on DDR4 is analyzed using Modelsim6.3g-p1 and Questasim.

6.1. Modelsim

ModelSim is Mentor Graphics' multi-language HDL simulation environment for simulating hardware description languages like VHDL, Verilog and SystemC, and includes an integrated C debugger. In conjunction with Intel Quartus Prime, Xilinx ISE or Xilinx Vivado, ModelSim can be used independently. Using the graphical user interface (GUI), simulation can be done.

ModelSim increases design quality and debug productivity in addition to supporting standard HDLs. ModelSims technology allows VHDL and Verilog to be transparently mixed in one design. Its architecture enables platform-independent compilation with outstanding native compiled code performance.

Using Modelsim, DDR3 memory model is analyzed by considering the standard timing parameters provided by micron technologies. The commands used to simulate the memory model are:

1. Vlib work
2. Vlog -sv+define+sg125 +define+den4096Mb ddr3.sv ddr3-module.v tb.v
3. Vsim work.tb
4. Add wave -r /*
5. run -all

once the waveforms are obtained, the delay between different operations are tabulated in the Table 4 in the result section.

6.2. Questasim

The Questa Advanced Simulator is Questa Verification Solution's core simulation and debug engine; the comprehensive advanced verification platform that reduces the risk of validating complex FPGA designs. The Questa Advanced Simulator is the core simulation and debug engine of the Questa Verification Solution; the comprehensive advanced verification platform capable of reducing the risk of validating complex FPGA designs.

Using this platform, DDR4 memory model is designed according to the required specifications given by JDEC spec standards. Using Modelsim, DDR4 memory model is analyzed by considering the standard timing parameters provided by micron technologies. The commands used to simulate the memory model are:

1. vlib work

2. vlog -work work +acc -l vcs.log -novopt -sv +define+DDR4-8G-X8 arch-package.sv

3. proj-package.sv interface.sv StateTable.svp MemoryArray.svp ddr4-model.svp tb.sv

4. vsim -novopt tb

5. run -all

once the waveforms are obtained, the delay between different operations are tabulated in the Table 4 under result section. Figure 8 represents the flow of DDR4 memory model with respect to State Transition diagram shown in Figure 7, where the different tasks are defined.

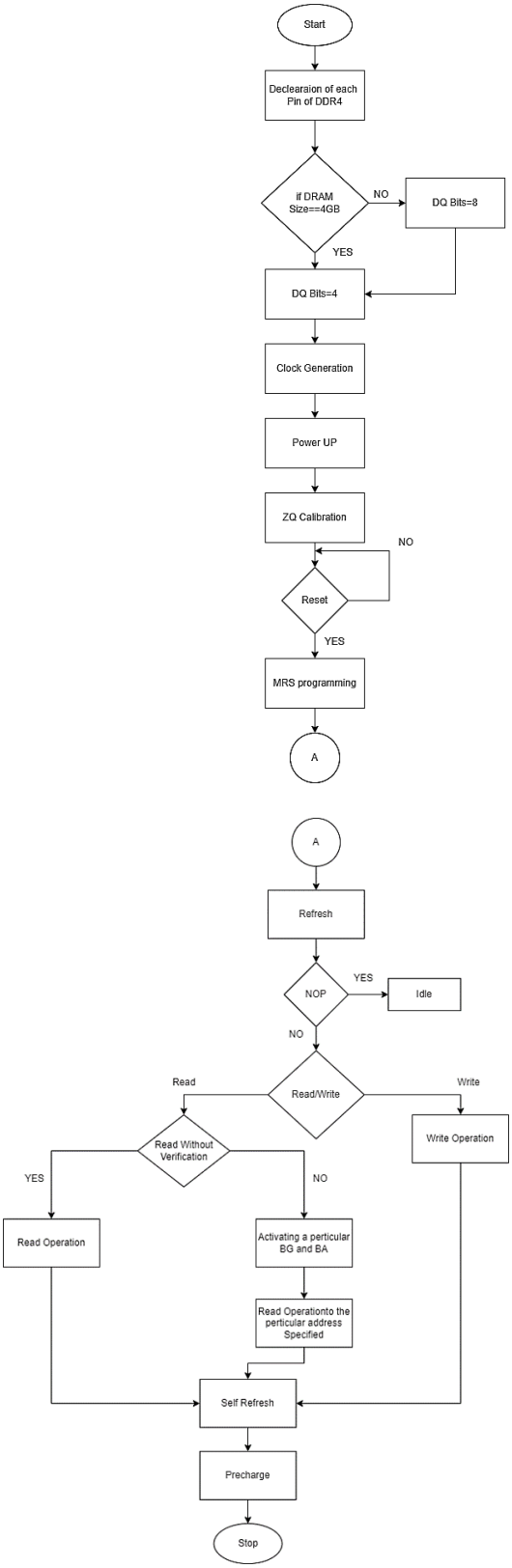

Fig-8: Flow Chart of DDR4 Memory Model.

7. RESULT

The DDR4 memory model is designed and successfully simulated using Modelsim and Questasim, where the different operations are simulated that is Idle, Reset, Refresh, MRS, Active, Write, Read, Pre-charge etc.

7.1. Idle

Initially DDR4 is in idle state with random Bank Group and Band Address selected with (RASn, CASn, WEn) = (1, 1, 1) with Reset active and Clock Enable Zero (CKE=0) as shown in Figure 9.

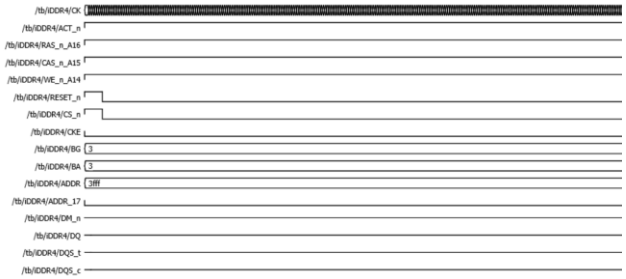

Fig-9: IDLE state (RASn=1, CASn=1 and WEn=1).

7.2. Reset

The DDR4 is reset with Chip select zero (CSn=0) and clock enable zero (CKE=0) as shown in Figure 10.

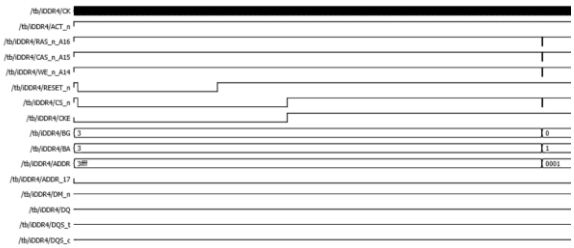

Fig-10: RESET Operation.

7.3. MRS Programming

Programming 7 MRS of DDR4 with (RASn, CASn, WEn) = (0, 0, 0) with 7 different addresses by selecting Bank Group and Bank Address. SDRAMs provide several features, functions and settings which can be programmed using the 7 Mode Registers. These registers can be programmed using the MRS command. The Mode Registers are set during initialization and thereafter they can be changed at any time during normal operation shown in Figure 11.

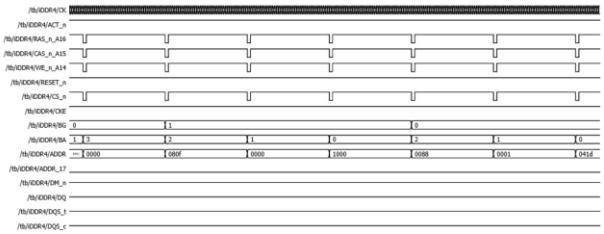

Fig-11: MRS Programming.

7.4. Refresh

To ensure data stored in the SDRAM is not lost, the memory controller must issue a REFRESH command for an average interval of tREFI. But before REFRESH is applied, all banks of the SDRAM must be pre-charged and idle for a minimum time of tRP (min). Once a REFRESH command is issued, there must be a delay of tRFC (min) before the next valid command is issued as shown in Figure 12.

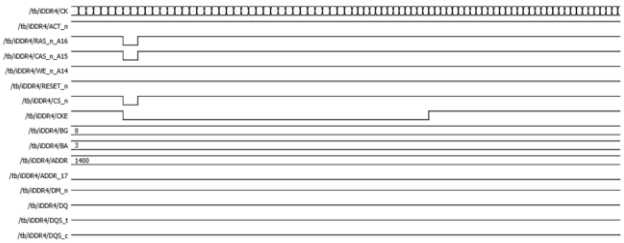

Fig-12: Refresh Operation (RASn=0, CASn=0 and WEn=1).

7.5. Write

Before writing on DDR4 memory model, Reset the memory and then provide write command by (RASn, CASn, WEn) = (1, 0, 0) with a minimum delay to write on DDR4 memory. Error occurs if minimum delay is not considered between two consecutive commands where delays are calculated and compared between DDR3 and DDR4 shown in Figure 13 and 14 respectively.

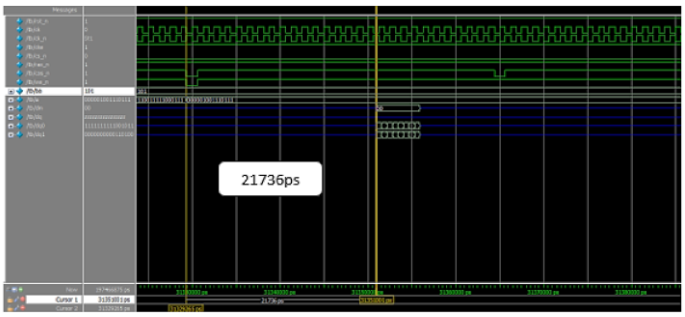

Fig-13: Delay before W rite Operation in DDR3.

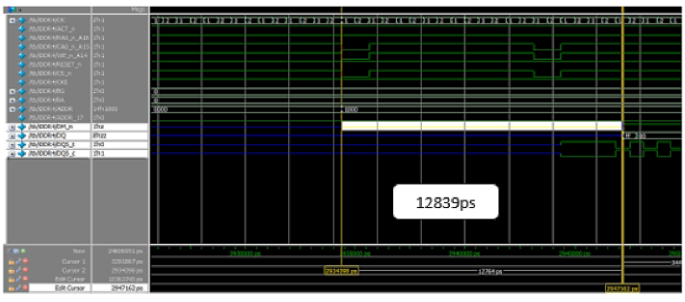

Fig-14: Delay before Write Operation in DDR4.

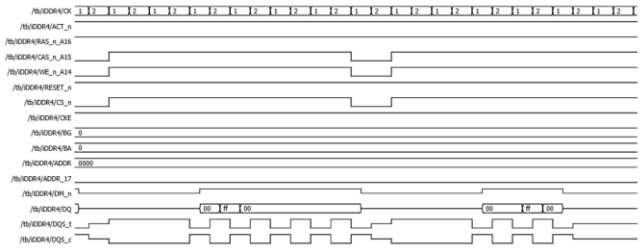

Fig-15: Writing a data to a Memory.

Data (00, ff, 00) on BG=0, BA=0 of (Address=0000). When DQS-t and DQS-c toggles the data is written on DDR4 memory shown in Figure 15.

7.6. Read

Read command by (RASn, CASn, WEn) = (1, 0, 1) with a minimum delay to read data from DDR4 memory where delay is calculated and compared between DDR3 and DDR4 as shown in Figure 16 and 17. Data stored in BG='0', BA='0', Address='0000' can be read from DDR4 memory error occurs if minimum delay is not considered between two consecutive commands as shown in Figure 18.

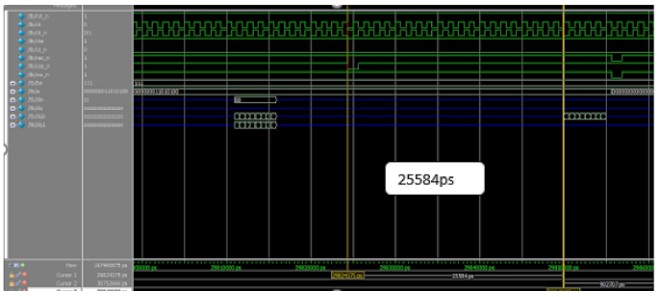

Fig-16: Delay between read command to data out in DDR3.

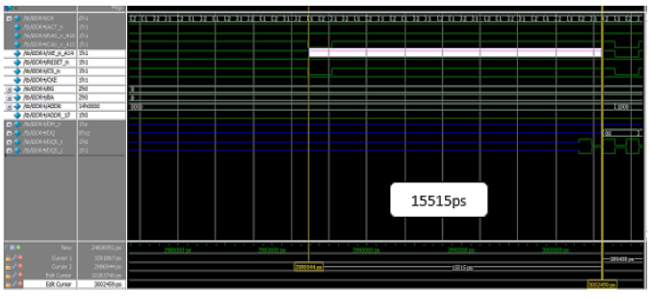

Fig-17: Delay between read command to dataout in DDR4.

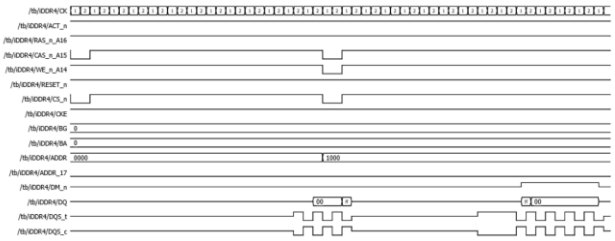

Fig-18: Reading a data from a Memory.

There should be some delay between any two consecutive operations in a Memory model, where the delay is calculated and compared between write and read operation in DDR3 and DDR4 which is shown in Figure 19 and 20 respectively. The delay between read and write operation in DDR3 and DDR4 are calculated as shown in Figure 21 and 22 respectively.

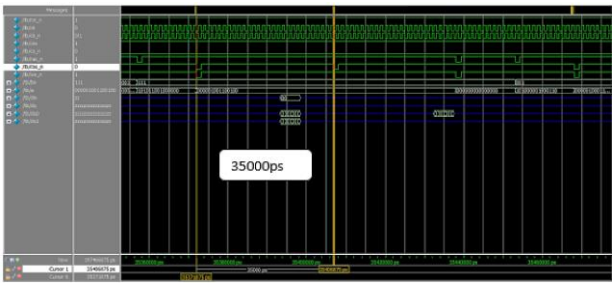

Fig-19: Minimum time between write and read operation in DDR3.

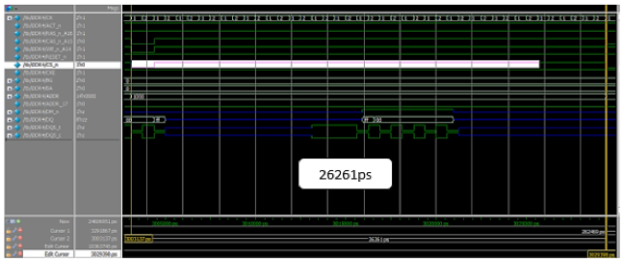

Fig-20: Minimum time between write and read operation in DDR4.

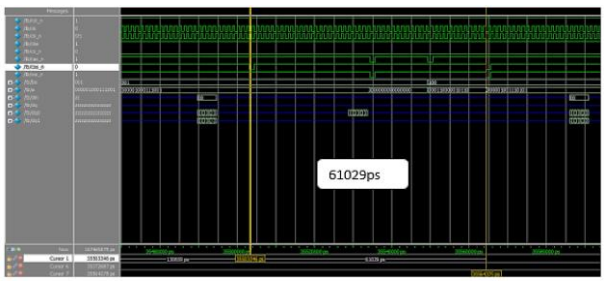

Fig-21: Minimum time between read and write operation in DDR3.

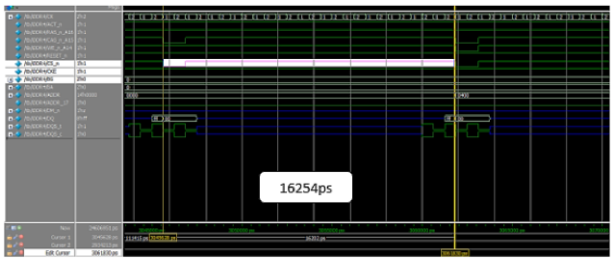

Fig-22: Minimum time between read and write operation in DDR4.

7.7. Pre-Charge

Pre-charge must be done if different BG need to be selected i.e., Pre-charge command by (RASn, CASn, WEn) = (0, 1, 0). Since data is stored in sense amplifier during write or read command, it must be sent to memory from sense amplifier during write command or read from memory to sense amplifier during read command as shown in Figure 23.

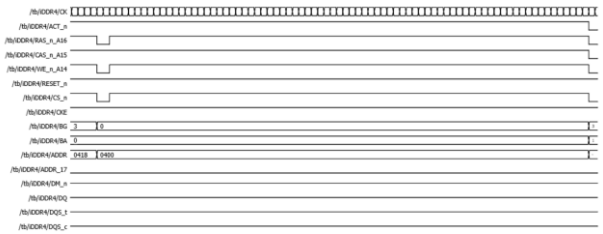

Fig-23: PRECHARGE Operation (RASn=0, CASn=1 and WEn=1).

8. Comparison of Data Access Time in DDR3 And DDR4

By considering the results obtained, the comparison of DDR3 and DDR4 is done by comparing the time delay between write/read command to the operation performed, and between any two operation that is either write to read or read to write which is shown in Table 4 and Total time taken to read and write the data to a memory address is calculated.

Table -4: Comparison of DDR3 and DDR4 During Read and Write Operation

Operations	DDR3(ps)	DDR4(ps)
Write command to data written	21736	12839
Read command to data read	25584	15515
Write and read	35000	26261
Read and write	61029	16254
Write operation	6250	4978
Read operation	7059	5643

By taking table into consideration, it can be said that the delay calculated in DDR4 is less than a delay occurred in DDR3. Hence, the performance of DDR4 memory model is enhanced in terms of data rate.

9. CONCLUSION

Modelling of DDR4 memory and advanced verification of DDR4 Subsystem is focused on designing and implementing the DDR4 memory according to DDR4 SDRAM JEDEC specifications, where the read and write operations of DDr4 is compared and tabulated with respect to DDR3. The designed DDR4 consumes lesser power and has greater data transfer rate compared to its predecessor i.e., DDR3, DDR2 and DDR. Its application ranges from low power mobile computing device to high density servers. Since there is an aggressive competition between different companies, the companies prefer to keep their research finding confidential, hence the upgradation of models becomes difficult. Therefore, the designed DDR4 model enables for easy upgradation.

REFERENCES

[1] Prajakta Chandilkar and Dr. Uday Wali, "Development of DDR2 SDRAM Module Interface Software Core", International Journal of Engineering Research and Application, pp.28-32, September 2017.

[2] Manikandan Sriram Mohan Dass, "Design and Verification of a Dual Port RAM Using UVM Methodology", IEEE Transactions on Memory management, volume 14, no.5, pp.1217-1243, June 2018.

[3] Md. Ashraful Islam, Md. Yeasin Arafath, Md. Jahid Hasan, "Design of DDR4 SDRAM Controller", 8th International Conference on Electrical and Computer Engineering, 20-22 December 2014.

[4] JEDEC Standard, "DDR3 SDRAM Specifications", JESD86-3B, JEDEC Solid State Technology Association, January 2009.

[5] JEDEC Standard, "DDR2 SDRAM Specifications", JESD79-2B, JEDEC Solid State Technology Association, January 2005.

[6] "URL: https://www.systemverilog.io/ddr4-basics".

[7] "URL:https://www.micron.com/-edia/client/global/documents/products/datasheet/dram/"