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PERFORMANCE ANALYSIS OF D-FLIP FLOP USING CMOS, GDI, DSTC TECHNIQUES

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Abstract - *This Paper explains the performance analysis of D-Flip Flop using three different techniques. They are D-Flip Flop using CMOS technology, Gate-Diffusion-Input(GDI) and DSTC technique. D flip-flop has been designed and layout simulated using 45nm technology in the first technique. The Gate diffusion technique is utilized directly following exploring different flip flop circuits since it is found to give the most minimal power delay when contrasted with other CMOS designs. The dynamic single-transistor-clocked (DSTC) flip-flop that experiences significant voltage drop at the result due to the capacitive coupling impact between the common node of the slave latch and the drifting result driving node of the master latch. The performance has been Analysed in terms of power dissipation and Propagation delay.*

Key Words: **D flip-flop, CMOS, Gate diffusion technique, DSTC, Power Estimation, Propagation Delay.**

1. INTRODUCTION

A bistable multivibrator, often known as a flip-flop or latch, is a circuit with two stable states that can be used to store state information. Signals provided to one or more control inputs can cause the circuit to change state, and it will have one or two outputs. In sequential logic, it is the most fundamental storage element. Flip-flops and latches are essential components of digital electronics systems found in computers, communications, and a variety of other applications.

The D flip- flop is extensively used. it is also referred to as a "data" or "delay" flip-flop. The D flip- flop captures the worth of the D- input at a particular portion of the clock cycle (alike because the rising edge of the clock). That captured value becomes the Q output. At further times, the output Q doesn't transform. The D flip- flop are often viewed as a memory cell, a zero- order hold, or a circuit.

D flip-flop is bistable circuits which give the result in reaction to a reference pulse. So the data put away in flip flops on the rising and falling edge of the clock signal is applied. as the inputs to other sequential circuits. Those flip-flops that store data on both the rising and falling of the clock signal is named as double edge triggered flip flops and those flip flops that store data any of the rising or falling edge are known single edge-triggered flip flops. So the latches and flip flops are the sequential circuits that pile 1 and 0 state called logic states. Latches works on level-triggered whereas flip flops work on edge-triggered.

In VLSI innovation the few past and years silicon CMOS innovation has turned into a prevailing creation process for moderately elite execution and cost-effective VLSI circuits. The VLSI innovation first semiconductor was created by William B. Hackey in 1947. [1] The incorporated circuits are created by the year 1960 and essentially there are four generations. The flip-flops termed so far in this module have been based on TTL technology, however many modern devices such as the 74HC and 74HCT series are CMOS ICs, which have deeply different internal structures. The flip flops in CMOS ICs persist on a different type of gate, called a 'Transmission Gate' or 'Bi-lateral Switch', which make it probable to build bi-stable flip-flops using less space within the IC, and have naiver structures than those used in TTL ICs.

Gate diffusion technique is termed as a new technique of low power digital combination of circuit design. This permits reduced power consumption and delayed propagation. [2] The GDI technique is more vital, because it involves less transistors compared to CMOS. GDI technique can be used to build fast, low power circuits using only few transistors and reduced power consumption, delay and area of the digital circuit. It preserves low complexity of logic design.

The dynamic single-transistor-clocked (DSTC) [3]flip-flop that experiences significant voltage drop at the result because of the capacitive coupling impact between the normal hub of the slave lock and the drifting result driving hub of the expert hook. This effect occurs at the rising edge of the clock and causes an extension in delay and short out power usage in the slave hook which could lead the extraordinary power use.

2. SIMULATOR

2.1 TANNER EDA TOOL

Tanner EDA is a set of tools for the design of integrated circuits. These tools permit you to enter schematics, accomplish SPICE simulations, do physical design (i.e., chip layout), and achieve design rule checks (DRC) and layout versus schematic (LVS) checks.

S-edit - a schematic capture tool
T-SPICE - the SPICE simulation appliance combined with S-edit
L-edit - the physical design tool

S-edit is a schematic access tool that is used to document circuits that can be focused forward into a layout of an integrated circuit. It also provides the capacity to achieve SPICE simulations of the circuits using a simulation engine called T-SPICE. T-SPICE can be setup and invoked from within S-edit. Today, in industry we utilize EDA tools to manufacture a netlist. It is easy to understand and debug. Also, for testability, it is easy if we have D flip-flops in scan chain.

3. SIMULATION METHODOLOGY

3.1 D FLIP-FLOP USING CMOS TECHNOLOGY

There are three bases of power dissipation in CMOS digital circuits. The first one is because of signal transistor, the following one is due to the leakage current and the final one is because of short circuit current which runs straight from the supply terminal to the ground. High leakage current plays the most significant part of contributor in the power dissipation of CMOS circuit as the threshold voltage, gate oxide thickness on the channel length is decreased.

The schematic design of D flip-flop is publicized in below figure 1 in which the 5 transistors where 3 NMOS and 2 PMOS are used.

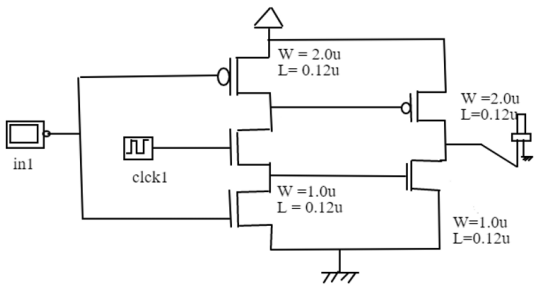

Fig 1: schematic design of D flip-flop

D flip-flop terms into a multi-threshold CMOS technology when 1 PMOS transistor and 1 NMOS transistor are linked to the circuit of D flip-flop so the clock is high and input is low because of the transistor M1 and M2 are “on” and M3 and M4 are “off” and the M5 transistor is “on” because of the output is low. The clock is high the input is high this transistor M1 is “off” and M2, M3, M4 transistors are on and the M5 transistor is “off” due to the output is high state i.e. High impudence state. In alternative way the clock is in low state due to the input is in low state and the M1 transistor is “on” and M2, M2, M3, M4, M5 transistors are “off” due to the output is low state.

After designing the early schematic in the Fig 1, we test the running of the circuit in Tanner EDA tool for supplementary analysis. So the circuit is designed in S-Edit software simulations arisen. The data stored is one, then the outputs will the similar.

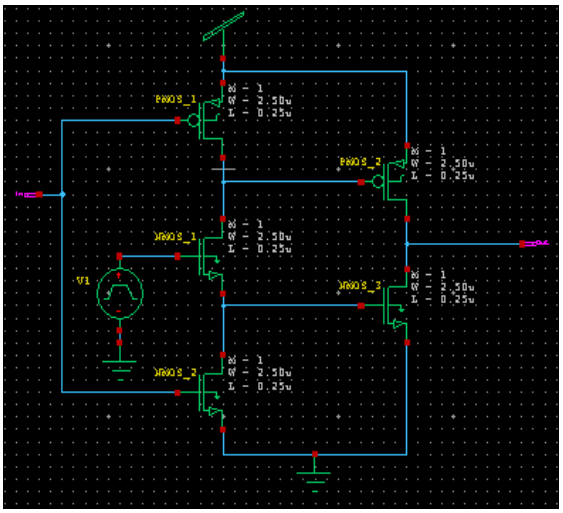

Fig 2: D Flip-Flop Using CMOS

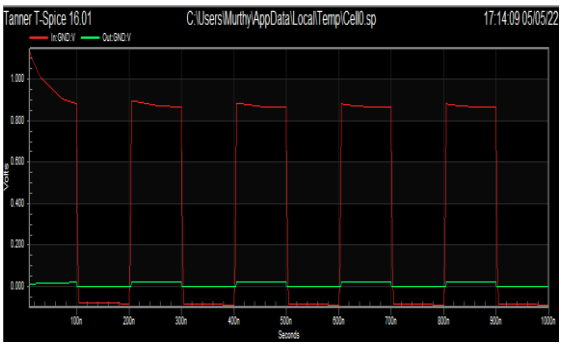

Fig 3: Output of D Flip-Flop Using CMOS

The D flip flop using CMOS Technology has a propagation delay 93.5197n/sec. The power consumption due to the width to length is 1.8856uW.

3.2 D FLIP-FLOP USING GDI TECHNIQUE

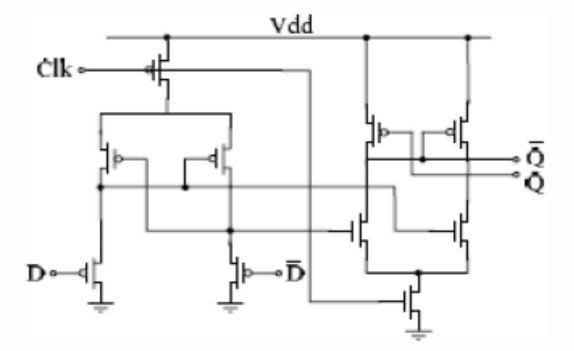

Fig 4: Schematic diagram of GDI

The main purpose of this effort is to minimize the power dissipation using GDI Technique. It is called Gate Diffusion Input Technique since the inputs are directly diffused hooked on to the gates of the transistors of N type and P type devices.

An innovative usage of a GDI DFF is give the idea in Fig 3. It depends on the Master-Slave link of two GDI D Latches. Every lock contains of four fundamental GDI cells, fetching about a basic eight-transistor structure. The circuit's segments can be subdivided into two principle classifications:

(a) Body doors - in control of the circuit's condition. These doors are organized by the CIk flag and create two option ways: one for straightforward condition of the lock (when the CIk is low and the signs are flourishing through PMOS transistors), and one more for the holding condition of the lock (when the Clk is high and inward values are saved up because of conduction of the NMOS transistors)

(b) Inverters (checked by x) - in control of synchronized the reciprocal estimations of the inward signs and the circuit yields. An extra vigorous part of inverters is buffering of the inward flags for swing rebuilding and enhanced driving capacities of the yields. This distribution of classes can aid understanding and improvement of circuit operation. The signal is transmitted through the dispersion hubs of the GDI cells in body entryways, as can be observed. It could cause a swing drop in VTH in yield signals. The inward inverters in their cradle part understand this problem. To get a small power delay item, the proposed circuit's execution can be improved by changing the transistor sizes (as a scope parameter in reenactment). This iterative technique includes a collection of independent size conformities:

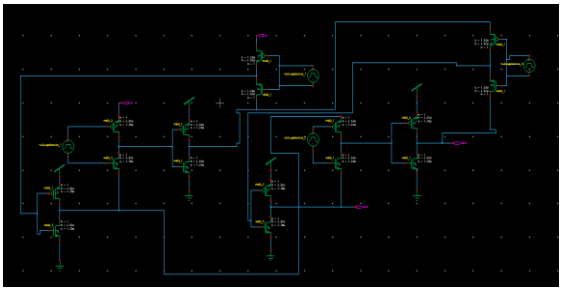

Fig 5: D Flip-Flop Using GDI

(a) First, the same scaling component is obtained for all of the circuit's transistors (body entryways and inverters).

(b) Second, while focusing on the negligible force delay item, iterative size advancements are connected separately to inverters and body entryways (for the most part via inverse moving of the scaling components around the "operation point" established in (a).

(c) For high load requirements, an additional streamlining on the Slave lock's inverter can be conducted independently.

The proposed DFF's somewhat conservative structure, which includes 18 transistors (plus an inverter for reciprocal D estimate), gives it a capable option for obtaining a blend of low range and good performance.

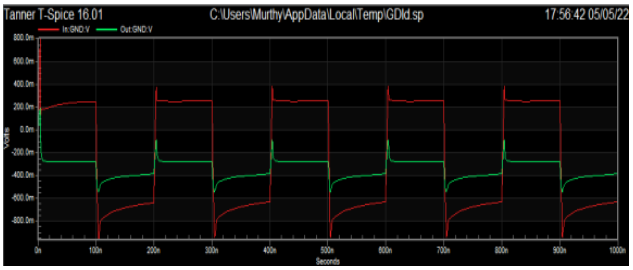

Fig 6: Output of D Flip-Flop Using GDI

The D flip flop using GDI Technology has a propagation delay 54.521n/sec. The power consumption due to the width to length is 1.1475uW.

After designing the early schematic in the Fig 3, we test the running of the circuit in Tanner EDA tool for supplementary analysis. So the circuit is designed in S-Edit software simulations arisen. The data stored is one, then the outputs will the similar.

3.3 D FLIP-FLOP USING DSTC TECHNIQUE

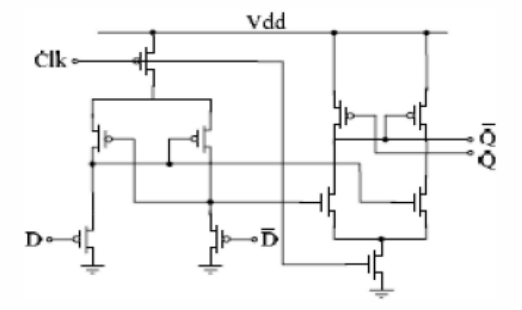

Fig 7: Schematic diagram of DSTC

Because of the topological contrasts among the current hooks, some of them required an altered test seat, i.e., a double information and/or a solitary yield. Be that as it may, these changes did not modify the examination's key methodology in view of the recreation conditions.

In DSTC circuit, we have utilized 12 transistors be that as it may, in GDI number of transistors utilized are 18 to manufacture D flip failure, so in DSTC lesser be the zone, lesser force scattering and lesser deferral as contrast with the GDI based D Flip Flop. Among all these circuits DSTC utilizes lesser transistors, lesser region, lesser postponement and lesser the force dispersal.

The fundamental purpose of the improvement is the minimization of the force delay item, given the constantly introduce trade-off in the middle of force and speed. The low power/high-speed performance of D flip-flops based on resistance is presented.

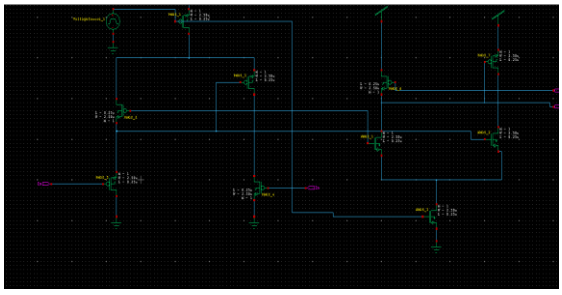

Fig 8: D Flip-Flop Using DSTC

Fig 7 represents the Schematic diagram of DSTC and Above Figure (fig 8) shows the implementation of fig 5 in tanner tool. the circuit is designed in S-Edit software simulations arisen.

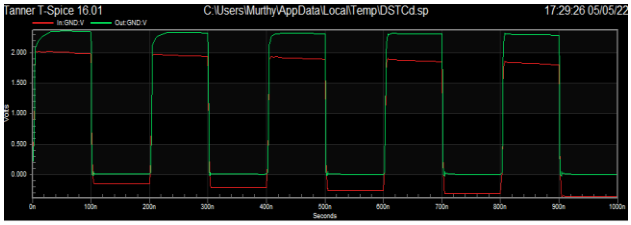

Fig 9: Output of D Flip-Flop Using DSTC

The D flip flop using DSTC Technology has a propagation delay 70.733n/sec. The power consumption due to the width to length is 1.4349uW.

4. RESULTS AND DISCUSSIONS

The layout simulations occur in T-Edit and W-Edit software. So the simulation results performed in the d flip flop layout consist of p diffusion and n diffusion and metal and contact cuts and substrate.

	Power Consumption(uW)	Propagation Delay(n/sec)
CMOS	1.8856	93.5197
GDI	1.1475	54.521
DSTC	1.4349	70.733

Table: Performance Results of D Flip flop

Propagation delay is obtained using delay formula and power is obtained using .Power (dot power) command in TANNER TOOL. The output signal wave forms of D Flip-Flop using CMOS, GDI and DSTC are shown in Fig 3, Fig 6 and Fig 9 respectively.

6. CONCLUSION

D Flip-Flop using CMOS, GDI and DSTC Techniques has been successfully designed and their performances is analyzed in terms of propagation delay and power estimation. An assortment of circuits has been actualized in 45 nm to contrast the proposed GDI structure and an organization of representative flip-flops, normally used for high execution outline. The simulation results are based on Tanner tool and it gives good lashing ability with good output signal and improved performance. DSTC uses fewer transistors, a smaller region, less postponement, and less force dispersal than the other circuits. Given the constant introduce tradeoff between force and speed, the main goal of the improvement is to minimize the force delay item. The resistance-based low-power/high-speed performance of D flip-flops is presented.

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