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Power quality issues and challenges in RES based System

Sunil Manjhi [1], Vikram Singh Sehmi [2]

[2] *M.Tech. Student, Dept. of Electrical Engineering, Shri Shankaracharya Group of Institutions, Bhilai CG, India*
[2] *M.Tech. Student, Dept. of Electrical Engineering, Bhilai Institute of Technology, Durg, CG, India*

Abstract– *To use renewable energy sources (RES) DC-AC conversion is an essential key, thus to perform this operation we use inverters. Inverters are famous in the renewable field. As we use AC in our house and many places, but the energy produced by the renewable source is DC, therefore we need an inverter. Multilevel Inverters (MLIs) have become a lot of and more well-liked in medium and highpower applications. this is often because of many inherent blessings of MLI over two-level inverters like high-quality output, smaller device ratings, and many other. [1]*

1. Introduction

Because of less dV/dt tension, less voltage stress across power semiconductor systems, small switching loss, and lower total harmonic distortion(THD) [1,2,3], MLI topologies have largely outplaced conventional two-level inverters. "***The Inverter is the electrical device that converts direct current(DC) to alternate current(AC)***".

Whereas multilevel inverters convert DC to AC in multiple voltage levels and improve waveform of the voltage (make close to the sinusoidal waveform and reduce THD). [4]

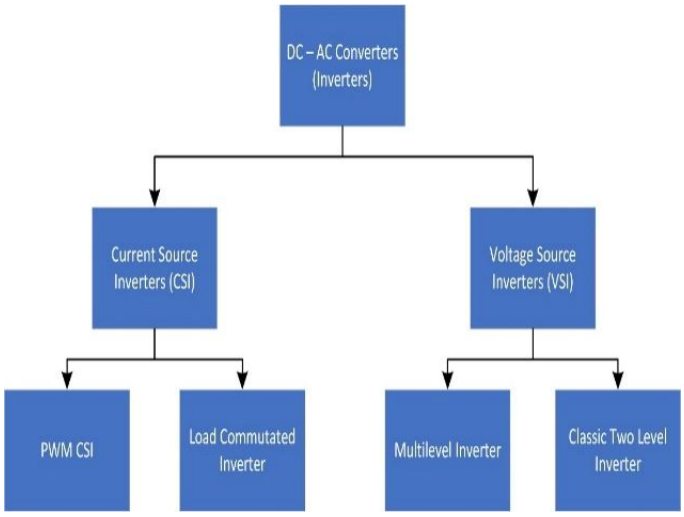


Fig 1. Classification of Inverters

Multilevel inverters are used in a variety of topologies. The distinction is in the switching system and the input voltage source for MLI. The following are the three most popular MLI topologies [5]:

1. Cascaded H-bridge(CHB) MLI
2. Diode-Clamped MLI
3. Flying-Capacitor MLI

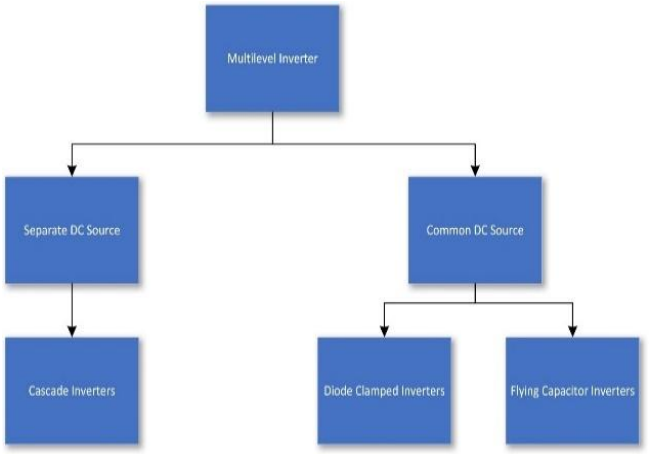


Fig 2. Types of inverters

1.1 Cascaded H bridge(CHB)

By connecting many H-bridge inverters in series, this inverter provides a sinusoidal output voltage. Each cell is given its own dc source, and each cell is connected in series with the others. Each voltage source with a switch configuration is known as a cell, and each cell is connected in series with each other, resulting in the output of CHB being the addition of the voltages given by each cell. For example, if the number of cells in any CHB configuration is N, the number of levels generated by N cell CHB will be 2N+1.

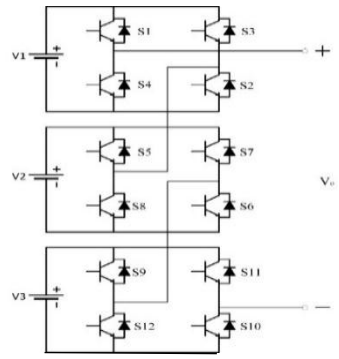


Fig 3 CHB Inverter

1.2 Diode Clamped multilevel inverters

Here diodes are used to control and limit the voltage stress on the control device or switches. Let V voltage around each capacitor and switch, so the number of sources = (X-1), 2(X-1) switching devices, and (X-1)*(X-2) diodes are required fór an X level inverter.

In a 5-level diode clamped multilevel:

X=5

Therefore:

Switch used = 2(X-1) = 08

Diode used = (X-1)*(X-2) = 12

Capacitor used = (X-1) = 04

A diodeclamped MLI is shown in Fig

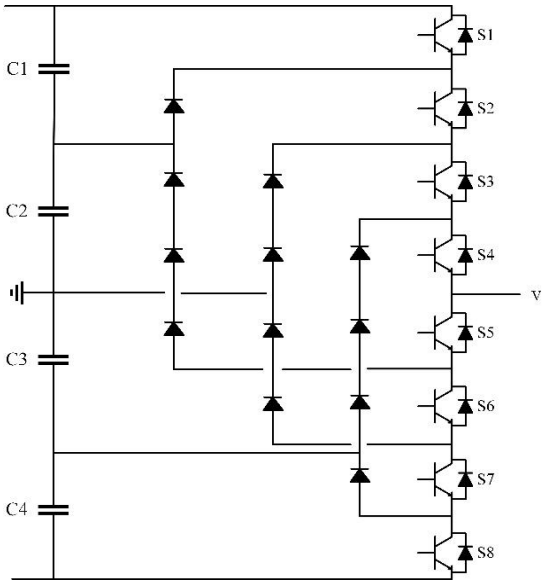


Fig 4 Diode-Clamped MLI

1.3 Flying-Capacitor multilevel inverters

Capacitors in this inverter limit the voltage of the power devices. The only difference between flying capacitor and diode clamped is that capacitors are employed to separate the input DC voltage. Let V represent the voltage in the vicinity of each switch and capacitor.[6]

X level flying capacitor inverter needs

Switch used: (2X – 2)

Capacitor used: (X – 1)

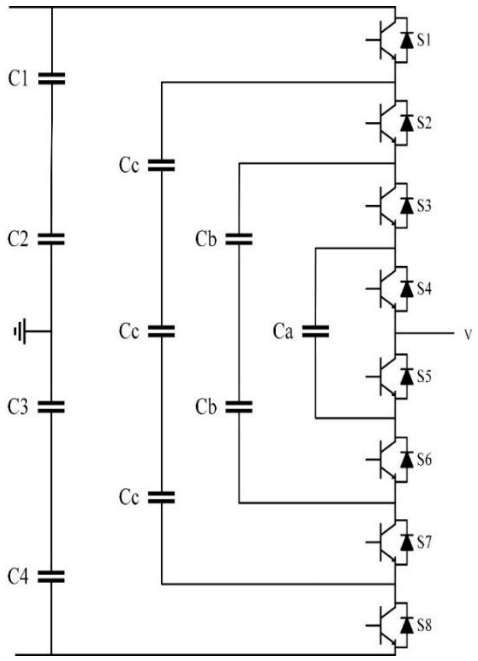


Fig 5 Flying-Capacitor MLI

2. REQUIREMENT OF FAULT TOLERANT MLI

The reliability of the topology of the MLI has the principal importance as the power semiconductor switches used in the architecture of the topology of the MLI are vulnerable. In light of the applications such as industrial manufacturing, the main operation is based upon induction motors and their inverter for process control.

To protect the inverter and induction machine(motor), traditional protection systems typically comprise of passive devices such as circuit breaker(CB), overload relays, and fuses. When a failure occurs[7], the protection devices separate the power sources from the multilayer inverter, resulting in the process being interrupted. Manufacturing equipment can cost thousands or hundreds of thousands of dollars per hr during a period of malfunction in power switches,

therefore fault-tolerant operation is required to ensure continuous operation and prevent damage to the inverter. [9]

In a recent survey over an amount of 200 products from 80 various companies, it is found that the power switches are responsible for 38% of failure in an inverter. The failure in power semiconductor switches can be classified into two types namely open circuit(OC) fault and short circuit(SC) fault. [7]

The SC failure causes the faulty switch to conduct even when it is turned off, potentially causing a shoot-through condition in the DC source or capacitor. This problem can be avoided by placing fuses in the conducting path, which will convert the fault back to an OC fault.

In the situation of an inverter with an induction motor, an OC fault will result in an unbalanced condition of load voltage and load current. If an induction motor is supplied with imbalanced voltage and current for an extended period of time, the induction motor may suffer critical damage due to high temperature. This could cause severe damage to the induction motor's winding and cause the entire system to shut down. As a result, an open circuit fault-tolerant multilevel inverter is required to ensure the inverter's proper operation while lowering the expense of additional protective devices.

The OC fault conditions on respective switches of each leg of Flying Capacitor or Diode Clamped causes the unbalancing of the capacitor voltage and ultimately results in the loss of a generation of voltage levels. This major issue will result in the failure of the healthy operation of both topologies. With this concern, the analysis is performed on open circuit fault on each switch of both topologies.

3. OPERATING PRINCIPLE OF THE PROPOSED MLI STRUCTURE

3.1 Analysis of OC Faults in 5-level MLI

A schematic diagram of the three-phase 5-level MLI structure is shown in Figure 1, and Phase-A of the proposed structure is shown in Figure 2. The proposed FT MLI consists of 8 unidirectional switches per phase and 5 redundant path switch, which includes 2 DC source voltage V1 and V2. The 14 switching state configurations of propose MLI are listed in Table 1.

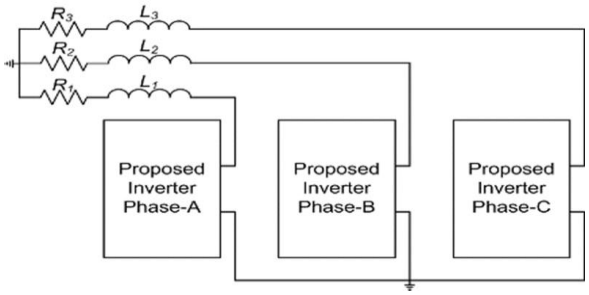


Fig 6. Schematic diagram of 3-ϕ 5-level MLI structure

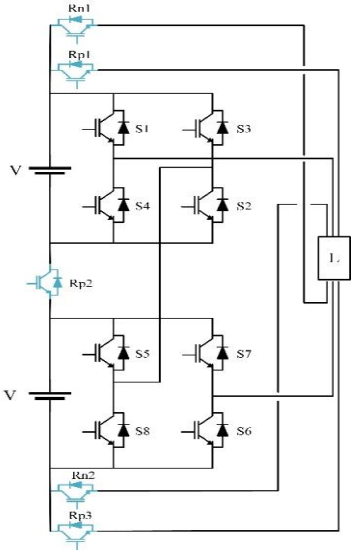


Fig 7. Phase-A of proposed 5-level MLI structure

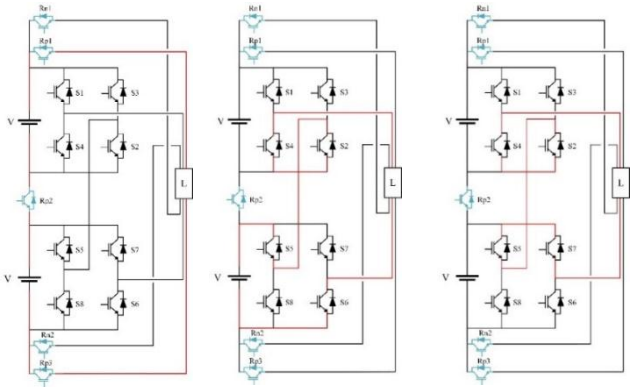
Table 1 Switching states of the studied 5-level MLI

0utput Voltage	Switching State	S1	S2	S3	S4	S5	S6	S7	S8
100V	State 1	ON	ON	OFF	OFF	ON	ON	OFF	OFF
50V	State 2	ON	ON	OFF	OFF	ON	OFF	ON	OFF
	State 3	ON	ON	OFF	OFF	OFF	ON	OFF	ON
	State 4	ON	OFF	ON	OFF	ON	ON	OFF	OFF
	State 5	OFF	ON	OFF	ON	ON	ON	OFF	OFF
0V	State 6	ON	OFF	ON	OFF	ON	OFF	ON	OFF
	State 7	OFF	ON	OFF	ON	OFF	ON	OFF	ON
	State 8	ON	ON	ON	OFF	OFF	ON	OFF	ON
	State 9	OFF	OFF	OFF	ON	ON	OFF	ON	OFF
-50V	State 10	OFF	OFF	ON	ON	ON	OFF	ON	OFF
	State 11	OFF	OFF	ON	ON	OFF	ON	OFF	ON
	State 12	ON	OFF	ON	OFF	OFF	OFF	ON	ON
	State 13	OFF	ON	OFF	ON	OFF	OFF	ON	ON
-100V	State 14	OFF	OFF	ON	ON	OFF	OFF	ON	ON

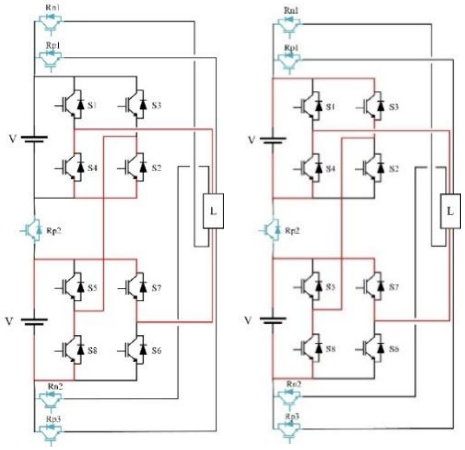
Table 2 is presented the lost switching states due to faults in the switches , fault in each switch effects the certain switching states and to compensate that we used the redundant switches with ensure the proper and affective working of FT-MLI during the Open Circuit fault , lost state is replaced by the different switching state of the redundant path shown in the table 3 , although stress on each switches increased due to the fault. Before fault, proposed topology work as a normal CHB inverter, until and unless there is fault, fault activate the redundant switch.

Under normal condition proposed topology works like a simple CHB and give output of level shifted five level output. But under faulty condition redundant path will be activated.

Below figures represents the working of the redundant path during the faulty condition.



State 1 State 2 State3



State 4 State 5

Fig 8. Current pathways and conducting pathways of proposed MLI for 5-level

For better understanding, Figure 9 represents a complete cycle of the 5-level o/p voltage and current waveform.

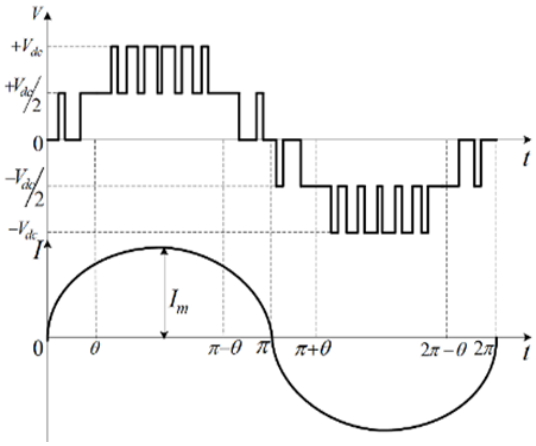


Fig 9. Complete cycle of the five-level output voltage and current waveform

.Table 2 Unavailable states in case of any single switch OC fault in MLI

Failed Switch	Effected Switching State	Output Voltage Level
S1	State 1,2,3,4,6,8,12	100V
S2	State 1,2,3,5,7,9,13	100V
S3	State 4,6,8,10,11,12,14	-100V
S4	State 5,7,9,10,11,13,14	-100V
S5	State 1,2,4,5,6,9,10	100V
S6	State 1,3,4,5,7,8,11	100V
S7	State 2,6,9,10,12,13,14	-100V
S8	State 3,7,8,11,12,13,14	-100V

Table 2 has shown that if any one of the switches encounters a failure then its effected states will be.

3.2 Design of Proposed Fault-Tolerant Inverter structure

The conventional topology requires the FT feature obstructing the output for faults in the switches. The authors have addressed the issue and some modifications in the existing single-phase MLI to incorporate inherent FT capability. An additional switch Rp1, Rp2, Rp3 and Rn1, Rn2 has been added to the conventional MLI, to obtain the modified single-phase (5-level) MLI with FT feature as shown in Figure 10.

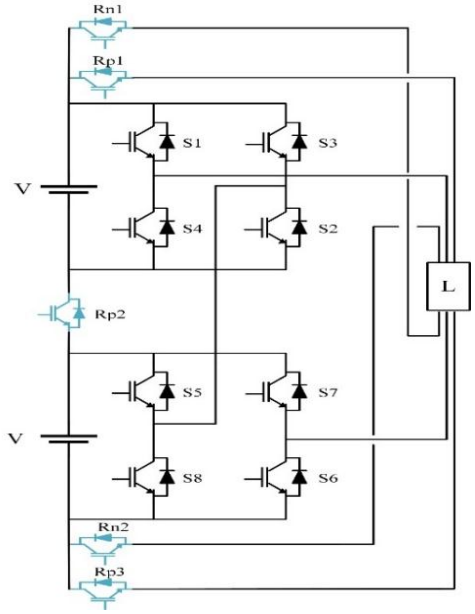


Fig 10. The Proposed FT- MLI structure

The valid switching status of the proposed FT MLI in case of single switch faulty conditions is presented in Table 3.[9]

Table 3 Available output voltage levels of the proposed FT MLI in case of single switch failure

Failed Switch	Active Switches	Output Voltage
S1	Rp1, Rp2, Rp3	100
S2	Rp1, Rp2, Rp3	100
S3	Rp2, Rn1, Rn2	100
S4	Rp2, Rn1, Rn2	100
S5	Rp1, Rp2, Rp3	100
S6	Rp1, Rp2, Rp3	100
S7	Rp2, Rn1, Rn2	100
S8	Rp2, Rn1, Rn2	100

4. SIMULATION RESULT

The simulation results of the proposed FT-MLI structure are discussed. To verify the structure under before-fault, faulty, and after-fault conditions, the proposed FT-MLI simulated using MATLAB-Simulink software. The current study employs a multicarrier phase opposition disposition PWM (POD-PWM) scheme with level shifting (LS-PWM). The gate signal pulses for triggering ON the power switching devices are generated using the LS-PWM modulation. [10]

In this multicarrier SPWM strategy, the 4 trianguler carrier signal are compare to the modulating sinusoidal reference signal for required gate pulses. The modulation index of 0.85 and the modulating wave frequency (fm) 50 Hz has been used for both simulation and experimentation. [11]

To examine the performance of the proposed FT-MLI structure is simulated using MATLAB-Simulink, which is also demonstrated experimentally through an R L load is taken with R = 20 ohm & L = 20 miliH. The simulation result and waveforms are show in the figure 11 & 12.

Components Rating

Input DC Supply Voltage Vs = 100V

Modulation index = 0.85

Switching frequency (fs) =2000 kHz

Load values R=20 Ω, L= 20 mH

Figure 11 and Figure 12 shows the output voltage and load current waveforms for OC fault in switches, respectively. The output waveform are maintained due to the redundant paths available for these faults

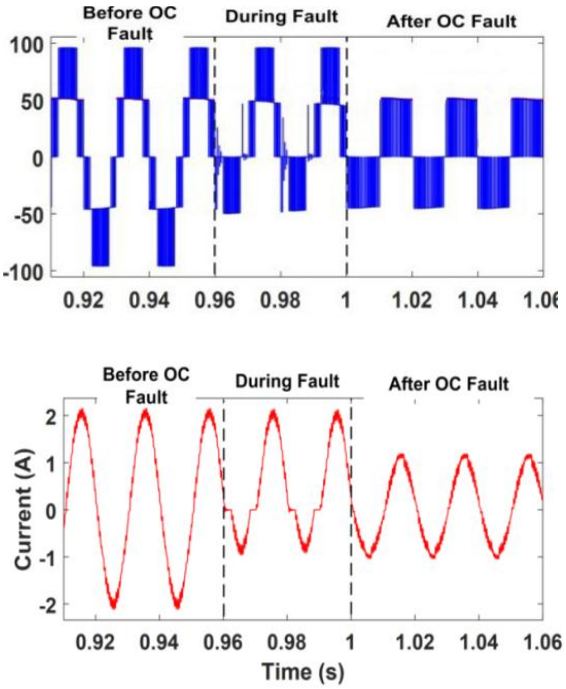


Fig 11. Simulation output voltage and load current waveform under fault

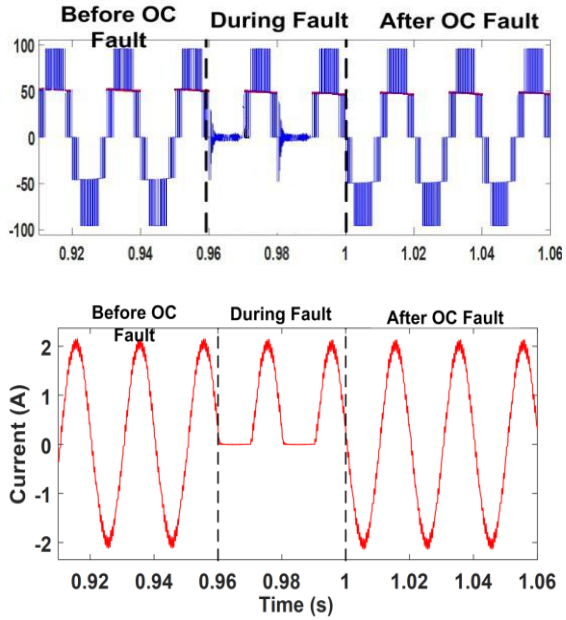
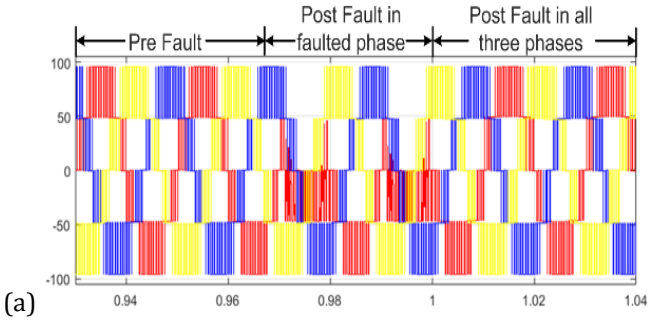
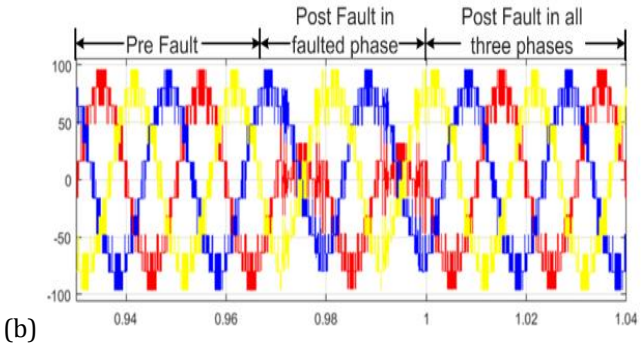


Fig 12. Simulation output voltage and load current waveform under fault

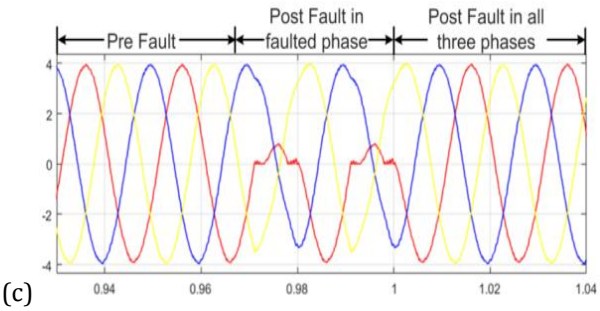
Similar results are obtained in the case of the three-phase structure of the proposed 5-level MLI. Figure 13 shows the phase voltages of the proposed FT- MLI structure for an open-circuit fault in the switch . Figure 13(b) and Figure 13(c) shows the line to line voltages and load current respectively.



(a)



(b)



(c)

Fig 13. Simulation output results for the proposed Fault Tolerant-MLI structure in switch S1 under Pre fault, faulty, post fault states (a) Line voltages, (b) Phase voltages, (c) Phase currents

Notably, the result clearly presented the proposed FT-MLI structure have the FT feature against OC faults that is any single switch failure. The output voltg is decreased from 5-level to 3-level & peak magnitude is halved. Simultaneously, a similar effect shows on the load current.

5. Conclusion

To prevent OC faults in switches with a small number of devices, this work provides a single-phase and three-phase FT-MLI structure with numerous redundant levels. In addition, the suggested FTMLI modulating technique has been tested in all modes of before-fault, faulty, and after-fault. According to a comparison, the presented FT-MLI structure contains fewer more devices than recently published fault-tolerant topology, but it ensure appropriate functioning when the system is faulty. Finally, various simulations show that the suggested MLI structure can operate in a fault-tolerant way.

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