International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0567
Volume: 09 Issue: 03 | Mar 2022 www.irjet.net p-ISSN: 2395-0072

Study on Processor used in Virtual Assistants: Google Assistant, Alexa, Siri Alexa

Nishita Patnaik[1], Kaustubh Agrawal[2]

[1] *School of Computer Science and Engineering, Vellore Institute of Technology, Vellore, India*
[2] *School of Computer Science and Engineering, Vellore Institute of Technology, Vellore, India*

Abstract - *The virtual assistant is a blessing for people in this developing and advancing world. It has given way by introducing technology to talk to a machine and even respond with an intelligent virtual assistant as people do with humans. This new technology has grabbed almost the entire world in many ways like smart phones, laptops, computers etc. The most prevalent Virtual assistants are Siri, Google Assistant and Alexa. Voice recognition, understanding of context and interaction with humans are the issues that have not been entirely solved through these IVAs. So we compared their architecture based on many characteristics from the analysis this research paper came up. According to those results, many things were covered by these assistants, but still, some improvements are going on in voice recognition, contextual understanding and hand free interaction. The main goal for this research paper is to get the idea and study the architecture of the popular Intelligent Virtual Assistant.*

Key Words: **Google Assistant, Siri, Processor, SSD, Hardware, voice recognition**

1. INTRODUCTION

Intelligent Virtual Assistant (IVA) is software that can perform a particular piece of work or services based on the question and command made. IVA is not only used for the term Intelligent Virtual Assistant. It also includes many things, for example, Conversational Agents, Virtual Personal Assistants, Personal Digital Assistants, Voice-Enabled Assistants or Voice Activated Personal Assistants, to give a few illustrations. IVAs join talk agrees to understand the foreign language, trade organisation, tongue age and speak to the association and respond to client's request and sales. Voice recognition IVAs like Siri, Google Assistant, and Amazon Alexa are recognised and has taken over all the devices in our daily use like cell phones, and continuously in homes (e.g., Amazon Echo and Google Home) and automobiles (e.g., Google Assistant blend with Hyundai). The market for IPAs is predicted 1,439.24 billion by 2024 at a CAGR of 11.91% during the forecast period. Organisations are rapidly using intelligent process automation as it gives them opportunities to automate their tasks and decisions, enhancing business processes and making IT operations work efficiently [1].

The specialised foundations that emancipate IVAs have developed quickly lately and have been the subject of broad research. People searched and found that people using IVAs are more restricted. We cannot agree that people are searching about IVAs and want advice for choosing IVAs. For example, even though people have this advanced feature of VA on mobile phones across the world, people like to use it frequently or not in the lowest. Current statistics showed that 98% of iPhone users had utilised Siri previously. However, just 30% used it routinely, and only 70% utilised it once in a while. IVAs technology is at the forefront of the AI- IoT revolution and edge computing.

VA built within the operating system has dedicated apps and home screen access to give basic information. Apple has their VA as Siri. They built it in iPhone, iPad, iPod Touch, Home Pod, Mac, Apple Watch, and Apple TV devices. Alexa works with Amazon's Resound, Fire, and Dash thing families, and many devices are running Android and iOS, including PDAs, savvy speakers and headphones, brilliant watches, and advanced cell devices including TVs, radios, lights, indoor controllers, and coolers. Google Assistant is like manner works with Android and Apple IOS platforms. IVAs are becoming popular at a reasonable rate, but still, people's curiosity is growing. For instance, I researched the ability to discuss interfaces (Siri can be used in locked screens) for more seasoned users. The writers focused on common commands like asking the climate conditions, writing notes, requesting headings, writing a quick message, asking an address, making a schedule, and knowing that the users were too positive to utilise discourse interfaces. At the same time, issues were recognised in connecting to the voice recognition with three assistants Siri, Google Assistant and Alexa. There were still some required modifications in voice speech recognition, and people are also finding the best in vocabulary understanding. The standard requirement is to feel unrestricted and can do his or her work in a relaxed manner. One typical example of human free inter linkage can be receiving a call then directly instructing VPs. The pattern is relative for different IVAs. People discuss their experience regarding using virtual assistance on smartphones [2]. Eventually, we accept improved user encounters, and selection is an achievable target across the board. This paper plans to help this goal.

2. OBJECTIVE

Presently the IVA's provide types of functionalities. However, these functionalities may differ from personal assistants and depend on the user and its usage. The main objective of this review is to validate the architecture used for a different personal assistant, which their creators usually exaggerate about. As these personal assistants are said to be fined, it becomes difficult for the individual to decide which one to pick, which one proves to be useful for itself. This paper tells us about the features of every personal assistant and how they work. And after the analysis of their features and find out the chances to combine various existing technologies with IVA's for making some unbelievable things which may turn the face of the existing technology.

3. LITERATURE REVIEW

The personal assistant is primarily AI-based has voice recognition, natural language understanding, and cloud computing to search the things on the internet and find it for you. Whenever the individual says "Ok Google", "Hey Alexa," or "Hey Siri", this is the wake-up call for these virtual assistants. They hear everything and interpret and come to work only when they wake up. They are passive listening devices that work only after the wake-up word. It starts to interpret the command you give through natural language processing; it is a subfield of AI, which is basically about the human interaction with machines, particularly how devices process a large amount of natural language data. It involves speech recognition, natural language understanding and natural language generation. When the commands are processed and reach the processor for further processing to searches through cloud computing and provide the best result, it converts the machine language to the human voice to provide us with the result. It all processes with the processor inbuilt inside it. The items that we took for analysis were Amazon Echo, Google Home and home pod these had processors marvel Armanda 1500 mini plus, Texas instrument and A8 processor. They all had the ARM, previously it was called Advanced RISC Machine, computer processors use reduced instruction set computing architecture (RISC), designed for a variety of settings Arm Holdings creates the architecture and licences it to others. create their devices that include one of those architectures—including systems-on-chips (SoC) and systems-on-modules (SoM) that incorporate memory, interfaces, radios, etc. Processors with RISC architecture typically require fewer transistors than those with a complex instruction set computing (CISC) architecture. The ARM architecture has developed in many years, where it provides execution and improving performance is their main focus. The ARM uses RISC architecture, as it has many beneficial features which the processors require, a large uniform array of processor registers which are located in CPU, these are also known as register files. These are usually implemented with SRAMs with multiple ports, a load or store architecture, where data-processing perform its operations on registers, not directly on memory, addressing modes. With all load or store addresses are fetched from register and instruction fields, consistent and fixed-length instruction fields are used to make instruction easier to decode. Furthermore, the ARM architecture provides controls on the Arithmetic Logic Unit (ALU) and shifter in data processing instructions to maximise the output of an ALU and a shifter, auto-increment and auto decrement addressing modes to make the best or most effective use of program loops, Load and Store Multiple instructions. We also added the *clock frequen*cy, which relates to the *rate* at which a processor's *clock* generator can create pulses that are needed to synchronise the actions of its components being used as an indication of the CPU's speed [3]. The pipeline comprises a whole task that has been broken out into smaller sub-tasks. In computers, the same basic logic applies, but rather than producing something physical on an assembly line, the workload itself gets broken down into smaller stages, called the pipeline. Processing in memory integrates a processor with RAM on a single chip. The result is also known as a PIM chip. Processing in memory is one way to remove the von Neumann bottleneck, a disadvantage caused by the discontinuation intrinsic in the basic computer architecture. In the basic model was known as the von Neumann architecture, programs and data are stored in memory; the processor and memory are kept at different locations and data travels between the two. Processor speeds have to boast remarkably in recent years. Memory up-gradation has mostly been in its memory capacity and its size. The ability to hold more data in comparatively lesser space and compromise with rates. The outcome was that the processor had spent a great amount of time waiting for data extracted from memory. As a result, the processor is circumscribed to the delivery rate at the bottleneck. In PIM chip fabrication, CMOS logic devices and memory cells are tightly packed; processor logic is directly attached to the memory stack and therefore, the combination of processing rate and memory relocation rate decreases latency and utilisation of power. We have also included GPIO in an Integrated circuit (IC). Some integrated circuits (ICs) include GPIOs as a major purpose, GPIOs as a convenient "accessory" to some other primary function. GPIOs are commonly seen in microcontroller ICs. GPIOs on a microcontroller may be the principal interface to external circuitry, depending on the application, or they may be simply one form of I/O utilised out of several, including such analogue I/O, serial communication and counter/timer [4]. A GPIO pin in some integrated circuits, particularly microcontrollers, may be capable of performing many duties. In such circumstances, it is frequently essential to set the pin to work as a GPIO (rather than its other purposes) in addition to specifying the GPIO's behaviour. Some microcontroller devices include internal signal management circuits that allows

GPIOs to be mapped to device pins programmatically. FPGAs enhance this capacity by providing programmable control of GPIO pin mapping, instantiation, and architecture. The most important thing for the processor to work fast is the memory; the register is the storage area inside the CPU. All data should be denoted in a register earlier, and it can be processed. The registers have the address of the memory block, which possesses the register where data is stored. These are Register Indirect Mode of Addressing There are several sorts of addressing modes in use.to increase the fetching and execution speed [5]. The memory hierarchy is kept in mind in the building of a processor as it is given in that more the size of memory larger the space it required and slower will be the processing and there will be a decrease in cost. L1 and L2 are levels of cache memory in a computer. We can see that in-memory hierarchy. The computer processor locates the data is required for its next level of cache memory, and therefore it decreases the time in contrast to having to search it in the main memory. Level 1 cache is the fastest and the costliest cache memory as it is already built within the chip with a zero-wait state interface. Level 2 cache is called secondary cache. Its working logic control is the same as Level 1 cache and implemented in SRAM [6]. It is slower than L1 but has a large memory. Dynamic random-access memory (DRAM) is a form of memory. memory used for data or program code for fast functioning. The processor can access any part of the DRAM is more preferred than having to proceed one at a time, and every time to process a new command, it has to start from the beginning. RAM is placed near a computer's processor, and it enables the data to be accessed quickly compared to the storage media such as hard disk drives and solid-state drives.

4. METHODOLOGY

We collected data about each of these virtual assistants and compared them based on their architecture and analysed each of them. The data was collected from various resources and the documentation of the developers. Many have not disclosed the parts and features used and how they work [7]. We took as many details as we could find everywhere.

Table -1: Devices used to access each Personal Assistant

VIRTUAL ASSISTANT	DEVICES
Google Assistant	Google Home
Alexa	Echo Dot
Siri	Apple TV and Remote

5. RESULT

5.1 Evaluation

This task aimed to compare the devices based on various parameters to learn and analyse each parameter and their working and the type of architecture required for virtual assistants. We analysed as many parameters as possible. We analysed features like the type of processor they have the microphone they used for listening commands, speakers for translating machine language to natural language understanding. Led drivers to show responses of the command or to show they have been activated by our wake-up call and the features of processor they used to like the clock rate, byte-addressable and GPIOs etc [8].

Table -2: Classification of Personal Assistant on different parameters

FEATURES	GOOGLE HOME (GOOGLE ASSISTANT)	ECHO DOT(ALEXA)	HOMEPOD (SIRI)
PROCESSOR	Marvell 88DE3006 Armada 1500 Mini Plus	Texas Instruments DM3725CUS100 Digital Media Processor	Apple A8 Processor
FLASH MEMORY	256 MB	4GB	16 GB
RAM	512MB	256MB	1 GB
SPEAKERS	High excursion speaker with 2” driver + dual 2” passive radiators	2.5” downward-firing woofer and 0.6” tweeter	International Rectifier PowlRaudio 98-0431 audio amplifier
MICROPHONES	Two InvenSense INMP621 MEMS microphones	S1053 0090 V6 Microphone (x7)	Apple/Dialog 338S00100-AZ PMIC
LED DRIVER	Two NXP PCA9956BTW LED drivers	Texas Instruments LP55231 Programmable 9-Output LED Driver (x4)	Texas Instruments TLC 5971 LED Driver
MICROPROCESSOR	ARM Cortex A7	ARM® Cortex-A8 Core	ARMv8-A

CLOCK RATE	1.2GHZ	1GHz	1.3GHZ
L1 cache	32-bytes. (2-way set-associative instruction) 64-bytes. (4-way set-associative)	32K-Byte (Direct Mapped) • 80K-Byte (2-Way Set-Associative)	64KB (2 way-set associative) 64KB (2 way-set-associative)
L2 cache	L2 cache size of 128KB, 256KB, 512KB, and 1MB. (8-way set-associative cache structure.)	64K-Byte (4-Way Set-Associative) • 32K-Byte L2 Shared SRAM and 16K-Byte L2 ROM	1MB (8 way-set-associative)
L3 cache	-	-	4MB(SRAM)
BYTE ADDRESSABLE	32 bits	64 bits	64 bits
GENERAL-PURPOSE INPUT/OUTPUTS	Up to 176 I/O ports with interrupt capability – Up to 8 secure I/Os – Up to 6 Wake-up, 3 tampers, 1 active tamper	Up to 188 General-Purpose I/O (GPIO) Pins (Multiplexed with Other Device Functions)	UP TO 200 GPIO
MEMORY CONTROLLER	8-,16-bit data bus width	16-bit Wide Multiplexed Address/Data bus	it width bus

5.2 Analysis of Result

We found that every processor uses the ARM cortex for their microprocessor on analysing. It shows that the architecture ARM processors' architectural is more advanced and has allowed devices to work efficiently with very little power. Execution of small size, high performance, and significantly less energy usage has to remain the main focus in forming the ARM architecture [9]. To maximise the amount of data passing through the system, conditional execution of complete instructions increases the implementation to the full extent. ARM has 31 general-purpose registers of 32 bit. At once, 16 registers are visible. The other leftover registers are used to accelerate deviation processing. All the registers prescribed in ARM instructions can fetch the address of any 16 visible registers. The entire deprived code utilises the central bank of 16 registers [10].

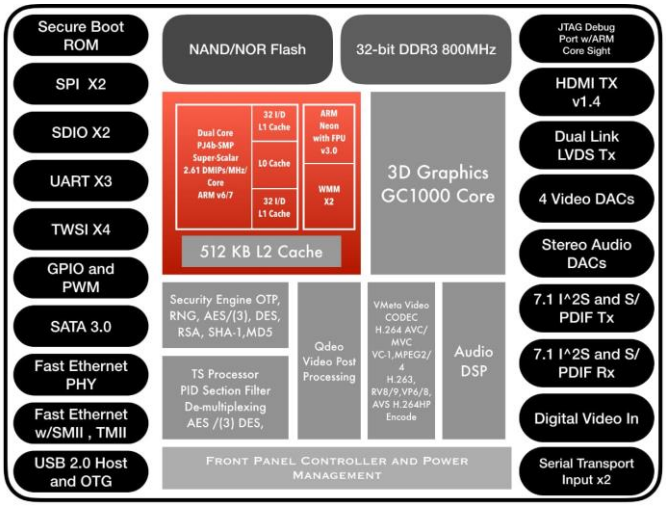

Fig-1: The architecture of Marvell ARMADA 1500(88DE3100)

These RISC architectures have evolved in these years and allow ARM processors to achieve a high performance and keep the small code size and utilise meagre power and small processor area [11]. The Marvell ARMADA 1500 (88DE3100) secure media processor system on chip (SoC) has the features of high-definition (HD) with the latest multi-format video and audio decoder. It has two processors, ARMv7, well suited with PJ4B processors with symmetric multi-processing (SMP) and a large L2 cache and can be attached and used within and not necessarily be an integral part of it [12]. It decodes two full HD streams and multi-channel audio and 2D and 3D graphics pipelines that allow rich and highly complex User Interfaces (UI) with a high potential gaming experience.

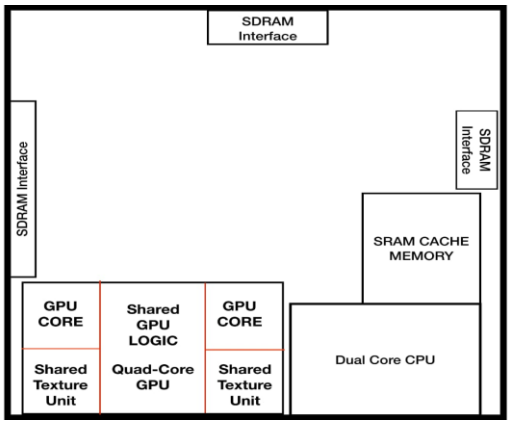

Fig-2: The architecture of the Apple A8 processor

The A8 CPU has a per-core and memory unit as L1 cache of 64 KB both for instructions and data set, an L2 cache of 1 MB used by CPU cores, and a 4 MB L3 cache that is used for the entire SoC As its previous version had a 6 decode, 6 issue, 9 wide, out of order design [13]. The processor is

dual-core, and it has a clock rate of 1.4 GHz. It has developed the 2nd generation Typhoon architecture by enhancing the capability of previous versions of Cyclone core to increase performance gain per Hz. The A8 graphics processing unit (GPU) is a PowerVR Series 6XT. However, Apple has designed custom shadier cores features[14].

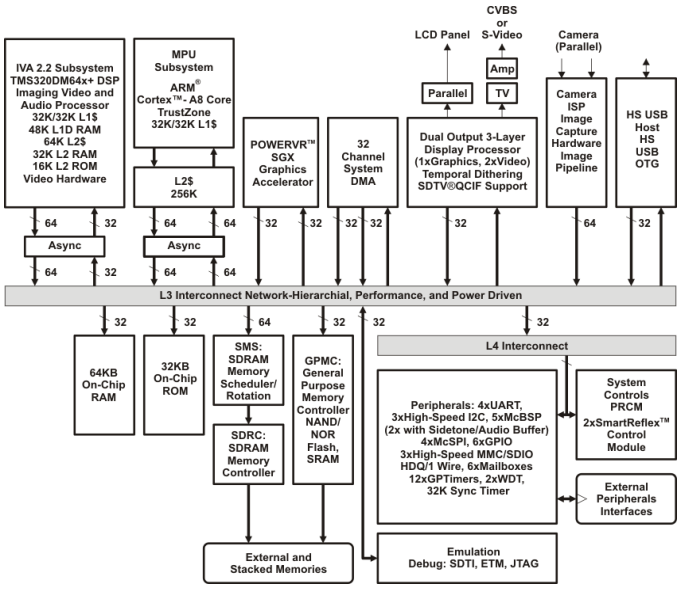

Fig-3: The architecture of Texas Instruments (DM3725CUS100) Digital Media Processor

6. DISCUSSION AND FUTURE

Virtual assistants have become increasingly common in the workplace. our daily routine. As life without our smartphones becomes impossible in today's world, many of them have virtual assistant Siri on iPhone or Google Assistant on Android phones and Alexa as a home speaker. All of the devices we took were the least featured device to focus only on the IVAs were rated based on the things that had inside the device as we know VA are the software implemented on the processor [15]. It shows a comparison between the three processors. All users select the best virtual assistants. We also have to include that recognising the voice required depends on various factors such as environment, voice modulation, frequency, etc. We have to keep involving the natural language understanding. The important thing is that people's voices vary, and they speak in different ways and different languages. All the IVAs are evolving, they all are interconnected to machine learning, and artificial intelligence is trying to give brains to machines. On surveying the three IVAs, Google assistant answered 59.80% of the question. Siri answered only 45%. Alexa loss only answered 7.91%.

According to the survey, IVAs have a poor retention rate, with only 25% of the frequent daily life users. Their retention indeed depends on the more significant memory they have [16]. The more it becomes a problem for processors to process and become slower. Alexa, Google Assistant, Siri will be betterment in the coming years. Likely, one day they will meet our expectations [17]. IVA's are indeed beneficial for the future where a human cannot reach, they will reach and help in various ways. There is research going on everywhere for enhancement in all tested devices. New studies are being conducted, and also, indeed, these devices with various machine learning technologies and algorithms will help us change the face of the technology [18].

REFERENCES

[1] Chung, H., & Lee, S. (2018). Intelligent virtual assistant knows your life. *arXiv preprint arXiv:1803.00466*.

[2] Tulshan, A. S., & Dhage, S. N. (2018, September). Survey on virtual assistant: Google assistant, siri, cortana, alexa. In *International symposium on signal processing and intelligent recognition systems* (pp. 190-201). Springer, Singapore.

[3] Bhonsle, V. S., Thota, S., & Thota, S. (2022). AKIRA—A Voice Based Virtual Assistant with Authentication. In *Communication and Control for Robotic Systems* (pp. 177-191). Springer, Singapore.

[4] Ryzhyk, L. (2006). The ARM Architecture. *Chicago University, Illinois, EUA*.

[5] POR, P. Arm® Cortex®-A7 800 MHz+ Cortex®-M4 MPU, TFT, 35 comm. interfaces, 25 timers, adv. analog.

[6] Karhe, R. R., & Sonawane, G. P. Digital Video Monitoring System Based On ARM Cortex A7.

[7] Bennett, G., Kaczmarek, S., & Lees, B. (2015). Getting Started with the New Apple TV. In *Developing for Apple TV using tvOS and Swift* (pp. 1-8). Apress, Berkeley, CA.

[8] Young, T., Hazarika, D., Poria, S., & Cambria, E. (2018). Recent trends in deep learning based natural language processing. ieee Computational intelligenCe magazine, 13(3), 55-75.

[9] Otter, D. W., Medina, J. R., & Kalita, J. K. (2020). A survey of the usages of deep learning for natural language processing. IEEE Transactions on Neural Networks and Learning Systems, 32(2), 604-624.

[10] Ahn, J., Yoo, S., Mutlu, O., & Choi, K. (2015, June). PIM-enabled instructions: A low-overhead, locality-aware processing-in-memory architecture. In 2015 ACM/IEEE 42nd Annual International Symposium on Computer Architecture (ISCA) (pp. 336-348). IEEE.

[11] Hestness, J., Keckler, S. W., & Wood, D. A. (2014, October). A comparative analysis of microarchitecture effects on CPU and GPU memory system behavior. In *2014 IEEE International Symposium on Workload Characterization (IISWC)* (pp. 150-160). IEEE.

[12] Earnshaw, R. (2003). Procedure call standard for the ARM architecture. *ARM Limited, October*.

[13] Foxx, C. (2017). Apple reveals HomePod smart speaker. BBC News, Jun, 5, 6.

[14] Betters, E., & Grabham, D. (2018). Apple HomePod vs Google Home vs Amazon Echo: What's the difference. Pocket-Lint. Available at: www. pocket-lint. com/speakers/buyers-guides/139063-apple-homepod-vs-google-home-vsamazon-echo-what-s-the-difference (accessed 20 July 2018).

[15] Berger, A. A. (2018). The Amazon Echo. In Perspectives on Everyday Life (pp. 79-82). Palgrave Pivot, Cham.

[16] Giese, D., & Noubir, G. (2021, June). Amazon echo dot or the reverberating secrets of IoT devices. In *Proceedings of the 14th ACM Conference on Security and Privacy in Wireless and Mobile Networks* (pp. 13-24).

[17] Kepuska, V., & Bohouta, G. (2018, January). Next-generation of virtual personal assistants (microsoft cortana, apple siri, amazon alexa and google home). In *2018 IEEE 8th annual computing and communication workshop and conference (CCWC)* (pp. 99-103). IEEE.

[18] Hoy, M. B. (2018). Alexa, Siri, Cortana, and more: an introduction to voice assistants. *Medical reference services quarterly*, *37*(1), 81-88.