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Design and Implementation of Different types of Carry skip adder

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Abstract - In many computer systems, adders are the basic building blocks. The Carry-Skip Adder (CSA) is one of the fastest and most space-effective adder topologies. The existing CSA structure available in the literature is high because of its conventional design. In the proposed adder, compound gates are employed. Performance improvement is observed due to the presence of AOI and OAI logic. 8-bit CSA is designed and analyzed using both Xilinx ISE 14.2 Vivado Design Suite and Cadence, to analyze area and power. The design is implemented on a Zed board using Verilog HDL programming.

***Key Words*: Carry Skip Adder, Common Boolean Logic (CBL), high performance.**

1. INTRODUCTION

The carry skip adder is an efficient adder when it comes to space and energy usage. Adders are an essential part of arithmetic and logical units (ALUs). It accelerates addition by spreading a carry bit throughout the entire adder. Because of its excellent computing efficiency and minimal delay, CSKA attracts a lot of interest. Additionally, due to the minimal number of transistors, the carry skip adder has relatively little wiring and a straightforward layout[1]. This paper goes into more information about the work that has been done to increase the speed and power of CSKA. Better speeds must be achieved with the least amount of power dissipation, which is difficult for VLSI designers to achieve. The analysis of an adder utilizing a traditional carry skip adder is covered and explains the design logic for CBL adders are the fastest adders with area overhead area, which are also efficient in terms of area and power[2][3].

Lowering the supply voltage is a very efficient way to reduce a circuit's power consumption. Additionally, power consumption is substantially decreased because the switching energy heavily depends on voltage. [1] We currently have a large number of adders with varying delays and power losses. For instance, carry skip adders (CSKA), parallel prefix adders, ripple carry adders (RCA), and carry increment adders (CIA) [2] When it comes to space and energy utilization, the carry skip adder is an expert adder. It accelerates addition by spreading a carry bit throughout the entire adder. Although CSKA has a substantially shorter delay than RCA[3]. Additionally, the carry skip adder has relatively short wiring lengths and a straightforward design due to its low transistor count By breaking the adder into varying-sized blocks that balance the latency of inputs to the carry chain, the delay and power dissipation of the carry skip adder are decreased[5]. It is important to note that the proposed adder's delay improvement was accomplished without increasing power consumption or circuit complexity[6]. In order to increase speed performance, this paper only offers an optimization strategy for the scenario of constant block size[7]. A 16-bit carry skip adder has been developed, which is an improvement of the conventional ripple carry adder created via reversible logic[8]. The suggested circuit significantly reduces the chip size and the number of transistors[9]. The size of the transistors, parasitic capacitance, and latency in the critical path are described in this study as the design's speed-limiting factors[10]. Binary Coded Decimal (BCD) adder and Carry Skip BCD adder implementations for reversible logic are presented in this work[11]. These devices should use high-speed, low-power, and area-efficient circuits to accomplish the calculations[12]. The technique put forward has been proven effective by using it in the design of more than 50 adders with different delays for the logic gates employed and bit counts[13]. This paper presents a novel technique for finding the best distribution with no limit on the number of skip levels and demonstrate a full-static carry-skip adder with minimal power dissipation and great operation efficiency[14].

2.LITERATURE SURVEY

Small technological devices are now a necessary component of daily life. Devices with extremely high speeds and low power consumption are in high demand. The main challenge in creating high-speed arithmetic units is minimizing the amount of time needed for carrying to propagate through adders. For this issue, numerous solutions have been put forth. One of them uses a carry skip adder rather than any other adder because it is a fundamental part of every processor.

[1] Carry Skip Adder Using Blocks of Full Adders
Lehman et al. made the initial suggestion for the carry skip adder (CSKA) (1961). Its speed was discovered to be higher than the typical RCA. To minimize latencies in carrying skip adders, some programs have been implemented. The

language used to present algorithms is T. Blocks of full adders are merged to form a CSKA, which influences the CSKA's overall speed (Chan, Schlag, Thompson, and Oklobdzija,992). The study sets up CSKA and CSLA adders to achieve the least amount of latency.

[2] Carry Skip Adder using Concatenation and Incrementation Schemes

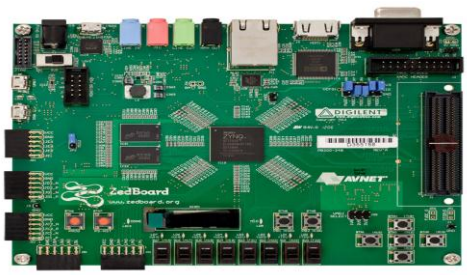
M. Bahadori et al(Bahadori, Kamal, Afzali, Pedram, 2016) representation of a CMOS CSKA structure shows that it uses less energy and operates more quickly than a traditional one. Carry the skip logic is accomplished by substituting compound gates known as OR-AND-invert (OAI) and AND-OR-invert (AOI) for multiplexers. Utilizing incrementation and concatenation methods significantly improves speed.

[3] Carry Skip Adder using Efficient Full Adders

The most crucial factors that need to be taken into account in the majority of VLSI applications are latency, power, and area. A quick adder can be used to do this. Comparing different adders, it was shown that carry-skip adders drain more power and take up more space than RCA adders but have shorter delays. In the study by S.K.Shirakol et al., Thus, the use of efficient full adders allows for the solution of the power and area problem. (2014) Parvati, Shirakol, Kulkami, and Akash.

3. ZED BOARD

The Zed Board from Xilinx is a cheap development board that includes everything required to create designs based on Linux, Android, Windows, or other OS/RTOS. Users can additionally access the processing system and programmable logic I/Os via a number of expansion connectors. Utilize the closely integrated ARM processor system and 7 series programmable logic of the Zynq-7000 SoC to build creative and effective designs using the Zed Board.



4. EXISTING ADDERS

Traditionally, Carry skip-adding is carried out in stages. An RCA block, a multiplexer, and a carry prediction unit make up each stage. RCA is used to calculate each stage's sum. It creates the sum using the input bits for the two numbers A and B. The 4-bit RCA block is used in the designed model. The carry prediction unit will output one when all of the bits of the relevant stage are in propagation condition.

CSKA divides words that are added to the blocks. Every block has an RCA that generates the carry and sum. However, CSKA shortens the wait time by excluding the group of Full stage adders from the carry computations.

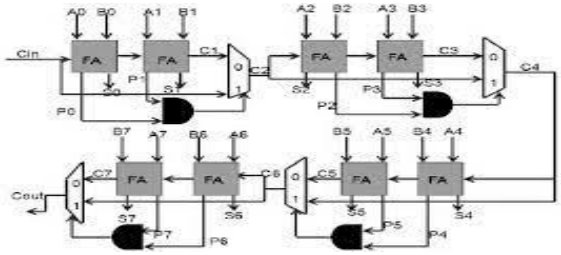


Figure -1: Carry skip-adder logic diagram

Figure 1 illustrates how multiplexers and AND gates are used to implement CSKA's skip operation. The RCA block and the skip logic make up each stage in this scheme.

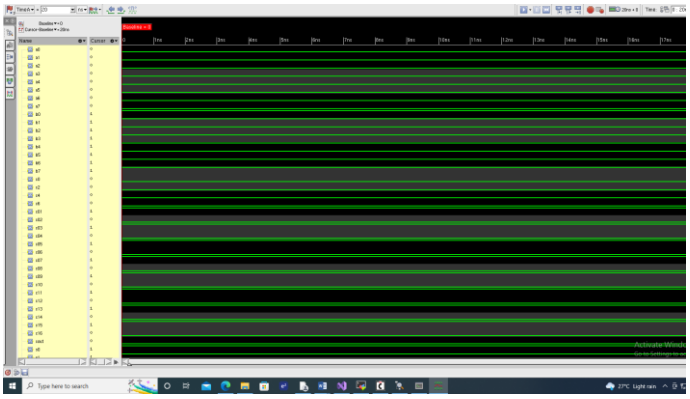


Figure -2 : Simulated output for carry skip adder

In the figure-2 the simulated output for conventional carry skip is produced using Verilog in cadence.

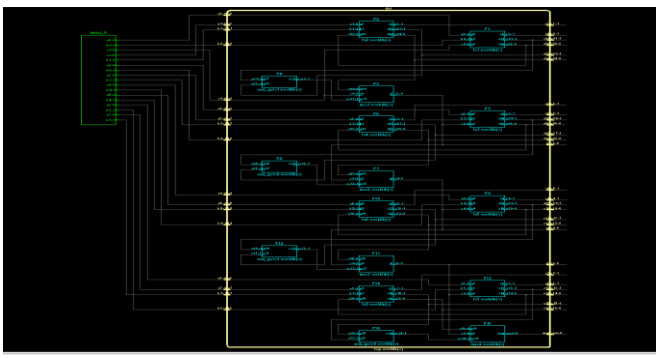


Figure-3: Schematic output of conventional carry skip adder

5. PROPOSED TECHNIQUE

An area-efficient CSLA is suggested by sharing the Common Boolean Logic (CBL) term in order to eliminate the redundant adder cells in the standard CSLA. The output of the summation signal is a carry-in signal with logic "0" and is an inverse signal of itself with logic "1," according to the analysis of the truth table of the single-bit full adder. To create the summation pair, which is what Common Boolean Logic calls the summation pair, we only need to design one XOR gate and one INV gate. In order to construct the carry pair, we also need to implement one OR gate and one AND gate. This allows the summation and carries circuits to remain parallel.

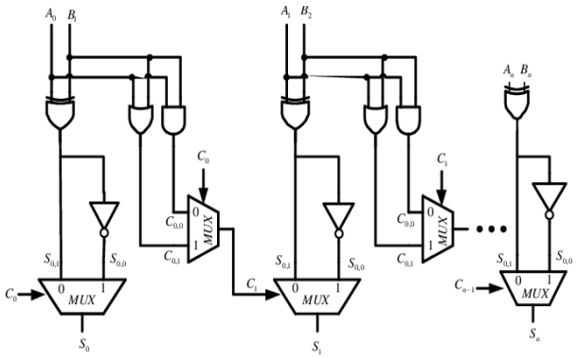


Figure - 4: Proposed Common Boolean Logic Diagram

$S = (A \oplus B)\, C'_{in} + (A \odot B)\, C_{in}$

$C = (AB)\, C'_{in} + (A+B)\, C_{in}$

It is clear that MUX bases its calculation of the final sum on the carry that has spread from the previous logic cell. The final sum and the carry for the next logic cell are both determined by the carry that will spread. The sum (S0) will be S1,0 if the carry propagating from the prior adder (C0) is "0," else, S0 will be S1,1. In other words, the carry that moves to the subsequent cell will be C1,0 if C0 is "0," else, it will be C1

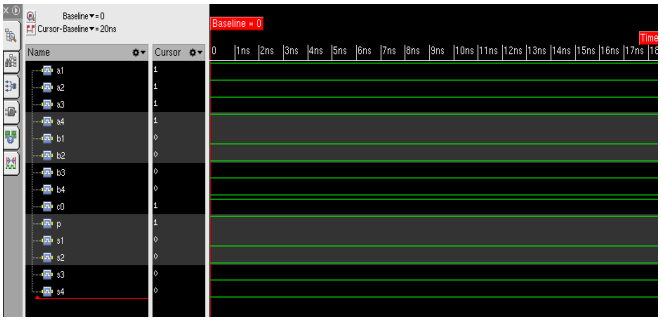


Figure-5 Simulated output for CBL

In the above-simulated output of common Boolean logic, it was observed that the number of inputs and outputs required in the circuit is less than that compared to conventional carry adders. due to which the total area and power reduce compared to the conventional method.

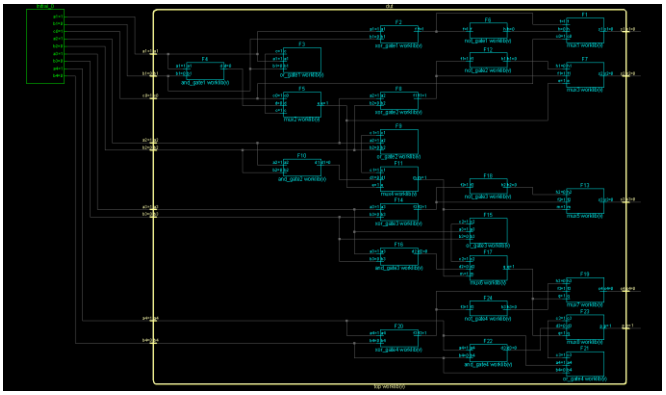


Figure 6: Schematic output of conventional carry skip adder

6. RESULTS

7. The table below shows the number of inputs LUTs and a total number of bonded IOBs. A look-up table, or LUT for short, is essentially a table that decides what the output is for any given input (s). It is known as the truth table in combinational logic. Your combinatorial logic behavior is effectively described by this truth table.

In other words, a LUT can implement whatever behavior you obtain by connecting any quantity of gates (such as AND, NOR, etc.), without feedback channels (to ensure it is state-less), and in any desired configuration.

An IOB is an input/output buffer. It essentially refers to the number of pins you have on your gadget. For instance, if your design includes a reset, a clock, an 8-bit input, and an 8-bit output (all single-ended), you will utilize 1+1+8+8=18 pins, resulting in 18 bonded IOBs.

Table 1: Comparison Between Conventional Carry Skip Adders And CBL.

Adders	No. of slices	No. of input LUTs	No. of bonded IOBs	Total
8-bit carry skip adders	1	2	18	21
CBL	1	1	10	12

Table-2: Power and area comparison of different adders.

Adders	Total power (μW)	Total area
Conventional carry skip adder	1.527	86.14
CBL (This work)	0.540719	72.00

The above table briefs us about the difference in the power and area of different types of addresses. power and the area have reduced in CBL compared to that of conventional carry skip adders this is due to the replacement of full adders with AOI circuits in the CBL circuits.

8-bit carry skip adders using full adders were simulated and the total power and area were calculated using cadence and LUT and a number of bonded IOBs were calculated, the obtained results were compared with the total area and power of common Boolean logic circuits. it was observed that the total area and power of CBL are less than that of conventional carry skip adders, this is because in CBL basic gates were used instead of full adders. Thus the obtained results are shown in the table1 and table 2.

7. CONCLUSION

The proposed adder is designed and the simulation results are examined using the Cadence tool in 45nm technology, simulations of Verilog code written for carry skip adder are carried out for power and area analysis. The same code has been analyzed in Vivado Design Suite and Xilinx ISE 14.2 and implemented on Zed Board. Findings indicate enhanced performance from the suggested adder. Compared to conventional carry skip adder 64.589 % decrease in power, an 18.737 % decrease of the area is visible in CBL (Common Boolean Logic).

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