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Analysis of FinFET and CNTFET based HybridCMOS Full Adder Circuit

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Abstract - *In the world of IC, the technology scales down to 32nmor below and CMOS has lost its recommendation during scaling beyond 32nm due to high power consumption and high leakage current. Scaling triggers Short Channel Effects that can be hard to conquer. So, FinFET is used because it reduces the shortchannel effects. FinFET can be used in the nanometre range. CNTFET is one of the replacements for present CMOS technology because it can provide a stronger control over the thinSi body and reduces the short channel effects. As the full adder isone of the most promising units of the ALU because it reduces speed and power consumption. The logic style used for implementation is a Hybrid CMOS (HC) Full adder which consumes fewer transistors and reduces power. Both technologies (FinFET and CNTFET) reduces short channel effects and can be used in nanometre technologies. In this paper, the main objectiveis to find out the analysis of the best efficient devices between FinFET and CNTFET based on the Hybrid CMOS Full Adder circuit. Here, these are proposed FinFET based Hybrid CMOS Full Adder and CNTFET based Hybrid CMOS Full Adder. These new hybrid adder is having only 10 transistors. The proposed full adder is a CNTFET and FinFET based design implemented using Synopsys tools in 32nm, 16nm, 10nm technology and calculates Power consumption, delay, and Power Delay Product (PDP) are investigated and showed with better result comparison.*

Key Words: **FinFET, Full Adder, CNTFET, MOSFET, Hybrid logic style**

1. INTRODUCTION

As the technology is scaled down, the electronics market is becoming more competitive, which results in low-power and low-energy. VLSI has become an important issue in today's consumer electronics. Therefore, many of the manufacturing industries are

designed in nanometer range for the demand forcompact, high performance, low power.

Nanometers rangedevices restricted with a phenomenon like Short Channel Effects which embraces hot carrier effect and tunneling over oxide thickness. To remove these limitations we use two major technologies i.e, FinFET and CNTFET which have stronger control over the thin Si body.

The addition is one of the most fundamental arithmetic components of the processor. In low power applications, Full Adder plays the most crucial role in it. Hence, it is veryimportant to execute the full adder circuit with low power and high performance. Conventional MOSFETs have been improved for low power and high-speed applications. However, the characteristics of the device are enhanced but there is still remains an issue with high active leakage.

Therefore, Fin-type Field Effect Transistor (FinFET) and Carbon Nano Tube Field Effect Transistor (CNTFET) has become the most promising substitute for the traditional MOSFET. In this paper, we compare the performances of FinFET and CNTFET with each other based on hybrid CMOSFull Adder circuits using different technologies.

The rest of the paper is arranged according to the sections as follows: In section II, An overview of FinFET, CNTFET, and Hybrid CMOS Full Adder. Proposed Work has shown in section III. In section IV, schematic design and simulations are presented. Section V analyzed and compare results. Finally, inSection VI it is concluded with future work.

2. OVERVIEW

2.1 CNTFET

The full form of CNTFET is Carbon Nano Tube Field Effect Transistor. Carbon Nanotube (CNT) is a Nano-scale tube that contains either a single or an array of carbon nanotubes. The layer is made up of graphite rolled up into a cylinder. Depending on the angle and diameter of the folding it may be either metallic or semiconducting. The differences between metallic and semiconducting CNT would be determined by chirality.

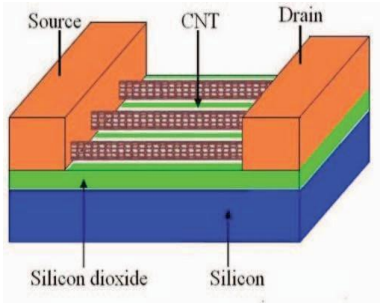

Fig.1: Structure of CNTFET [1]

CNTs are Hexagonal networks of carbon atoms and each tube acts as a channel whereas, in the MOSFET architecture, the whole silicon acts as a channel.

CNTFET is a 4 terminal device.

The heavily doped CNT is underneath the drain or the source while the pure CNT is placed under the gate (channel). It carries high drive current, higher transconductance and it has the same mobility in n-type and p-type. CNTFET's V-I characteristics are similar to MOSFET's.

One of the advantages of using CNTFET is that it eases the manufacturing process by using a rolled up the hollow cylindrical form of CNTs. It also shows better performance on gate capacitance due to the decrement of source and drain width. It allows for better switching speed and better short channel immunity. It requires less amount of power and propagation delay when compared to the CMOS devices.

CNTFET has the potential to mitigate the limitations of Silicon-based IC technology which has a physical limit to reduce the size of the devices to the nanoscale technology, due to its unique structures and magnificent physical & mechanical properties. Therefore, CNTFET is considered as one of the most promising devices for nanoscale technology.

2.2 FinFET

A FinFET was developed by Berkley researchers of the University of California. It was designed for use with SOI(Silicon-on-Insulator). FinFET is categorized as a type of multi-gate Metal Oxide Semiconductor Field Effect Transistor (MG-MOSFET). A Multi-Gate transistor combines several gates into one device. FinFET technology refers to its name to the fact that the FET structure used looks like a set of fins[4].

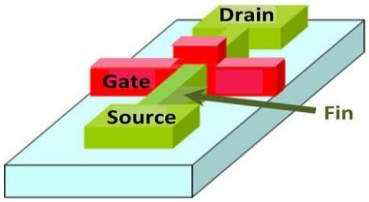

Fig.2: Structure of FinFET[4]

In this paper, we implemented the proposed circuit with FinFET using the SG Mode configuration. In Short-Gate (SG) mode, the front gate and the back gate are shorted together because it will give better driving strength to all over the circuit. If one of the inputs gets exaggerated then the operation would be controlled either by the front or back gate. This type of mode will help to achieve low leakage and it will be improved efficiency also.

2.3 Proposed Hybrid 1-bit Full Adder

Hybrid logic is the approach that requires using of different types of logic architecture. The proposed 1-BIT full adder circuit considerably improves the performance.

The implementation of full adder involves the following expression:

$$SUM = A \oplus B \oplus Cin \quad (1)$$

$$Cout = A \,.\, B + Cin \,.\, (A \oplus B) \quad (2)$$

The implementation must be done by the reduction in transistors and intracellular node connections in comparison to the conventional Full Adder. This proposed circuit can minimize the delay, power dissipation, area, and the overall performance of the circuit. One such implementation can be achieved by using a combination of TG(Transmission Gate) and PTL(Power Transistor logic).

The conventional hybrid CMOS full adder architecture can be split into three modules and block diagram is shown in fig:3.

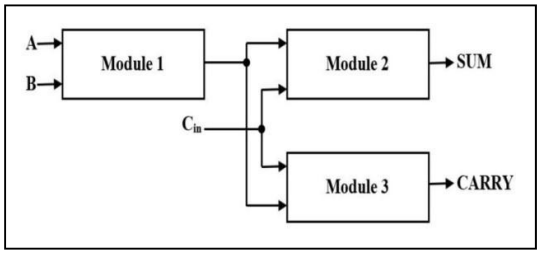

Fig.3. Block Diagram of proposed full adder[10]

Modules 1 and 2 are the XNOR modules which generate the sum (SUM) signal. The XNOR block modules are used to get better power and require non-complementary inputs which shows the perfect output. The CARRY output signal is generated by Module3. Therefore, these modules are designed to reduce power consumption by using the best possible extent that is avoiding the voltage degradation possibility.

There is a Level Restoration Circuit at the output stage. The output signal can get the output with full swings because of the Level Restoration Circuit. So, it can operate at low voltages and also provides a full-swing operation. This proposed circuit has a lower PDP as compared to the other types of different architecture. Despite of this, Modules II and III have low PDP. Therefore, the new adder is expected to have low power consumption.

3. PROPOSED WORK

The two new full adders consists of less number of transistors,because of less number of transistors results in less switching activity and area.

3.1 FinFET based 10T Hybrid CMOS Full Adder

The 16T Hybrid full adder circuit is improved to 10T which isshown in fig. 4. Here we are using shorted gate FinFET according to the modes of operation. There are two XNOR circuits using in 10T circuits which are in cascaded form.

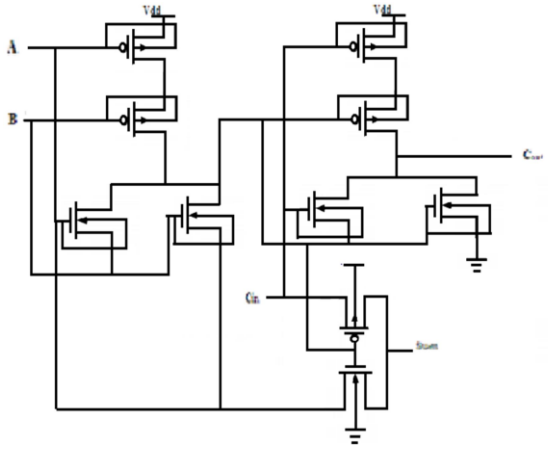

Fig. 4 : Circuit Diagram of FinFET based 10T Hybrid Full Adder

In this circuit, the first sum signal is generated and then the carry-out signal is generated. There are intermediate nodes, lower-transistor count, and having lower loading of the inputs which helps to generate a balanced Sum and Cout signal. The advantage of using 10T is to reduce power consumption because there is no direct path to the ground.

3.2 CNTFET based 10T Hybrid CMOS Full Adder

Hybrid logic design is one of the logic designs used for the implementation of a full adder. The number of transistorscount is 10, as shown in fig.5

A, B, and Cin are the inputs and Sum & Cout are the outputs. 10T generates A XOR B and to generate the output, it can be used with its complement as a select signal. The main advantage of using CNTFET based 10T is to perform exceptionally good at lower technologies. It has also a smaller delay because of its supply voltage. Meanwhile, the only disadvantage of using 10T full adder is to produce high capacitance values for the inputs.

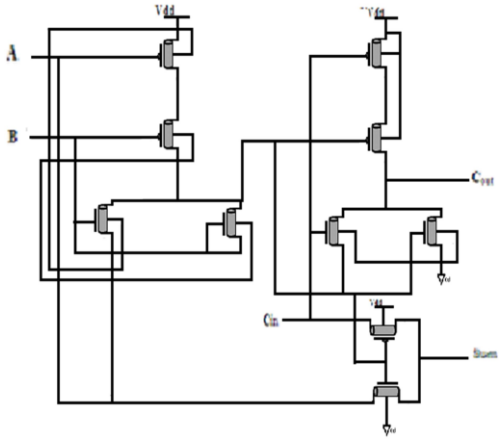

Fig. 5 : Circuit Diagram of CNTFET based 10T Hybrid Full Adder

A, B, and Cin are the inputs and Sum & Cout are the outputs. 10T generates A XOR B and to generate the output, it can be used with its complement as a select signal. The main advantage of using CNTFET based 10T is to perform exceptionally good at lower technologies. It has also a smaller delay because of its supply voltage. Meanwhile, the only disadvantage of using 10T full adder is to produce high capacitance values for the inputs.

4. SIMULATION RESULT

4.1Hybrid CMOS Full Adder

Figure 6 shows the schematic of the conventional 1-bit hybrid full adder. The proposed adder is designed with a combinationof three different logic blocks.

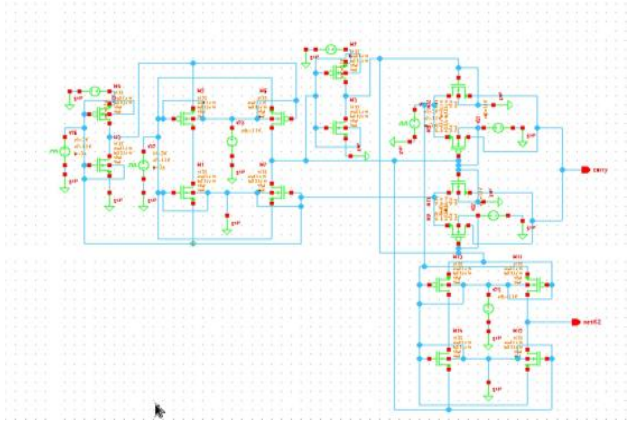

Fig. 6 : Schematic of Hybrid Full Adder

Fig. 7: Transient analysis of Hybrid Full Adder

4.2 Finfet based 10T hybrid CMOS Full Adder

Figure 8 shows the schematic of the Proposed 10 T Hybrid fulladder. The 16T Hybrid full adder circuit is improved to 10T, The supply voltage is taken as 0.85 V for FinFET based 10T Hybrid Full Adder using Synopsys Tool in 16nm technology.

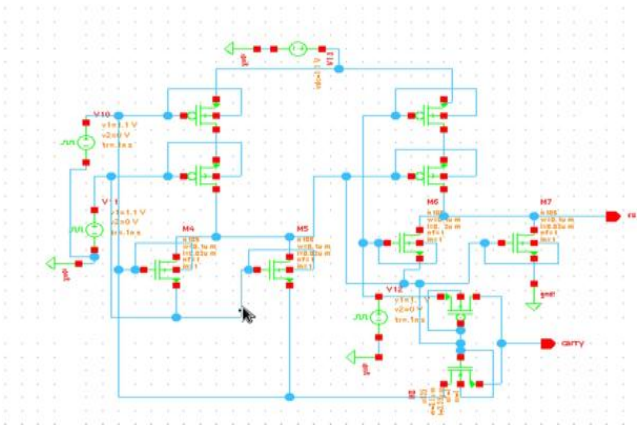

Fig. 8 : Schematic of FinFET based 10T Hybrid Full Adder

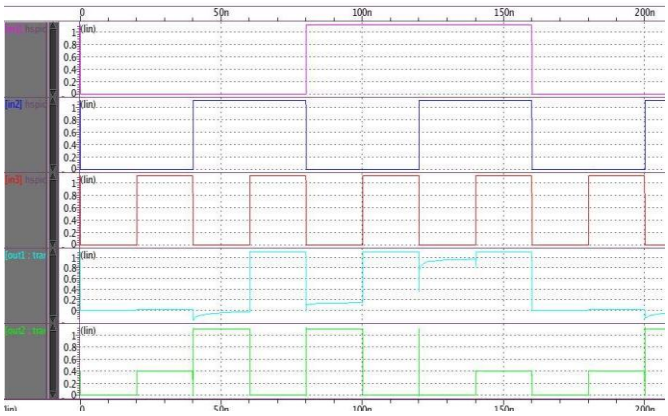

Fig. 9: Transient Analysis of FinFET based 10T Hybrid Full Adder

4.3 CNTFET based 10T Hybrid CMOS Full Adder

The results of the 10 Transistor simulation can be seen in figure 10. The simulation results show the proposed circuit can operate at a higher speed with low power dissipation. The CNTFET based 10T full adder is implementing using a supplyvoltage of 0.75 volts since 10nm technology is used.

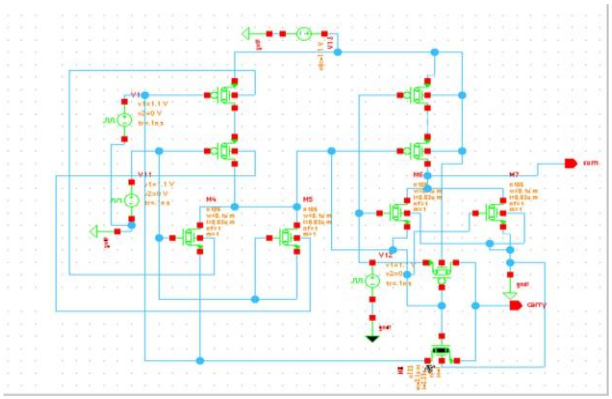

Fig. 10 : Schematic of CNTFET based 10T Hybrid Full Adder

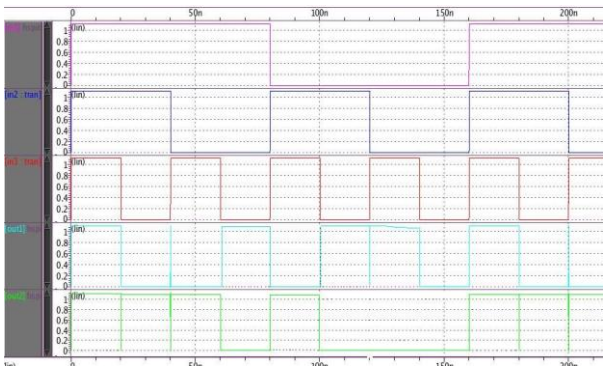

Fig. 11 : Transient Analysis of CNTFET based 10T Hybrid Full Adder

5. OBSERVATION

Those proposed circuits are compared in terms of power consumption, delay, and the number of transistors used in circuits.

Table -1: Performance Analysis

PARAMETERS	Hybrid CMOS FA	Proposed FinFET Design FA	Proposed CNTFET Design FA
Technology Used	32nm	16 nm	10nm
Supply Voltage	1.1 V	0.85 V	0.75 V
Power(uW)	2.079	2.902	1.9420
Delay(ps)	39.5	15.8	6.31
PDP 10^-21	82.8315	45.8516	12.2540

From the output waveform, calculate the values of power, delay, and power delay product. Power consumption and delaytime both are lowest for CNTFET based Hybrid Full Adder.

The FinFET based Hybrid Full Adder also have a very low delay comparison to Hybrid CMOS Full Adder.

CNTFET Based Hybrid Full adder has low power consumption and low delay comparison to both Hybrid CMOSFull Adder and FinFET based Hybrid Full Adder.

The results show that the CNTFET Hybrid FA is 93% less than the power consumed by Hybrid FA whereas CNTFET Hybrid FA is 66% less than the power consumed by FinFET Hybrid FA. The Delay of CNTFET Full Adder is reduced to 39% compared to FinFET based Hybrid CMOS FA whereas CNTFET Full Adder is reduced to 15% compare to Hybrid FA. CNTFET Full Adder is reduced to 26% and 14% toFinFET Full Adder and Hybrid Full Adder.

6. CONCLUSIONS

In this Paper, Full Adder circuits are implemented by using FinFET and CNTFET Technology Simulated in SYNOPSYS TOOLS using 32nm,16nm and 10nm Technology with the supply voltage of 1.1 V, 0.85 V and 0.75 V. One of the logic style that is hybrid CMOS modeling our proposed circuit. This type of logic design allows designers to operate flexibly on theCMOS region to achieve the overall performance of a circuit. Most conventional adders showed lower power consumptionat low voltage and higher power consumption at high voltage, but our proposed model surmounted this obstacle and showed lower power consumption in all types of the input voltage. The augmentation of efficiency, delay, and Time delay product (PDP) will be seen by a broad comparison of all designs.

Using the designed 1-bit full adder blocks, we can design the 2-bit, 4-bit, 8-bit, 16-bit, 32-bit, 64-bit Adder/Subtractor circuits, and so on. Besides that, the performance and potentialof other logic styles should be explored in future work. We can even design and compare these designs in all possible Nanometer technologies beyond 7nm.

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