International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 09 Issue: 10 | Oct 2022 www.irjet.net p-ISSN: 2395-0072

AN OUTLINE OF HARMONICS AND MULTILEVEL INVERTER

[1]Naumesh Kumar Verma, [2]Mrs. Simardeep Kaur, [3]Raina Jain

[1]PG, scholar, Dept. of Electrical and Electronics Engineering, SSGI, Bhilai, India.
[2]Assistant Professor, Dept. of Electrical and Electronics Engineering, SSGI, Bhilai, India.
[3]Assistant Professor, Dept. of Electrical and Electronics Engineering, CEC, Bilaspur, India.

Abstract- *As conventional energy sources run out, several nations are turning to renewable energy sources like solar, wind, and BESS. Large-scale photovoltaic PV power plants have emerged as one of the key development trends in the PV industry in the field of renewable energy. Over the past two decades, there has been a notable increase in the production of and integration of solar power plants into the utility grid. The utilization of power electronic devices, such as DC/AC converters, has grown as the number of photovoltaic power plants has increased. Inverters are the name for this electrical power equipment. Inverters serve as a bridge between the grid and renewable energy sources by converting direct current into alternating current. Power plants that produce harmonics in the system use inverter-based technology and other non-linear loads. A lot of work has gone into developing ways for getting rid of or cutting down on harmonic distortions that this conversion's output causes. The purpose of this study is to look into the factors that contribute to harmonics in PV inverters, as well as their impacts and methods for reducing them.*

Key words: Harmonics, Inverter, Multilevel Inverter.

1. INTRODUCTION

The problem of grid harmonics isn't new. Utilities recognized the importance of harmonics within the Twenties and early Nineteen Thirties once distorted voltage and current waveforms were discovered on transmission lines. At that time, the key considerations were the consequences of harmonics on synchronous and induction machines, telephone interference, and power condenser failures. Results of a number of the first investigations are also reviewed by considering a typical 250-mile, 220-kV transmission line:

1. A sending-quit emf of seven percentages 1/3 harmonic incorporates fifty three percentage 1/3 harmonic on the receiving quit of the road.

2. Under full load, the 1/3 harmonic on the quit of the road is decreased from fifty three to 29 percentage.

3. The energy component on the generator aspect is 0.848 for a wave containing harmonics (in comparison with 0.96 for a harmonic-loose sinusoidal wave).

4. The energy component on the load aspect is 0.82 for a harmonic-loose sinusoidal waveform and is measured as 0.75 through metering.

5. For an induction motor constructed in 1930, harmonics triggered vibrations and periodic rasping sounds. Input energy measurements vary due to relative harmonic content. Rotor currents also are vary for numerous harmonic contents.

Such behavior, actual within side the 1930s, can also additionally nevertheless exist today. Manufacturers' response to harmonics had been to construct gadget that tolerates greater harmonics and to lessen mutual coupling to cell phone circuits. Nevertheless, it's far clean that harmonics are once more turning into a extreme problem, representing for the primary time capability harm to purchaser hundreds in addition to the strengthnetwork.
The Issue Today's control framework consonant issues can be followed to a number of variables:

1. The significant increment of nonlinear loads coming about from modern innovations such as silicon-controlled rectifiers (SCRs), control transistors, and chip controls etc.

2. Arevision to the gear plan's logic. The lower-below 5-Khz frequency range appears to be the most harmful for controlling machinery and gadgets.

These conditions are no longer valid, and utilities are increasingly concerned about noise.

2. EFFECTS OF HARMONICS ON THE POWER SYSTEM

For more than 50 a long time, harmonics have been detailed to cause operational problems. A few of the major impacts incorporate:

1. Capacitor bank disappointment from dielectric break-down-or responsive control over-burden.

2. Obstructions with the swell control and control line carrier frameworks, which result in the breakdown of the metering, stack control, and further exchanging structures.

3. Intemperate misfortunes in-and warming of-induction and synchronous machines.

4. Overvoltage's and over the top streams on the system' from reverberation to consonant voltages or streams on the network.

5.Dielectric breakdown of protects cables coming about from consonant over voltages on the system.

6 Frameworks for broadcast communications with inductive impedances.

7. Mistakes in induction kWh meters.

8. Flag obstructions and transfer glitch, especially in solid-state and microprocessor-controlled frameworks.

9. Impedances with expansive engine controllers and power plant excitation frameworks.

10. Mechanical motions of induction and synchronous machines.

11. Unsteady operation of terminating circuits based on zero voltage crossing discovery or locking.

These impacts depend, of course, on the consonant source, its area on the control framework, and the arrange characteristics that advance the engendering of harmonics.

2.1 Sources of Harmonics Harmonic

Sources are separated into two categories:

1. Built up and known.

2. Modern and future.

2.2 Established Harmonics Sources

'A survey of the writing demonstrates that the known sources of harmonics incorporate

1. Tooth swell or swells within the voltage waveform of turning machines.

2. Varieties in air-gap hesitance over synchronous machine post pitch.

3. Flux mutilation within the synchronous machine from sudden load changes.

4. Nonsinusoidal dissemination of the flux within the discuss crevice of synchronous machines.

5. Transformer magnetizing streams.

6. Arrange nonlinearities from loads such as rectifiers, inverters, welders, bend heaters, voltage controllers, recurrence converters, etc.

2.3 Analysis of Harmonics and Their Sources

Systems containing nonlinear circuit parameters carry non sinusoidal streams indeed when the connected voltage is of a pure-sine waveform. Gadgets such as rectifiers and soaked transformers have been said as causes of circuit nonlinearity which cause voltage and cur-rent sounds. The genuine wave shapes change considerably and depend on the loads and the control sources. Whether single or three-phase, once the wave shape of both the current and voltage have been decided, the consonant substance can be analyzed. Examinations to determine the size and arrange of sounds are based on Fouri-er's hypothesis and the application of Quick Fourier Changes is the premise for advanced investigation of inspected information [1]

3. MULTILEVEL INVERTER

At first the inverters were utilized to drive for the most part the helping stack when the framework gets off. But, these days dueto expanded progression in innovation inverters improves their skyline of applications. In prior days as it were two level inverter were utilized and produces the yield with two distinctive voltage levels but it has tall exchanging misfortunes and consonant voltage causes the stream of the consonant current within the circuit and produces the misfortunes. So, to overcome the impediments certain headway takes put in existing inverter such that levels can be expanded more than two so that unadulterated sinusoidal waveform is delivered at the output voltage and sounds within the yield can be smothered and rate of misfortunes can be diminished and this topology is named as multilevel inverter topology.

There are mainly three different types of the multilevel inverter

1)Diode clamped multilevel inverter.

2)Flying capacitor multilevel inverter.

3)Cascaded H-bridge inverter.

Over these multilevel inverter has a few focal points over the two level inverter.

1) Diminished Consonant impact of distortion.

2) Immaculate sine waveform due to numerous voltage levels.

3) Works at
both essential and tall exchanging recurrence PWM

4) Diminished exchanging misfortunes

5) Tall control quality

6) Low rate of alter of voltage

Tragically multilevel inverter do have a few disadvantage one primary disadvantage of these it requires number of switches indeed in spite of the fact that they are of littler rating. Each switch is related to its door driving circuit since of that generally framework gets to be more complex and expensive.

4. CONCEPT OF MULTILEVEL INVERTER

Conventional two level inverter produces two levels within the yield voltage. Indeed in spite of the fact that the AC yield waveform is delivered it incorporates sounds and these causes the tall rate of alter of voltage as compared to the multilevel inverter. A few gadgets demands for low rate of alter in voltage.

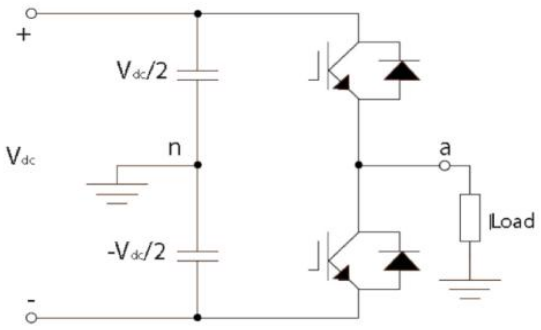

Figure 1-Two level inverter

In multilevel inverter we create more than two voltages level which shows nearly inoculate sinusoidal yield voltage wave-form.Whichhas low dv/dt, low consonant distortions since of numerous voltage levels within the yield the wave-form gets to be more smoother but with expanding levels the circuit gets to be more complex due to expansion of the valves. And complicated control circuit is additionally re-quired

4.1 Comparison between conventional and multilevel inverter

S.no	Conventional in-verter	Multilevel inverter
1.	Higher THD in yield voltage	Lower THD in yield voltage
2.	Device has high switching stresses	Device has low switching stresses
3.	Not applicable for application having high voltage	Applicable for appli-cation having high voltage
4.	Unable to produce high voltage level	Can produce high voltage level
5.	Switching losses are high	Switching losses are low

5. DIFFERENT TOPOLOGIES OF MULTILEVEL IN-VERTER.

Figure-2 Topologies of multilevel inverter

There are essentially three sorts of multilevel inverter classified agreeing to the voltage source utilized within the inverter. The Fig.2 underneath appears the topologies of multilevel inverter

5.1 Diode Clamped Multilevel Inverter

It was developed in 1981 and is also known as a neutral point clamped inverter (NPC). The DCMLI topology, which is utilised to produce an output voltage with three levels, is shown in Figure 3. Four unidirectional power switches, two diodes, and two capacitors make up this topology's configuration. To distribute the blocking voltage among the clamping diodes, they are wired in series.

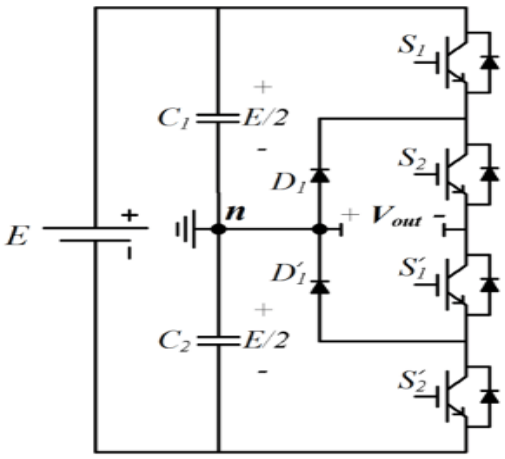

Figure 3- Diode Clamped Multilevel Inverter

The output voltage in this architecture has three levels: Vdc/2, 0, and Vdc/2. Vdc/2 is produced by leaving S1 and S2 switches on, while Vdc/2 is produced by turning on S3 and S4. The 0 level voltage is created by turning on switches S2 and S3. It is anticipated that each active switching device will experience voltage stress throughout the passage of the equivalent voltage across the DC link capacitors, with this voltage stress being clamped to the voltage of each capacitor using diode clamping. In a practical application, the clamping diodes are connected in series to share the blocking voltage. Then, each active device merely needs to block a voltage level of V /(m 1) dc. The clamping diodes' voltage ratings must differ for reverse voltage blocking. The primary problem with the design in high voltage applications, when using the DCMLI under PWM, is the clamping diodes' diode reverse recovery. Due to its high-power delivery capability, simplicity, and efficiency, the DCMLI has a greater industrial use than the other multilevel converter topologies. It has found use in variable speed motor drives, high voltage system interconnections, and static VAR compensators (SVC). The DCMLI converter does not require a capacitor because all of its parts are connected via a single DC bus. As a result, it can be applied to different back-to-back topologies, such as adjustable speed drives and high voltage back-to-back connectivity. However, the issues with this converter include the challenge of balancing and stabilising the capacitor DC voltage in the DC link, as well as the difficulty in real power flow from a single inverter owing to discharging or overcharging of the DC level without proper control.

5.2 Flying Capacitor Multilevel Inverter

The topologies of the FCMLI and DCMLI are very similar; the difference is that the FCMLI uses floating capacitors rather than clamping diodes. The size of the voltage steps in the output waveform of the FCMLI is a direct result of the voltage variation in the nearby capacitors. The'm' level inverter's FCMLI structure consists of 0m 1 0 DC link capacitors. Figure 4 shows a schematic of the three-level FCMLI topology, which also includes a DC supply with two capacitors to acquire the voltage levels (Vdc/2, 0, and Vdc/2) and four unidirectional power switches and a flying capacitor. For the positive polarity output voltage to be produced, switches S1 and S2 must be in the ON position, while while S3 and S4 are switched ON for the negative polarity output voltage. Switches S1 and S3 or S2 and S4 are activated to produce the output voltage at the 0 level. Compared to a DCMLI, the voltage synthesis in the FCMLI is more adaptable. By carefully choosing the switching combination, the issue of voltage balancing can be solved when there are more than five levels. The ability to manage the reactive and active power is one of this topology's main advantages. On the other hand, the usage of several capacitors makes the system expensive and challenging to assemble. Furthermore, real power transmission in such setups suffers from large switching frequency losses.

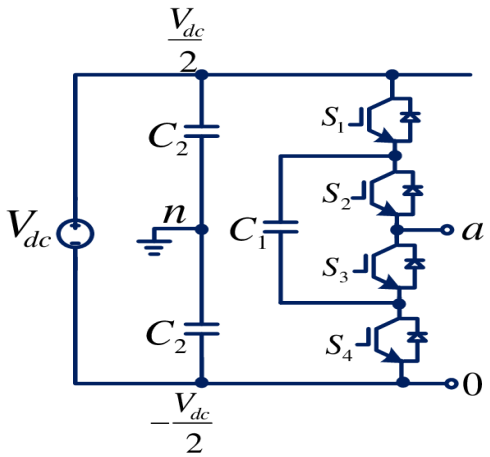

Figure 4- Flying Capacitor Multilevel Inverter

5.3 Cascaded H-Bridge Inverter

The serial connecting of several single-phase H-bridge inverters with independent DC sources results in the creation of CHB-MLIs (SDCS). Figure 3 depicts an H-bridge with four unidirectional power switches and one DC supply. The four switches (S1-S4) are connected in various ways to generate the desired output. Each inverter level is programmed to provide three voltage outputs (+Vdc, 0, and Vdc) via the connection of the DC source to the AC output. The +Vdc output is created when the S1 and S4 switches are in the ON position, whereas the Vdc output is produced when the S2 and S3 switches are in the ON position. Either S1 and S2 or S3 and S4 must be in the ON state in order to generate the 0 output voltage. The full-bridge inverter's AC outputs are connected in series such that the voltage waveform created represents the total of the outputs from all the inverters. The number of output phase voltage levels in a cascade inverter is denoted by m = 2s + 1, where s is the variety of DC sources. Compared to DCMLI and FCMLI, this design requires fewer components because clamping diodes and clamping capacitors are not used. Additionally, because it lacks DC link capacitors, it is free of the voltage balancing issue. Conversely, independent renewable energy sources and separate converters can be used to replace the various DC sources, or by single renewable energy sources with multioutput converters where the voltage balancing is the major concern. Multilevel cascaded inverters have been proposed for use in applications for the generation of static variables, as well as an interface with RES; they have also been considered for use in battery-powered applications. A cascade inverter can be directly connected in series with the electrical system and utilised for static var correction as well. As they require independent DC sources when utilised in fuel cells and photovoltaics, they are appropriate for connecting RES to the AC grid. They have also been suggested for usage as the primary traction drive in electric vehicles because several batteries or ultracapacitors work as SDCSs in these applications. This topology's structure is adaptable and can be employed with various numbers of inverter levels. By applying varying ratios of DC sources and minimising switching redundancy caused by inner voltage levels, different output voltages can be generated. To lessen the requirement for independent DC sources, transformer-dependent CHBMLIs have been created; they have a CHBMLI-like structure but are distinguished by the serial connection of the output voltage of the isolation transformer.[2]Here, the proposed study outlines the design and application of a novel multilevel inverter method for a solar-powered board. Most often, two level cascade inverters are used for voltage conversion from DC to AC. In this study, a two-level inverter was able to provide two distinct voltage levels or yields. The yield voltage waveform is roughly in the shape of two levels, therefore the THD of a 2-level inverter isn't as high, or unusually high. To limit and lower the THD value, an underused multilayer inverter is shown here with fewer switches. Different levels of DC voltage sources are used to synthesize the desired AC voltage.[3]

Two different types of multi level inverters were modelled and implemented in hardware in this study. According to the results of the simulation, the proposed topology 2's THD Range has a consonant mutilation spectrum of 5.51%.

The proposed architecture 1 includes actualized multi carrier stage relocated PWM as well. The most hard scenario is the voltage adjustment problems at the source and stack sides. By utilising a hysteresis controller within the proposed topology, the capacitor voltage adjusting technique is developed based on third consonant balanced infusion1. The model that was additionally produced for both the planned and actual results was also authorized. [4]

The use of a seven-level cascade H-bridge MLI for a grid-connected PV framework based on a Phase Shift Pulse Width Modulation (PSPWM) method was demonstrated in this paper. The system was successful in providing a compelling interface between the network and divided sun based boards as DC sources by controlling the battery execution based on MPPT and an advanced control technique.

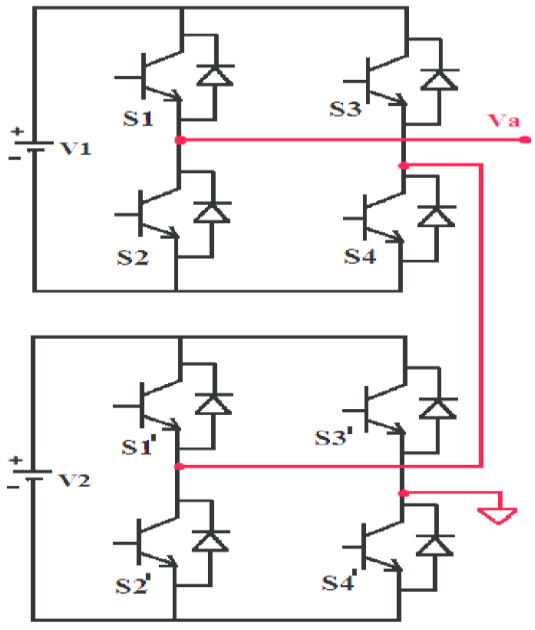

Figure 5 Cascaded H-Bridge Inverter

The proportionate demonstration includes three boards associated in arrangement to constitute the actualized PV/battery framework coordinates with the H-bridge MLI. By regulating battery performance, the DC transmission voltage is kept stable in the face of various disruptive factors. Additionally, compared to a standard inverter, the cascade H-bridge MLI execution appears to significantly reduce noise. This makes the Inverter capable of eliminating a tall sum of consonant, with moo THD voltage.[5]

This study investigates the operation of a PV system with a boost converter, where the MPPT method and a multi-level inverter topology control the exchange. Due to its ability to provide waveforms with a far wider consonant range, multilevel inverters are suitable for use in high voltage and high control applications. This study first discusses the design and consideration of the P-V and I-V characteristics of the PV framework, after which the yield is related to the boost converter. MPPT calculation with P and O sort is used for exchanging. Finally, this previous structure is connected to a cascaded multilevel inverter based on multiple carriers. The elemental yield voltage is improved by the cascaded multilevel inverter technique, which also reduces consonant mutilation. To answer the question, a single stage, five level cascaded inverter is used. Effectively, the ponder can be stretched to an m-level inverter. Consonant examination, measured THD, and yield voltages are contrasted and analysed with a DC-AC inverter in an effort to validate the framework's main elements.[6]

When compared to other conventional topologies, the inverter in the suggested figure contains less switches. The switch diminishment causes a decrease in the starting amount fetched. From the reproduction, the THD value is determined, and it is compared to the THD value of a multilayer inverter with values from more recent times and after level sifting. This results in a decrease in THD value when using the Specific Consonant End Beat Width Tweak Strategy. Here, THD is reduced by using closed-circle PWM techniques. Utilizing LCL filtering condition will reduce it initially as you learn a sounds period.

6. RESULT

As conventional energy sources run out, several nations are turning to renewable energy sources like solar, wind etc. Large-scale photovoltaic PV power plants have emerged as one of the key development trends in the PV industry in the field of renewable energy. Inverters serve as a bridge between the grid and renewable energy sources by converting direct current into alternating current. In this paper detail of harmonic and multilevel inverter has been discussed and various latest techniques which are used in today's world.

REFERENCES

1. P. S. Harmonics, "Power System Harmonics: An Overview," in IEEE Transactions on Power Apparatus and Systems, vol. PAS-102, no. 8, pp. 2455-2460, Aug. 1983, doi: 10.1109/TPAS.1983.317745.

2. A. K. Koshti and M. N. Rao, "A brief review on multilevel inverter topologies," 2017 International Conference on Data Management, Analytics and Innovation (ICDMAI), 2017, pp. 187-193, doi: 10.1109/ICDMAI.2017.8073508.

3. Yadav, Sagar & Khadse, Chetan. (2019). Implementation of Multilevel Inverter for Harmonic Reduction in Solar PV Application. 665-669. 10.1109/ICICICT46008.2019.8993146.

4. R. Priya and R. Valli, "Advanced Multilevel Inverter Techniques for PV Applications with Reduced Switching Devices and THD with Voltage Balancing," 2019 IEEE International Conference on System, Computation, Automation and Networking (ICSCAN), 2019, pp. 1-7, doi: 10.1109/ICSCAN.2019.8878702.

5. Hassan, Abdelwahab & Azmy, Ahmed & Yehia, Doaa & Gurgi, Zeina. (2018). Harmonic Reduction for Grid-Connected Photovoltaic System based on Multilevel Inverter. Australian Journal of Basic and Applied Sciences. 12. 135-145. 10.22587/ajbas.2018.12.9.23.

6. R. Priya and R. Valli, "Advanced Multilevel Inverter Techniques for PV Applications with Reduced Switching Devices and THD with Voltage Balancing," 2019 IEEE International Conference on System, Computation, Automation and Networking (ICSCAN), 2019, pp. 1-7, doi: 10.1109/ICSCAN.2019.8878702.

BIOGRAPHIES

Naumesh kumar verma is a student of Mtech (Power system) in electrical and electronics engineering of final year. He is perusing Mtech degree from Shri Shankaracharya Group of Institution affiliated with Chhattisgarh swami Vivekananda Technical University. His interest is in power system, artificial intelligence and renewable energy.

Mrs. Simardeep Kaur received her M. Tech degree in Electrical Engineering from RGPV, Bhopal. She is currently pursuing Ph.D. degree in Electrical Engineering. Currently, she is faculty in SSTC, Bhilai. Her research interest includes distribution generation protection, distributed generation & Micro Grid.

Raina Jain has received her Bachelor of Engineering Degree in Electrical Engineering from lakhmi chand institute of technology, Bilaspur in 2017. Master's Degree in Power System Engineering from SSTC, SSGI, Bhilai, in 2021 affiliated with Chhattisgarh Swami Vivekanand Technical University, Bhilai. She is currently working as an Assistant Professor at the Department of Electrical And Electronics Engineering, in Chouksey Engineering College, Bilaspur. Her area of interest is in power system, artificial intelligence, control system, and renewable energy .