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Design of Optimized Vedic Multiplier

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Abstract - *Multiplication is an essential operation in most arithmetic applications, and multipliers form one of the most important elements in any digital signal processor. Speed and area efficient multipliers are crucial in DSP applications. The speed of digital circuits must be increased and the area must be decreased. In this paper, an Urdhva-Tiryakbhyam algorithm based 8 X 8 and 16 X 16 Vedic multiplier using carry save adder, which has optimized speed and area is designed. The proposed algorithm was developed in Verilog HDL, and its implementation was carried out using Xilinx Vivado. The suggested multiplication technique is then illustrated to show its usefulness. This Vedic multiplication circuit has turned out to be effective in terms of speed and area.*

Key Words: Carry Save Adder, Urdhva Tiryakbhyam Sutra, Vedic Multiplier, Vedic Mathematics

1. INTRODUCTION

Multipliers are one of the most common elements in digital circuit designs, since they are fast, reliable, and efficient components. There are varieties of multipliers present and depending on the type of application, specific architecture is selected to suit the requirements.

Multipliers generally determine the performance of an algorithm, because multipliers are usually placed in the critical delay path of the algorithm. Different algorithms are available for use, each with a unique set advantages and trade-offs in various parameters like speed, power, or area. Since digital multipliers play a crucial role in DSP, research on them has always been active.

1.1 Vedic Multiplication

The proposed multiplier architecture is developed on the basis of Vedic multiplication Sutra. Vedic sutras are used in even the traditional way to multiply two integers in the decimal system. This paper uses Vedic multiplication sutras, which are applied to the binary number system.

1.2 Urdhva Tiryakbhyam Sutra

The multiplier proposed is developed on the basis of ancient Indian Vedic Mathematics algorithm Urdhva Tiryakbhyam (UT). The UT Sutra facilitates the simultaneous generation of partial products and the sums associated with them. The algorithm can be generalizable to n x n bit numbers.

1.3 Algorithm for 8 X 8 Bit Multiplication using UT

Consider two 8-bit numbers are M and N

$$M = M_7\ M_6\ M_5\ M_4\ M_3\ M_2\ M_1\ M_0$$
$$N = N_7\ N_6\ N_5\ N_4\ N_3\ N_2\ N_1\ N_0$$

Let $A_0 = M_3\ M_2\ M_1\ M_0$ and $A_1 = M_7\ M_6\ M_5\ M_4$
$B_0 = N_3\ N_2\ N_1\ N_0$ and $B_1 = N_7\ N_6\ N_5\ N_4$

$$\begin{array}{r} A_1\ \ A_0 \\ \times \\ B_1\ \ B_0 \\ \hline F\ E\ D\ C \end{array}$$

$$CP = A_0 * B_0 = C$$
$$CP = A_1 * B_0 + A_0 * B_1 = D$$
$$CP = A_1 * B_1 = E$$

where, CP = Cross Product and F= Carry Overflow

1.4 Algorithm for 16 X 16 Bit Multiplication using UT

Consider two 16-bit numbers are M and N

$$M = M_{15}\ M_{14}\ M_{13}\ M_{12}\ M_{11}\ M_{10}\ M_9\ M_8\ M_7\ M_6\ M_5\ M_4\ M_3\ M_2\ M_1\ M_0$$
$$N = N_{15}\ N_{14}\ N_{13}\ N_{12}\ N_{11}\ N_{10}\ N_9\ N_8\ N_7\ N_6\ N_5\ N_4\ N_3\ N_2\ N_1\ N_0$$

Let $A_0 = M_7\ M_6\ M_5\ M_4\ M_3\ M_2\ M_1\ M_0$ and $A_1 = M_{15}\ M_{14}\ M_{13}\ M_{12}\ M_{11}\ M_{10}\ M_9\ M_8$
$B_0 = N_7\ N_6\ N_5\ N_4\ N_3\ N_2\ N_1\ N_0$ and $B_1 = N_{15}\ N_{14}\ N_{13}\ N_{12}\ N_{11}\ N_{10}\ N_9\ N_8$

$$\begin{array}{r} A_1\ \ A_0 \\ \times \\ B_1\ \ B_0 \\ \hline F\ E\ D\ C \end{array}$$

$$CP = A_0 * B_0 = C$$
$$CP = A_1 * B_0 + A_0 * B_1 = D$$
$$CP = A_1 * B_1 = E$$

where, CP = Cross Product and F= Carry Overflow

2. METHODOLOGY

The 8 X 8, 16 X 16 multipliers are developed and tested for functionality using the proposed Vedic multiplier algorithm. High-speed arithmetic can be computed effectively using Vedic mathematical methods. The UT sutra demonstrates that it is a practical method for achieving fast multiplication operations. Due to the parallel computation of partial products when the UT sutra is used, the multiplier unit's latency is decreased.

The carry-save adder is used in this case to calculate the partial products of multiplication. This enables architectures that quickly calculate the partial products using a tree of carry-save adders. The final multiplication result is then obtained by adding the final set of carry bits to the final partial products using one "normal" adder. For this final stage, it is typical to employ a very quick carry-lookahead or carry-select adder to achieve the best performance.

2.1 8 X 8 Vedic Multiplier

Fig.1 shows the existing 8 X 8 architecture. For proposed 8 X 8 Vedic multiplier presented in paper, architecture is developed as in Fig 2. The proposed method is realized using four 4 X 4 multiplier and adder blocks. Carry save adders are utilized to increase overall speed and optimize the area. In the Fig.2, a 16-bit output is generated by multiplying two 8-bit inputs. The adder blocks utilized in the design will not add a lot of latency because they are employed in carry save arrangements. This design has a larger than average transistor count. However, the improved performance is a compensation for the hardware complexity. As can be observed, CSA block inputs have zero padding. This is to ensure that all inputs to the CSA stage have uniform bit lengths.

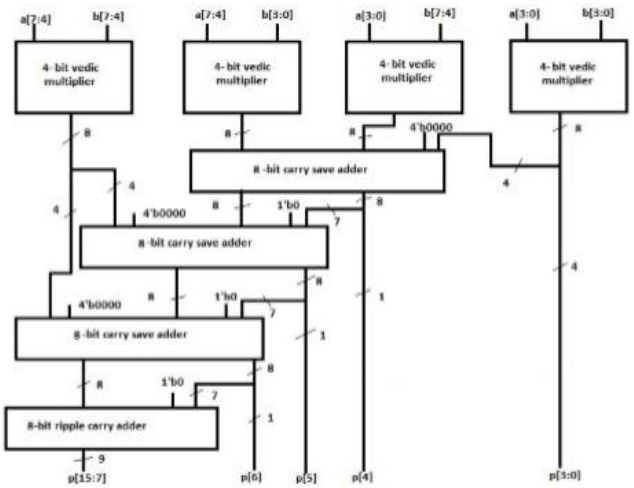

Fig -1: Existing 8 X 8 Multiplier Architecture

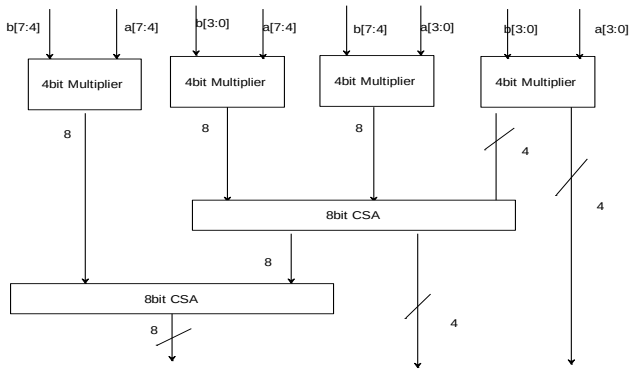

Fig -2: Proposed 8 X 8 Multiplier Architecture

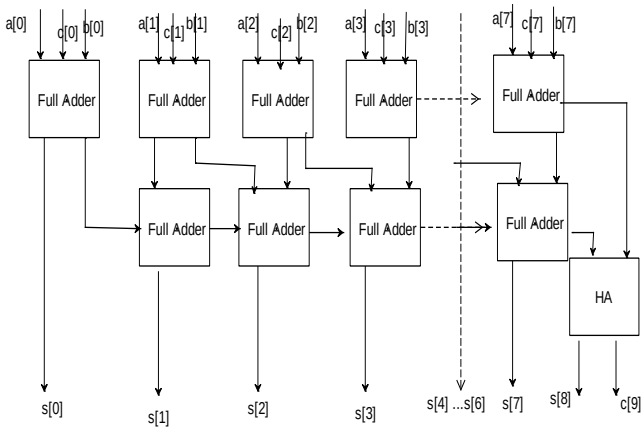

Fig -3: 8-bit CSA

2.2 16 X 16 Vedic Multiplier

Initially a 2-bit Vedic multiplier is designed, then progressive multiplier stages are designed to obtain the 16 X 16 multiplier design. Following that, 8 X 8-bit Vedic multipliers and 16 X 16- bit Vedic multipliers were built utilizing the 4- bit multiplier as basic block.

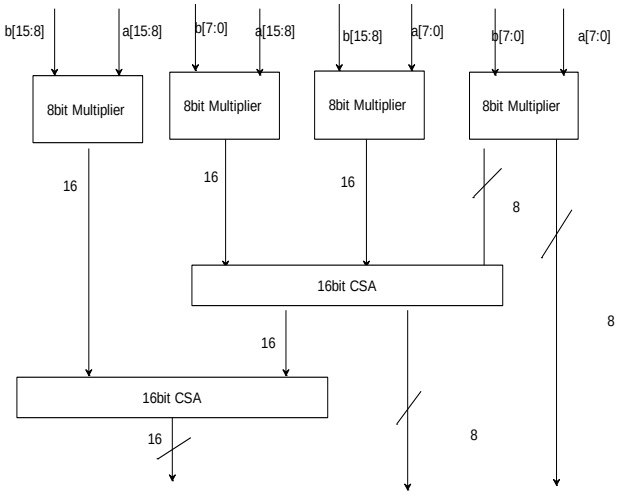

Fig -4: Proposed 16 X 16 Multiplier Architecture

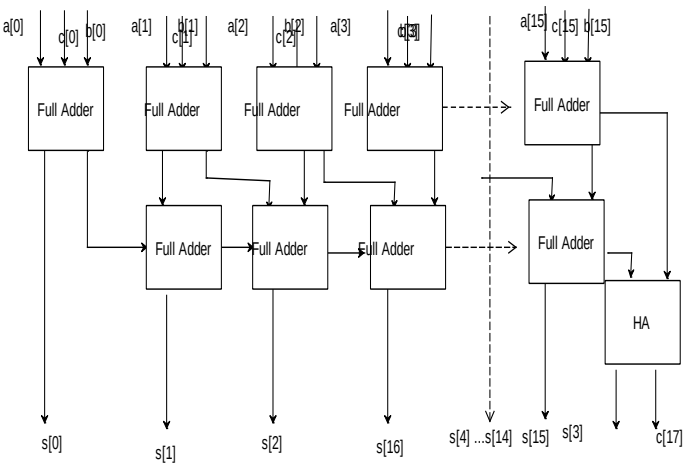

Fig -5: 16-bit CSA

3. RESULTS

Fig. 6 shows the RTL schematic of the proposed 8 X 8- bit Vedic Multiplier circuit and Fig.9 shows the RTL schematic of proposed 16 X 16 Vedic Multiplier. As mentioned earlier, we see that the proposed system uses Carry Save adders. Fig.7 and Fig. 10 shows the output simulation waveforms. For both the circuits, resource utilization is shown in Fig.8 and Fig. 11. The design is implemented in Xilinx Vivado using Verilog HDL.

3.1 8 X 8 Vedic Multiplier

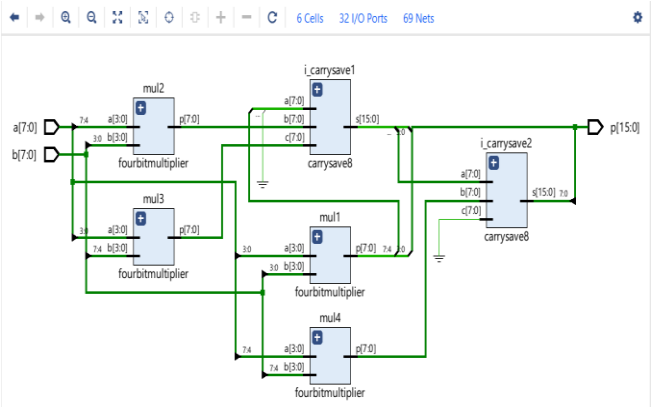

Fig -6: RTL Schematic of Proposed 8 X 8 Multiplier

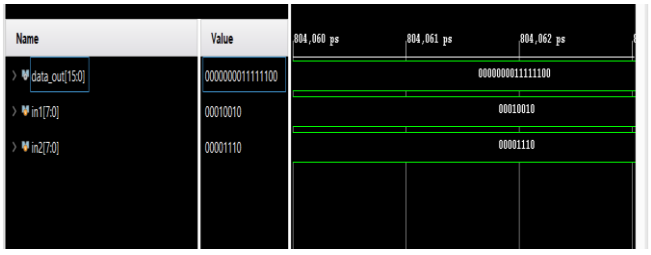

Fig - 7: Output waveform of Proposed 8 X 8 Multiplier

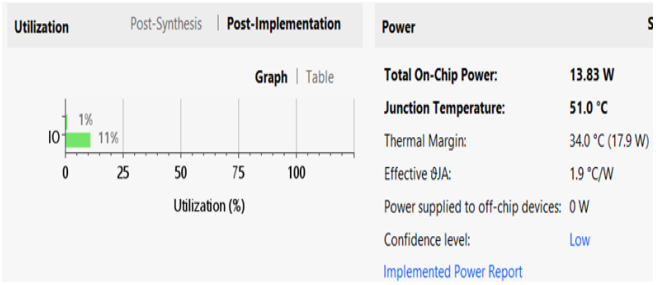

Fig -8: Resource utilization of Proposed 8 X 8 Multiplier

3.2 16 X 16 Vedic Multiplier

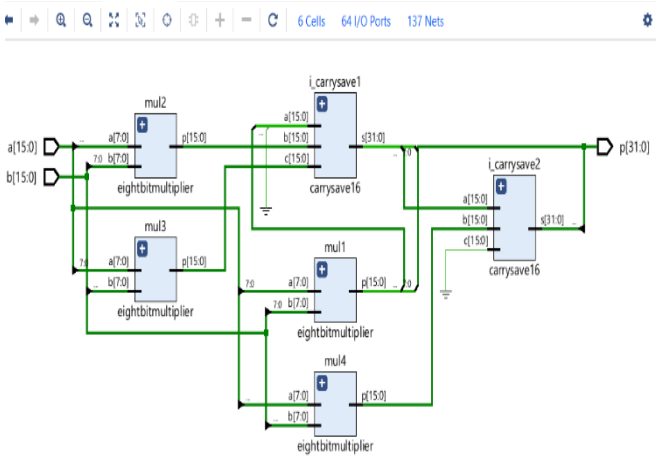

Fig -9: RTL Schematic of Proposed 16 X 16 Multiplier

Fig -10: Output waveform of Proposed 16 X 16 Multiplier

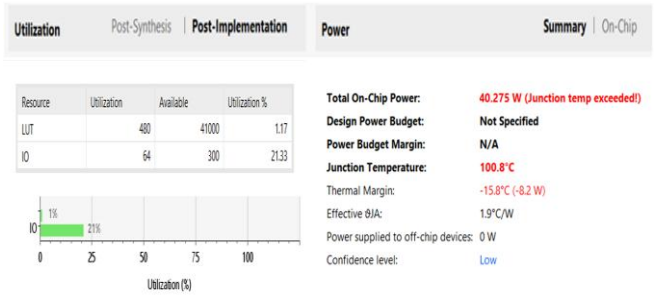

Fig -11: Resource utilization of Proposed 16 X 16 Multiplier

3.3 Device Utilization Summary

Table 1 shows the summary of device utilization of the implemented 8 x 8 and 16 x 16 Vedic Multipliers.

Table-1: Summary of Utilization

Logic utilization	8 X 8 Vedic Multiplier	16 X 16 Vedic Multiplier
Number of Slices	33	143
Number of LUT's	109	480
Number of bonded IOB's	32	64
Time Delay (ns)	11.743	14.055

3.4 Comparison between other multipliers and Proposed Vedic Multiplier (8 x 8)

Time delay and area, as shown in Table 2, are two important multiplier parameters that were improved for the 8 X 8 multiplier as shown from the results, illustrating the advantage of Vedic multipliers over other multipliers.

Table-2: Comparison between conventional multipliers and Proposed 8 x 8 Vedic Multiplier

Multiplier	Area (in LUT)	Delay (in ns)
Booth Multiplier	216	25.860
Array Multiplier	130	23.106
Wallace Multiplier	145	16.678
Proposed Vedic Multiplier	109	11.743

3.5 Comparison between other multipliers and Proposed Vedic Multiplier (16 x 16)

The time delay and area for a 16 X 16 multiplier is compared and contrasted using different multipliers in Table 3.

Table-3: Comparison between conventional multipliers and Proposed 16 x 16 Vedic Multiplier

Multiplier	Area (in LUT)	Delay (in ns)
Booth Multiplier	632	37.041
Array Multiplier	505	61.241
Wallace Multiplier	590	36.7
Proposed Vedic Multiplier	480	14.055

Performance of various 8X8 and 16X16 multipliers is compared, considering parameters like delay and number of LUT's. In comparison to the conventional multipliers, it is found that the proposed Vedic multiplier's computation speed is relatively faster. The delay is found to be lesser (11.743 for 8 X 8 multiplier and 14.055 for 16 X 16 multiplier). Additionally, there are lesser LUTs in the proposed design. As a result, the suggested Vedic multiplier uses lesser area.

4. CONCLUSION

Using the Urdhva Tiryakbhyam sutra and the Carry Save Adder, the design of the 8 X 8 and 16 X 16 Vedic multipliers is explored in this paper. Xilinx Vivado is used to simulate and synthesize the proposed multiplier. Performance is compared with existing multipliers including Wallace tree, Array, and Booth multipliers. When compared, the results suggest that the proposed Vedic multiplier using the Urdhva Tiryakbhyam sutra with CSA gives better speed. It can be concluded that the proposed Vedic multiplier can be utilized to optimize speed and area and is more efficient than traditional multipliers.

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