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A Comparative Analysis on Parameters of Different Adder Topologies

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Abstract - *Due to their widespread use in the effective implementation of fundamental binary arithmetic, adders are an essential component in digital integrated design. A basic adder topology unquestionably requires higher working speeds, tolerable power consumption, and significantly less chip area. An extensive comparative examination of many modern adder topologies is provided in the current paper. The in-depth analysis of the adder that is described in this paper aims to make it easier to choose an adder topology for any digital design while balancing the trade-offs between area, propagation delay, and power dissipation. In this paper, a thorough comparison of four distinct adder topologies—the Ripple Carry Adder, Carry Save Adder, Carry Skip Adder, and Carry Select Adder—is made on basis of a number of design metrics and performance factors.*

Key Words: Ripple Carry Adder, Carry Skip adder , Carry save Adder, Carry select Adder, trade-off.

1.INTRODUCTION

The foundation of DSP applications are adders. Adders carry out addition, subtraction, multiplication, and division operations. According to Chen et al, the most common operation in digital signal processing is addition. The binary adder is the essential element of DSP, and the fundamental component of all binary adder structures is the full adder cell. A complete adder cell consists of three inputs (A, B, and Cin) and two outputs (sum S and Carry Cout). By cascading the full adder cells, the fundamental adder structure known as the "RCA" is produced. In addition to the A and B inputs, the carry produced at the nth bit is then delivered as the input to the n+1 full adder cell bit. The RCA is not just the slowest of all the adders, but it is also the simplest because the carry propagates from Least significant bit to Most significant bit. CSelA, CSA, CSkA are further varieties of carry adder structures. Because the carry ripples, ripple carry adders are the slowest adder structures. Keep looking The ahead adder uses carry propagate and carry produce signals to reduce carry propagation from right to left, however this increases the size, the number of gates, and the complexity of the system. The propagation time of carry is shortened in Carry Skip Adder by skipping over the group of adder stages and presents hardware and performance compromise.

1.1 Ripple carry adder

The full adder (FA) block cascade method is used to construct the ripple carry adder seen in Fig.1. When a carry (Cin) is originally provided at any point throughout the ripple carry, a complete adder adds two bin values A and B along with the carry. The starting bit of sum and carry-out will be a output that is obtained. The carry-in of the previous step is presented as the carry-out of the subsequent stage, and so on. The following is the formulae to calculate carry and sum.

$$\text{Sum} = A \oplus B \oplus \text{Cin} \quad (1)$$
$$\text{Carry} = A \,\&\, B \mid B \,\&\, \text{Cin} \mid A \,\&\, \text{Cin} \quad (2)$$

The latency in RCA varies based on the design and the number of bits employed

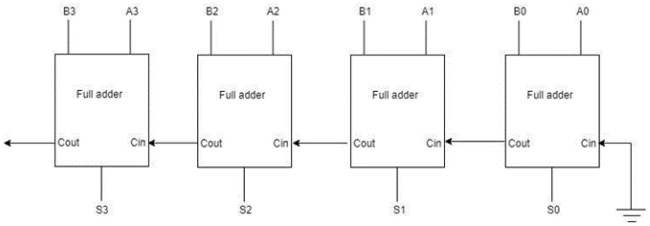

Fig.1: RCA

1.2 CSaA

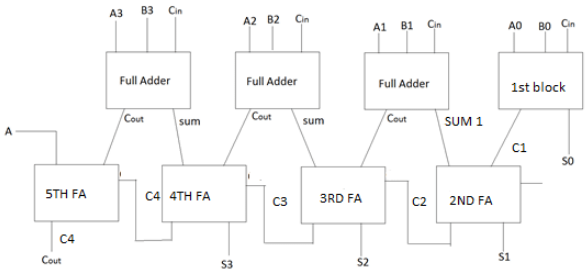

Fig.2: CSA

It was discovered to add decimal numbers via carry save addition. But the binary number system can also use it. When we wish to add more than two numbers, carry save addition is employed. The principle of carry save addition is to take the three values x, y, and z and convert it into 2 numbers carry and sum , wait until the very last step

before directly transmitting the carry information in carry save addition. The carry save strategy divides this procedure into two phases. First, calculate the amount while disregarding any carries: The final addition is then calculated by shifting the carry sequence C left by one position. An initial 0 is placed in front of the partial sum sequence S. (MSB). The two are then added together, and the resulting sum is computed, using a rca.

1.3 CSelA

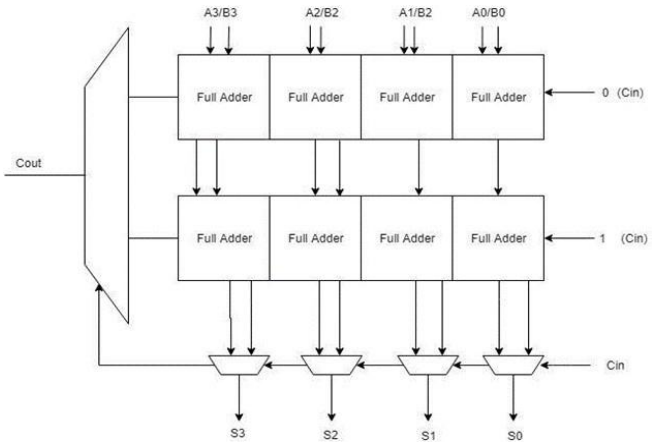

Fig.3: Carry Select Adder

A combinational logic circuit called a "Carry Select Adder" combines two n-bit parallel numbers and outputs the yield as the sum of the two 2-bit numbers combined with a carry bit. The only difference between this and the Ripple Carry Adder, which serves the identical purpose, is how they are designed. Compared to the Ripple Carry Adder, the Carry Select Adder produces fewer full adders. As shown in Fig. [3], a 4 bit Carry Select is made up of two parallel RCAs and multiplexers that provide the output carry and sum. The inputs are sent to the first set of RCA with input carry set to 0, and the identical set is supplied to the second set of RCA with input carry set to 1, allowing simultaneous computation to take place. A succession of muxes receive the total from the adders as inputs, and the next RCA to be taken into consideration is determined by the FA's carry. The output carry follows a similar procedure. CSIA is the most advanced adder among all in terms of area and power and has a very short delay.

1.2 CSkA

Carry propagation is skipped to position I in the carry skip adder without waiting for rippling, which speeds up execution. By skipping over clusters of adjacent adder stages, a CSkA shortens the carry-propagation time. While the CLA technique typically outperforms the CSkA in terms of speed, the CSkA requires less chip space and uses less power. Stages are broken down into r-bit blocks of a simple carry scheme to create a carry-skip adder. Carry skip logic is introduced to each block to decide whether carry-in can be moved directly to the next block. A ripple carry adder is used within each block to produce the total and carry out bit. For block propagation and block production, each block generates a signal.

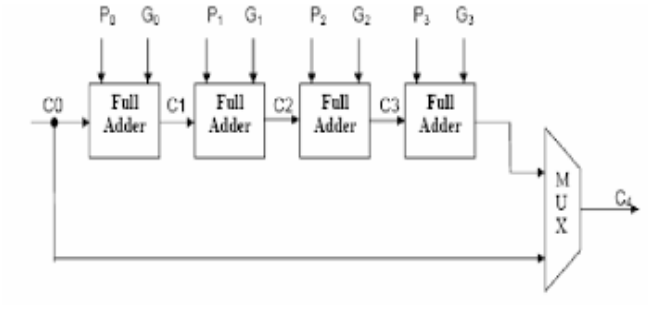

Fig.4: CSkA

The Cout signal serves as the block generate signal when a block's Cin signal is set to zero. As a result, a r bit AND gate is also used to form the block propagate signal. The block generates and spreads signals that deliver input to the block after it.

2 PERFORMANCE ANALYSIS

Table-1: The Adder Topologies' Associated Power Dissipation

Topology	Pd (µW)
RCA	0.502
CSkA	0.602
CSA	0.603
CSelA	0.952

Table-2: The Adder Topologies' Associated Delay

Topology	Delay(ns)
RCA	18.771
CSkA	18.598
CSA	18.564
CSelA	16.816

Table-3: The Adder Topologies' Associated Area

Topology	Area (µm²)
RCA	837.71
CSkA	2232.22
CSA	1234.25
CSelA	3097.89

Table-4: The Adder Topologies' Associated Power delay product

Topology	Power delay product (watt. sec)
RCA	9.42 e -15
CSkA	11.195 e -15
CSA	11.194 e -15
CSelA	16 e -15

3. SUMMARY

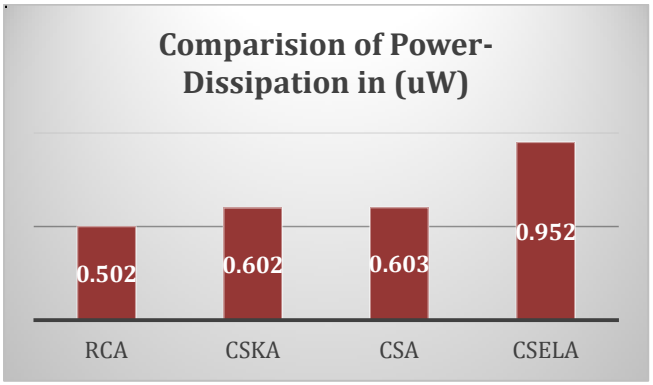

Fig.5: Comparison of PD

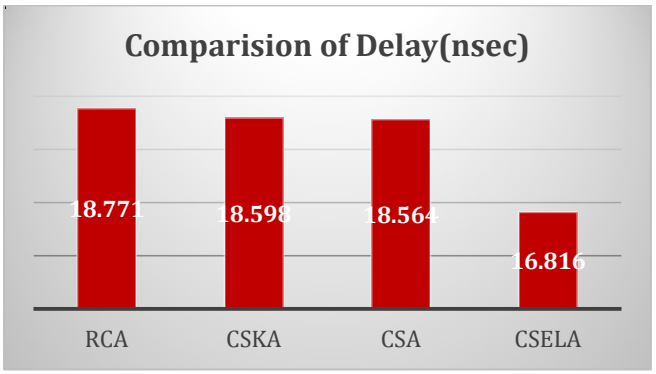

Fig.6: Comparison of Delay

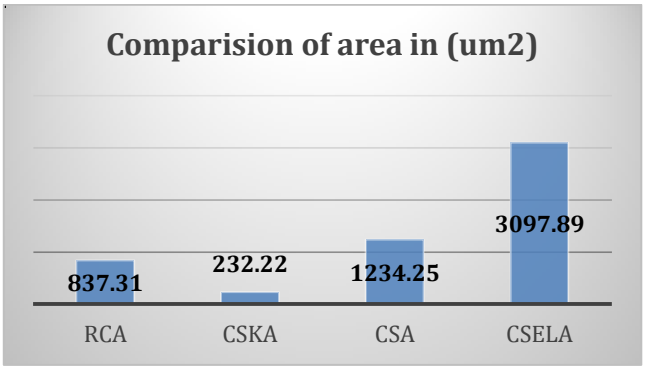

Fig.7: Comparison of area

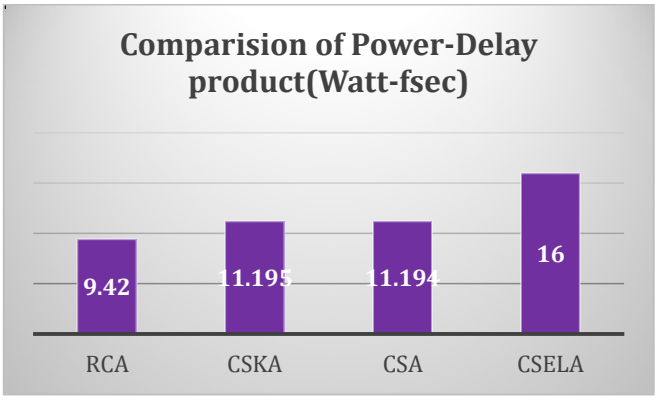

Fig.8: Comparison of power-delay product

The comparison of 4 different adders, namely the RCA, CSkA, CSA, and CSelA is the important concern in this paper. These adders were chosen for comparison because, according to the specification, they are often used in many applications. In order to simulate the operation of adders and multipliers in digital signal processing applications, the platform Xilinx uses the Verilog Language. The results of the analysis and comparison of the adders are tabulated above.

CSelA consumes less space than other adders overall. Because space is one among the factors that affects how complex a circuit is, RCA, CSKA, and CSA have low area usage and little variations. The amount of power used by a system has a significant impact on how productive it is as well. According to the adders taken into account, CSelA consumes more power (0.952uW), but RCA comes out as the adder with the lowest power consumption (0.502uW). In the current situation, the processing speed is taken into account while evaluating the system performance.

4. CONCLUSIONS

The area, power, and delay are the three primary metrics used in this article to compare various adders. Out all the adders selected, Carry Select Adder, a rapid adder, offers the best outcome in terms of latency. The Ripple carry

adder was shown to use the least amount of power in this study. The preferred adder varies depending on the application; for example, when space is limited and latency is not the most important factor, the carry select adder will be recommended. When the limitations are expanded from speed to power and area, the work's importance becomes apparent.

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