International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 09 Issue: 10 | Oct 2022 www.irjet.net p-ISSN: 2395-0072

# Area Efficient 9/7 Wavelet Coefficient based 2-D DWT using Modified CSLA Technique

**Megha Chaturvedi[1], Prof. Gurpreet Singh[2]**

[1] *Research Scholar, Trinity Institute of Technology & Research, Bhopal, India*
[2] *Professor Electronics' & Communication Dept., Trinity Institute of Technology & Research, Bhopal, India*

---

**Abstract -** *The DWT is expressed in a generalized form know as discrete wavelet transform which analyzes both the low and high sub bands at every level of breakdown with equal priority. A pragmatic approach to signal processing is provided by the DWT mathematical technique. It is frequently utilized in many signal and image processing applications because of its many beneficial qualities, such as adaptive time-frequency window, decreased aliasing distortion, and efficient computing complexity. In order to compress images and videos, 2-D DWT is frequently utilized. But in some DWT architectures, flipping approach adds considerable design complexity. In order to give multiplier-less implementation and ensure that our suggested work would function for every bit, we have included the BK adder and MDA approach. In comparison to the previous approach, the suggested MDA and MCSLA-based 2-D DWT algorithm exhibits good performance. The suggested architecture for DWT implementation minimizes the maximum combinational path delay while also reducing chip size and computation time.*

***Key Words***: VHDL Simulation, 2-D DWT, MDA, Low-pass Sub-band (LPSB), High-pass Sub-band (HPSB)

## 1. INTRODUCTION

Engineering professionals choose digital signal processing methods based on the characteristics of the signal being studied. The two main methods utilized commonly for signal analysis are frequency-based and time-frequency-based methods. A stationary signal is analyzed using the frequency-based method (FBT), while non-stationary signals are typically analyzed using time-frequency techniques (TFT), such as the short time Fourier transform (STFT), wavelet transform, etc. Although no information is obtained in the time domain, the FBT offers energy information of the function in the frequency domain. A musical note or a vehicle's noises are examples of non-stationary signals from which the TFT captures the transient properties and represents them in a time-frequency map for signal analysis. [1, 2].

Over the years wavelet transform has emerged as a predominant tool for time-frequency decomposition of a signal. Wavelet is designed especially to study the non-stationary data, and due to its generality and accurate results, it has become useful in a number of areas. For a non-stationary signal, the frequency content at a particular point in time is different from the frequency content at another point, e.g., a sudden transient [3]. The Fourier transform is not able to specify accurately at what point in time the transient occurs because the Fourier bases are sinusoids that are infinite in extent and can give information only based on the entire duration of the signal. Hence, the Fourier bases are not able to localize the important events of the signal. On the contrary, wavelet has bases of finite duration, and this property enables it to identify and locate in time the important events in the signal which can be used to differentiate one signal from the other efficiently [4, 5].

Wavelet analysis allows researchers to isolate and manipulate the specific type of in formation hidden in the data, similar to the human ear picking the sound of the flute in a symphony. A diverse variety of wavelets can be used to analyze a signal, the type of wavelet to be used depends on the application. Wavelet is found in different branches from the signal analysis to the problems in engineering, physics, and mathematics. In the signal processing application, wavelet is mainly used in analyzing the non-stationary signals to provide the time-frequency information of an important transient [6]. In the bio-medical engineering, earth or ocean engineering the transient always carry a significant amount of information for the respective domain. The wavelet transform is found to be particularly useful for analyzing the signals that are considered to be aperiodic and noisy. The ability to analyze a signal distinctly both in time and frequency simultaneously has set wavelet transform apart from the STFT. Hence, wavelet transform is used to investigate a variety of physical phenomena such as climate change analysis, heart monitoring, seismic signal de-noising, astronomical image de-noising, video and image compression [7, 8].

## 2. DISCRETE WAVELET TRANSFORM

The history of DWT goes back to the year 1976 when a technique was invented by Croiser, Galand, and Esteban to decompose the discrete time signals. In the same year, Flanagan, Crochiere, and Weber conducted a similar analysis on the voice signal. The technique was named as sub-band coding. Burt developed a method known as pyramidal coding in 1983 that is comparable to sub-band coding, sometimes referred to as multi-resolution analysis. The pyramidal coding system still had redundant information that might be removed. By removing the redundant code from the

pyramidal coding in 1989, Vetterli and Le Gall improved the sub-band coding [9]. The DWT, when compared with the CWT is considerably easier to develop and implement. Although the CWT can be discretized and computed for DWT, the accurate discrete transform is not obtained. The information provided by this sampled version of the CWT is highly redundant. On the other hand, analyzing this redundant information takes a lot of time and energy. The DWT, on the other hand, speeds up processing while still extracting enough usable data from the signal for analysis and synthesis. The DWT decomposes the input spectrum into two sub-bands, namely the high-pass sub band and the low-pass sub-band. A low-pass filter is used to filter the input signal to produce a low-pass sub-band, while a high-pass filter is used to produce a high-pass sub-band [10]. A finite impulse response (FIR) filter with a short length is used to create the low-pass and high-pass filters. This pair of low-pass and high-pass filter form a quadrature mirror filter (QMF) for the perfect signal reconstruction. The computation of the DWT using low pass and high-pass filters is performed either by the convolution scheme or lifting scheme [11].

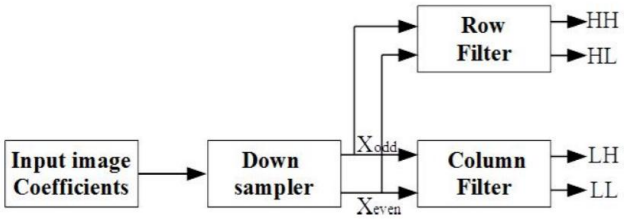


**Fig -1**: Two Level Diagram of Discrete Wavelet Transform

## 3. PROPOSED ARCHITECTURE

Particular focus is placed on system performance and cost in digital systems. Effective performance typically comes with a larger price cost. However, with a moderate increase in the hardware, better performance can be obtained. In the course of a computation, addition and multiplication are the fundamental operations that are performed frequently. The speed with which these operations are performed has a great impact on the overall performance of the digital system. Since the beginning of the digital computers, many fast algorithms for the basic arithmetic operations have been developed and implemented [12, 13].

There has been continuous research and development towards the newer algorithms. The main reason for the emerging algorithms is the rapid change in the technology used to implement these arithmetic operations. Besides the dependence on the technology used to implement the algorithm, it is the unique feature of the algorithm that affects the performance of the arithmetic operator [14].

In this stream graph, the double information is connected to the serial in serial out register. In the DWT design, all whole numbers are related to the twofold frame. The word length of two pieces of information, in this case 3 down to 0, means that the range of the information is from 0 to 15.

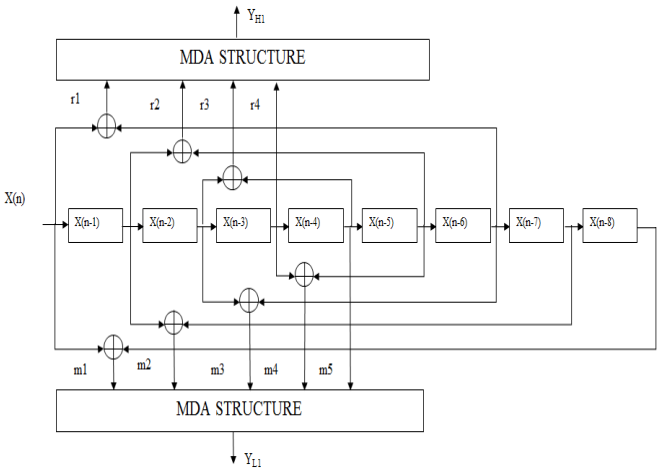


**Fig -2**: Block Diagram of 9/7 Wavelet Coefficient based Discrete Wavelet Transform

If takes the LPS coefficients $h_0$, $h_1$, $h_2$, $h_3$, and $h_4$ multiply by $u_1$, $u_2$, $u_3$, $u_4$ and $u_5$ then multiplier-less 1-D DWT LPS output is

$$Y_{LPS} = \begin{bmatrix} h_0 & h_1 & h_2 & h_3 & h_4 \end{bmatrix} \bullet \begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ u_4 \\ u_5 \end{bmatrix}$$

Where,

$$u_1 = X(n) + X(n-8)$$

$$u_2 = X(n-1) + X(n-7)$$

$$u_3 = X(n-2) + X(n-6)$$

$$u_4 = X(n-3) + X(n-5)$$

$$u_5 = X(n-4)$$

$$Y_{LPS} = \begin{bmatrix} 77 & 34 & -10 & -2 & 3 \end{bmatrix} \bullet \begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ u_4 \\ u_5 \end{bmatrix}$$

So,

$$Y_{LPS} = [01001101 \;\; 00100010 \;\; 11110110 \;\; 11111110 \;\; 00000011] \bullet \begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ u_4 \\ u_5 \end{bmatrix}$$

All the LPS coefficient arranges down to up is below:

$$Y_H = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 \\ 0 & 1 & 1 & 1 & 1 \\ 1 & 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 1 & 0 \end{bmatrix} \bullet \begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ u_4 \\ u_5 \end{bmatrix}$$

All rows pass through look up table and replace LPS coefficient to input

$$Y_H = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 \\ 0 & 1 & 1 & 1 & 1 \\ 1 & 0 & 1 & 1 & 0 \\ 1 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 1 & 0 \\ 0 & 1 & 1 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 1 & 0 \end{bmatrix} \bullet \begin{bmatrix} u_1 \\ u_2 \\ u_3 \\ u_4 \\ u_5 \end{bmatrix} = \begin{bmatrix} u_1 + u_5 \\ u_2 + u_3 + u_4 + u_5 \\ u_1 + u_3 + u_4 \\ u_1 + u_4 \\ u_3 + u_4 \\ u_2 + u_3 + u_4 \\ u_1 + u_3 + u_4 \\ u_3 + u_4 \end{bmatrix}$$

## 4. MODIFIED CARRY SELECT ADDER

If a XOR gate is realized with less number of gates in AOI logic, then there is a chance for reduction in the area and power consumption. Hence, we used alternative expression/approach for the XOR gate which is shown in equation 1.

$$A \bigoplus B = (\overline{A \bullet B}) \bullet (A|B)$$

**Table -1:** The size of RCA and CSLA groups are used in 4-, 8-, 16-, 32- and 64-bit conventional sqrt CSLA adder

| Size of the CSLA Adder(bit) | RCA (bit) | CSLA (bit) |
|---|---|---|
| 4 | 2 | 2 |
| 8 | 2 | 2 and 4 |
| 16 | 2 | 2, 3, 4 and 5 |
| 32 | 2 | 2, 3, 4, 6, 7 and 8 |
| 64 | 2 | 2, 3, 4, 5, 6, 7, 8, 8, 9 and 10 |

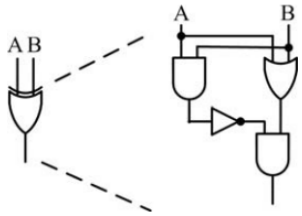


**Fig -3**: A 2-input Modified XOR

The XOR gate is shown in Fig. 3, we call it as modified XOR gate. The advantage of the modified XOR gate is needed only four and nine gates for implementing HA and FA respectively. Furthermore, a modified XOR can act as HA. In the conventional XOR gate, NOT gates are followed by AND gates and, finally, OR gate is presented but in the modified XOR gate AND and OR gates are presented in the first stage. Consequently, an additional AND gate is not required to find carry of HA. Further, only four gates are needed to implement the modified XOR gate. This modified XOR gate was used inside RCA and CSLA to reduce the gate count which leads to reduction in area as well as reduction in the power consumption of the CSLA. Moreover, the design is quite easy because the conventional XOR gate is replaced by the modified XOR gate.

## 5. SIMULATION RESULT

This section displays the results of the 2-D DWT's synthesis utilizing the MDA and MCSLA techniques. The view technology schematic (VTS), register transfer level (RTL) view, hardware and synthesis utilization, VHDL test bench, and comparison of the 2-D DWT design for existing architecture are all explained in this section. Shift registers, various bits of the BK adder, and the multiplier-less MDA approach make up the 2-D DWT architecture.

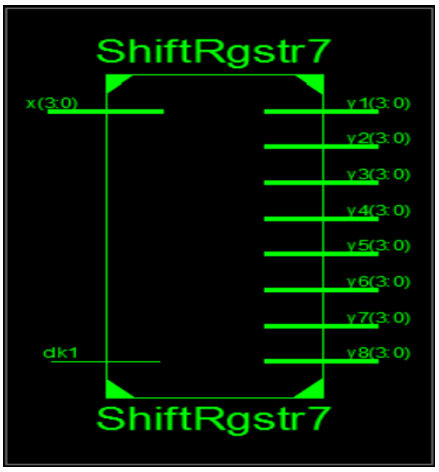


**Fig -4**: VTS for 4-bit SR

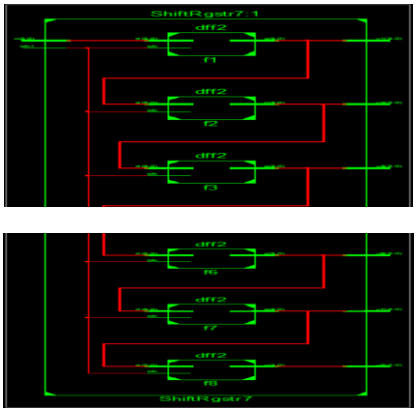

**Fig -5**: RTL for 4-bit SR

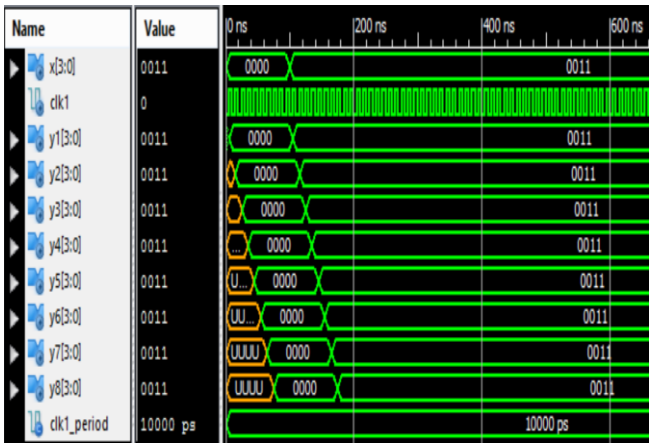


**Fig -6**: VHDL Test-bench in Shift Register

Figure 7 depicts the second level DWT in RTL. It includes every element of a 2-D DWT. It includes every shift register, D-flip flop, and MCSLA. The view technology is dependent on this RTL schematic.

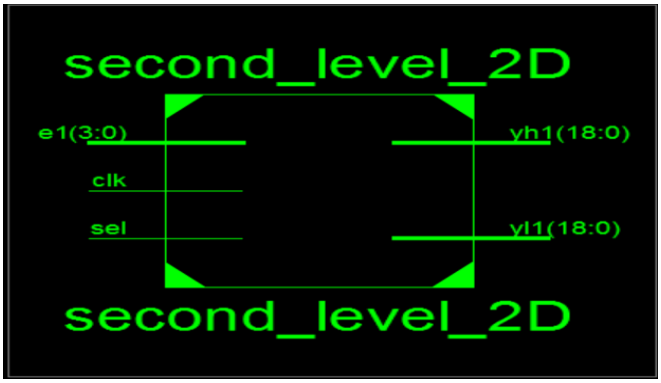


**Fig -7**: VTS for 2-D DWT

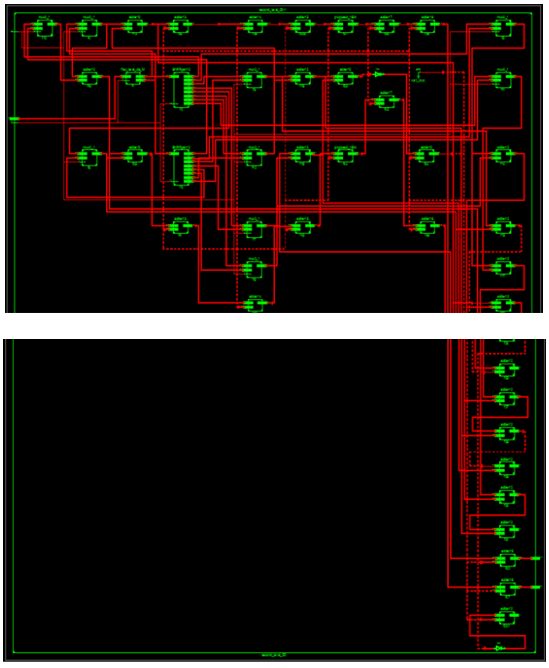

**Fig -8**: RTL for 2-D DWT

This figure 9 shows the waveform of the second level DWT. Here the input is given as '0011' and the output finally comes for both the filters. 'yh' is '1111101000000000000' for high pass filter output and 'yl' is '0000011000000000000' for low pass filter output.

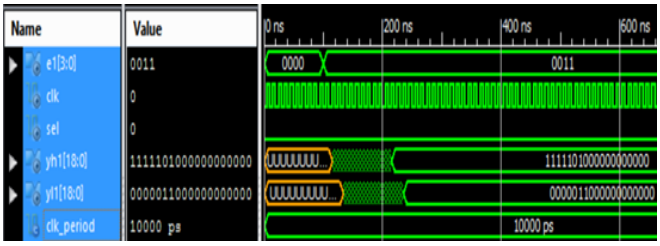


**Fig -9**: VHDL Test-bench in 2-D DWT

**Table -2:** Hardware Utilization for 2-D DWT Architecture

| | |
|---|---|
| Select Device | 4vfx12sf363-12 |
| Register | 224 |
| Flip Flop | 224 |
| XOR Gate | 778 |
| Memory | 286452 Kilobytes |
| Real Time to XST | 17.00 secs |
| CPU to XST | 16.93 secs |

## 5. CONCLUSION

For this MDA technique is used which provides approach for multiplier less implementation. It contains adder, shift registers and free of multiplier.

Finally we have designed the 1-D and 2-D DWT using MCSLA and MDA technique which provide better efficiency and shows better results than the previous design.

DWT has been an important technique of multimedia applications. This is not only the key algorithm of signal processing, but has also led to revolutions in image and video coding algorithms. There are many DWT architectures of flipping type, folded type and pipeline architecture for signal transform. Each structure has its own advantages and disadvantages. However, an efficient architecture design of DWT in JPEG 2000 is an important area of research to explore.

## REFERENCES

[1] Jhilam Jana, Sayan Tripathi, Ritesh Sur Chowdhury, Akash Bhattacharya and Jaydeb Bhaumik, "An Area Efficient VLSI Architecture for 1-D and 2-D Discrete Wavelet Transform (DWT) and Inverse Discrete Wavelet Transform (IDWT)", Devices for Integrated Circuit, IEEE 2021.

[2] Zhang, W., Wu, C., Zhang, P. and Liu, Y., "An Internal Folded Hardware-Efficient Architecture for Lifting-Based Multi-Level 2-D 9/7 DWT", 2019, Applied Sciences, 9(21), p.4635.

[3] Samit Kumar Dubey, Arvind Kumar Kourav and Shilpi Sharma, "High Speed 2-D Discrete Wavelet Transform using Distributed Arithmetic and Kogge Stone Adder Technique", International Conference on Communication and Signal Processing, April 6-8, 2017, India.

[4] Rakesh Biswas, Siddarth Reddy Malreddy and Swapna Banerjee, "A High Precision-Low Area Unified Architecture for Lossy and Lossless 3D Multi-Level Discrete Wavelet Transform", IEEE Transactions on Circuits and Systems for Video Technology, Vol. 45, No. 5, pp. 01-11, May 2017.

[5] Mamatha I, Shikha Tripathi and Sudarshan TSB, "Pipelined Architecture for Filter Bank based 1-D DWT", International Conference on Signal Processing and Integrated Networks (SPIN), pp. 47-52, May 2016.

[6] Maurizio Martin and Guido Masera, Massimo Ruo Roch and Gianluca Piccinini, "Result-Biased Distributed-Arithmetic-Based Filter Architectures for Approximately Computing the DWT", IEEE Transactions on Circuits and Systems—I: Regular Papers, Vol. 62, No. 8, pp. 2103-2113, August 2015.

[7] Basant Kumar Mohanty, Pramod Kumar Meher, "Memory-Efficient High- Speed Convolution-based Generic Structure for Multilevel 2-D DWT", IEEE transactions on Circuits, Systems for Video Technology, Vol. 23, No. 2, pp. 353-363, February 2013.

[8] Basant K. Mohanty, Anurag Mahajan, Pramod K. Meher, "Area- and Power-Efficient Architecture for High-Throughput Implementation of Lifting 2-DDWT", IEEE Transactions on Circuits and Systems-II: Express Briefs, Vol.59, No.7, pp. 434-438, July 2012.

[9] Chengjun Zhang, Chunyan Wang, M. Omair Ahmad, "A Pipeline VLSI Architecture for High-Speed Computation of the 1-D Discrete Wavelet Transform", IEEE transactions on Circuits and Systems-I; Regular Papers, Vol.57, No.10, pp. 2729-2740, October 2010.

[10] Zhang, Chengjun, Chunyan Wang, and M. Omair Ahmad, "A pipeline VLSI architecture for high-speed computation of the 1-D discrete wavelet transform", IEEE Transactions on Circuits and Systems I: Regular Papers, Vol.57, No. 10,pp: pp. 2729-2740, October 2010.

[11] S. M. M. Rahman, M. O. Ahmad, and M. N. S. Swamy, "A New Statistical Detector for DWT-Based Additive Image Watermarking using the Gauss-Hermit Expansion," IEEE Transactions Image Processing, Vol. 18, No. 8, pp. 1782–1796, August 2009.

[12] P. K. Meher, B. K. Mohanty and J. C. Patra, "Hardware-Efficient Systolic-Like Modula Design for Two-Dimensional Discrete Wavelet Transform", IEEE Transactions on Circuits and Systems—Ii: Express Briefs, Vol. 55, No. 2, pp. 1021-1029, February 2008.

[13] Chao Cheng, Keshab K. Parhi, "High-Speed VLSI Implementation of 2-D Discrete Wavelet Transform", IEEE Transactions on Signal Processing, Vol.56, No.1, pp. 393-403, January 2008.

[14] C. C. Cheng, C.-T. Huang, C.-Y. Cheng, C.-Jr.Lian and L.-G. Chen, "On-chip Memory Optimization scheme for VLSI Implementation of Line-Based 2-D Discrete Wavelet Transform," IEEE Transactions on circuit and System for Video Technology, vol.17,no.7, pp. 814-822, July 2007.

[15] M. Martina, and G. Masera,"Multiplier less, folded 9/7-5/3 wavelet VLSI Architecture, "IEEE Transactions on Circuits and System, Express Brief Vol. 54, No. 9, pp. 770- 774, September 2007.