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A Self-Balancing Switched Capacitor Multilevel Inverter Structure with Six-fold Gain Factor

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Abstract - In this article, a novel self-balancing switched capacitor multilevel inverter structure with six-fold gain factor is proposed. This inverter's design calls for a single DC supply, 3 capacitors, and 14 switches to generate an output voltage with 13 levels. The power storage mechanism used by this inverter construction allows it to automatically balance itself by charging and discharging capacitors in series and parallel with a DC source. The proposed inverter does not require a back-end H-bridge, therefore each switch is not subjected to as much voltage stress as under a peak load. The result is a striking reduction in Total Blocking Voltage (TBV) from $88V_{dc}$ to $33V_{dc}$ and Maximum Blocking Voltage (MBV) from $6V_{dc}$ to $4V_{dc}$ for similar topologies and thus makes it a preferable choice for renewable energy applications. The proposed SBSCI topology modes of operation, capacitor design and control strategy are delineated. A thorough comparison with existing literature demonstrates the proposed topology's affordability and compactness. The performance and viability of the suggested topology are validated using the MATLAB/SIMULINK software.

***Key Words*: Maximum Blocking Voltage (MBV), Self-Balancing Mechanism, Total Cost Function (TCF), Voltage gain, Self-Balancing Switched Capacitor Inverter (SBSCI).**

1.INTRODUCTION

Due to their better waveform nature and reduced switching voltage stress of each power switch, multilevel dc-ac power converters are currently the most widely used solution in industries for high-power applications with medium voltage levels. It significantly benefits applications requiring medium voltage and high power, such as those for electric vehicles and renewable energy sources. [1],[2]. MLIs have gained popularity because to their intrinsic advantages, which include lowering switching frequency, lowering switching stress, and improving voltage and current waveforms by decreasing harmonics [3]. Researchers from all around the world are paying close attention to the neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) inverters, which have already achieved commercial viability [4]. Although the MLIs being advantageous it also suffers with some flaws like capacitors balancing issues and requirement of complex circuits in case of flying capacitor inverter (FC) and Neutral point clamped inverter (NPC). The cascaded H-bridge inverter (CHB) necessitates numerous DC supply's, increasing the system's size and cost. All of these conventional MLIs have one thing in common: they aren't capable of raising voltage. To address this issue for the researchers, switching capacitors are the best option. The switching capacitor topology-based MLI has become more prevalent in recent years [5].

Up until this point, different switched capacitor topologies have mainly been used in single-phase systems, with the most popular variety being created by stacking switched capacitor topologies with an inverting H-bridge. The ac output voltage is produced by the H-bridge on the end side, while the circuit on the front side produces a range of dc levels. A traditional series/parallel switching capacitor dc/dc multilevel circuit, as well as its streamlined variant and an updated structure, are employed to power the H-bridge [9]. When an H-bridge is used, the switches are under more voltage stress. By using a different commonly utilized integrated circuit created by sandwiching a switching capacitor based multilevel converter circuit between two half bridges, it is possible to get beyond the restrictions of these topologies [6-8]. In [10], a modular switched capacitor topology was analyzed while keeping all of the benefits of switched capacitor topologies. Although [9-10] uses single dc source to attain 13-levels at the output but it provides with high switching stress across the switches that limits the topology to work for low power applications. Some topologies suffer with the least gain. However, some topologies that aim to increase high voltage levels are unable to reduce switching stress [10]. Some switched capacitor topologies requires auxiliary H-bridge for polarity generation [11]. The single source topology requires complex algorithms and voltage balancing auxiliary circuits in order to attain high power density. This causes the system's size and cost to grow. The literature analysis mentioned above provides room to develop a novel topology that possesses the following appealing qualities. An SBSCI topology with 13 levels and a six-fold gain factor is described in this article.

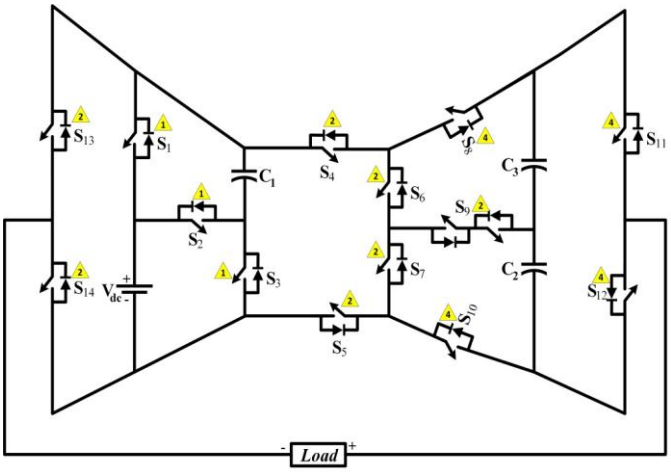

Fig1: Proposed SBSCI topology

Some of the things that make it unique include the following:

- ✓ Voltages in a capacitor have a self-balancing tendency.
- ✓ Maximum Blocking Voltage across each switch is less that peak load voltage
- ✓ It employs 14 switches and three capacitors in a 1:2:2 ratios to generate an output voltage waveform with 13 levels.
- ✓ It has the capacity to increase the input voltage.
- ✓ The suggested structure responds to dynamic variations in load very well.
- ✓ This architecture's decreased switching stress makes it appropriate for medium and high power applications.

The arrangement of this document is as follows: the second segment describes the topology architecture and its operation. The modulation scheme and capacitance analysis are shown in Segment 3. The comparison of the suggested design with the existing designs is evaluated in segment 4. Segment 5 displays the findings of the planned topology validation and followed by conclusion in Segment 6.

2. PROPOSED TOPOLOGY DESIGN & OPERATING PRINCIPLE

2.1 Circuit explanation:

The proposed innovative topology schematic diagram along with maximum blocking voltage along each switch can be seen in Fig1. It consists of 3 capacitors (C_1, C_2, and C_3), 14 switches (S_1–S_{14}), and a single DC source (V_{dc}). Out of 14 switches, S_9 is the only one that is bidirectional. The switches maximum blocking voltage is lesser than the load maximum voltage. And the suggested design the capacitors get charged and discharged in the ratio of$C_1 : C_2 : C_3 = 1v_{dc} : 2v_{dc} : 2v_{dc}$. A battery or any other renewable energy source could serve as the intended topology DC power source. Switching pairs that are complementary to one another include (S_2S_3), (S_8S_{10}), ($S_{11}S_{12}$), and ($S_{13}S_{14}$).

2.2 Operating Principle:

By assuming that each element in the suggested switched capacitor architecture is perfect, the analysis that follows is made simpler. As shown in Tab1 and Fig2, the proposed topology operation may be explained by thirteen states with distinct switching sequence that results in 13 levels at output. Tab1 contains a list of the suggested topology's legal switching combinations. In Tab1, the on and off states of the switches are indicated by "0" and "1," respectively. The symbols for the capacitor's charging, discharging, and idle states are ↑, ↓, –.

State1. $v_{dc} = 0$

The output voltage $v_{dc} = 0$ can be achieved by activating switches S_5, S_{10}, S_{12}, S_{14}. Here Capacitor C_1=C_2=C_3 remains idle (-). It shown in the Fig2(G).

State2. $v_{dc} = \pm 1$

The output voltage $v_{dc} = \pm 1$ can be achieved by activating switches S_1, S_3, S_4, S_8, S_{11}, S_{14} for positive level and shown in Fig2(F) and capacitor C_1 gets charged. And by activating switches S_1, S_3, S_5, S_{10}, S_{12}, S_{13} for negative level and shown in Fig2(H) and capacitor C_1 gets charged.

State3. $v_{dc} = \pm 2$

The output voltage $v_{dc} = \pm 2$ can be achieved by activating switches S_2, S_4, S_5, S_7, S_8, S_9, S_{11}, S_{14} for positive level and shown in Fig2(E) and capacitor C_3 gets charged and capacitor C_1 gets discharged. And by activating switches S_2, S_4, S_5, S_6, S_9, S_{10}, S_{12}, S_{13} for negative level and shown in Fig2(I) and capacitor C_1 gets discharged and C_2 gets charged.

State4. $v_{dc} = \pm 3$

The output voltage $v_{dc} = \pm 3$ can be achieved by activating switches S_1, S_3, S_4, S_6, S_9, S_{11}, S_{14} for positive level and shown

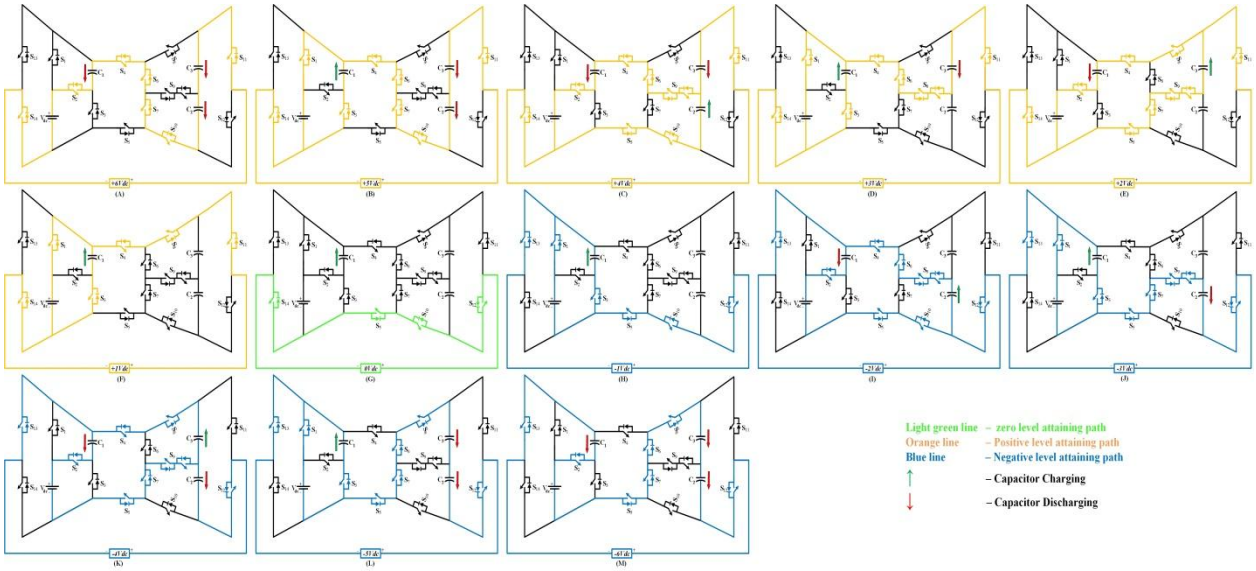

Fig2: Positive and Negative half-cycle operating states along with zero state

in Fig2(D) and capacitor C_3 gets discharged and capacitor C_1 gets charged. And by activating switches S_1, S_3, S_5, S_7, S_9, S_{12}, S_{13} for negative level and shown in Fig2(J) and capacitor C_2 gets discharged and C_1 gets charged.

State5. $v_{dc} = \pm 4$

The output voltage $v_{dc} = \pm 4$ can be achieved by activating switches S_2, S_4, S_5, S_6, S_9, S_{10}, S_{11}, S_{14} for positive level and shown in Fig2(C) and capacitor C_1 ,C_3 gets discharged and capacitor C_2 gets charged. And by activating switches S_2, S_4, S_5, S_7, S_8, S_9, S_{12}, S_{13} for negative level and shown in Fig2(K)

and capacitor C_1, C_2 gets discharged and C_3 gets charged.

State6. $v_{dc} = \pm 5$

The output voltage $v_{dc} = \pm 5$ can be achieved by activating switches S_1, S_3, S_4, S_6, S_7, S_{10}, S_{11}, S_{14} for positive level and shown in Fig2(B) and capacitor C_2 ,C_3 gets discharged and capacitor C_1 gets charged. And by activating switches S_1, S_3, S_5, S_6, S_7, S_8, S_{12}, S_{13} for negative level and shown in Fig2(L) and capacitor C_2, C_3 gets discharged and C_1 gets charged.

State7. $v_{dc} = \pm 6$

The output voltage $v_{dc} = \pm 6$ can be achieved by activating switches S_2, S_4, S_6, S_7, S_{10}, S_{11}, S_{14} for positive level and shown in Fig2(A) and capacitor C_1 ,C_2 ,C_3 gets discharged. And by activating switches S_2, S_5, S_6, S_7, S_8, S_{12}, S_{13} for negative level and shown in Fig2(M) and capacitor C_1 ,C_2, C_3 gets discharged.

2.3 Capacitor voltage Balancing Mechanism:

This subsection demonstrates the self-balancing mechanism of voltage across the capacitors. The most crucial component of the suggested switching capacitor architecture is the trio of the capacitors C_1, C_2, and C_3, which charge when arranged in parallel to the input supply. During the voltage level $\pm 1v_{dc}$, $\pm 3v_{dc}$, $\pm 5v_{dc}$ the capacitor C_1 gets charged to v_{dc}. During the voltage level C_2 $+4v_{dc}$, $-2v_{dc}$ and charges to $2v_{dc}$ and during voltage level $-4v_{dc}$, $+2v_{dc}$ the capacitor C_3 charges to $2v_{dc}$. It is enlisted in Tab1 and depicted in Fig2. The capacitor C_1 gets arranged in series with source voltage to provide voltage level of $\pm 2v_{dc}$, $\pm 4v_{dc}$, $\pm 6v_{dc}$. At the same time the capacitor C_2 gets discharged to produce voltage level of $-3v_{dc}$, $-4v_{dc}$, $\pm 5v_{dc}$, $\pm 6v_{dc}$. And the capacitor C_3 gets discharged to produce voltage level of $+3v_{dc}$, $+4v_{dc}$, $\pm 5v_{dc}$, $\pm 6v_{dc}$. The capacitors naturally achieve self-balance using the series/parallel approach of charging and discharging them.

3. CAPACITANCE ANALYSIS & MODULATION SCHEME

3.1 Capacitance Analysis:

Designing a switched capacitor multilevel inverter requires careful consideration of the capacitors' capacitance. Because the effectiveness of the inverter is impacted by the voltage fluctuations in the capacitor. Losses will increase if the

Tab1: Proposed 13SBSCI Topology switching states

Switching States	Switches														Charging & Discharging of Capacitors		
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	S_{13}	S_{14}	C_1	C_2	C_3
$+6V_{dc}$	0	1	0	1	0	1	1	0	0	1	1	0	0	1	↓	↓	↓
$+5V_{dc}$	1	0	1	1	0	1	1	0	0	1	1	0	0	1	↑	↓	↓
$+4V_{dc}$	0	1	0	1	1	1	0	0	1	1	1	0	0	1	↓	↑	↓
$+3V_{dc}$	1	0	1	1	0	1	0	0	1	0	1	0	0	1	↑	–	↓
$+2V_{dc}$	0	1	0	1	1	0	1	1	1	0	1	0	0	1	↓	–	↑
$+1V_{dc}$	1	0	1	1	0	0	0	1	0	0	1	0	0	1	↑	–	–
0	0	0	0	0	1	0	0	0	0	1	0	0	0	1	–	–	–
$-1V_{dc}$	1	0	1	0	1	0	0	0	0	1	0	1	1	0	↑	–	–
$-2V_{dc}$	0	1	0	1	1	1	0	0	1	1	0	1	1	0	↓	↑	–
$-3V_{dc}$	1	0	1	0	1	0	1	0	1	0	0	1	1	0	↑	↓	–
$-4V_{dc}$	0	1	0	1	1	0	1	1	1	0	0	1	1	0	↓	↓	↑
$-5V_{dc}$	1	0	1	0	1	1	1	1	0	0	0	1	1	0	↑	↓	↓
$-6V_{dc}$	0	1	0	0	1	1	1	1	0	0	0	1	1	0	↓	↓	↓

capacitor's voltage ripple is greater, and vice versa. The maximum discharging duration, maximum load current, and power factor angle are additional elements that affect a capacitor's discharge values. Consequently, the discharging quantity (Δq_c) of the capacitor is shown as

$$\Delta q_c = \int_{t_b}^{t_a} i_{max} \sin(2\pi f t - \emptyset)\, dt \qquad \text{equation 1}$$

Where I_{max} represents the highest load current, between the load voltage and current, there is a power factor angle (ϕ), the lower and upper bounds of each capacitor's discharging duration are (t_a-t_b), "f" indicates the fundamental frequency, ϕ be the power factor angle between v_{dc} and i_{max}, the longest discharging period of the capacitors C_1, C_2, and C_3 are $(t_2,t_9)(t_3,t_8)(t_3,t_8)$.

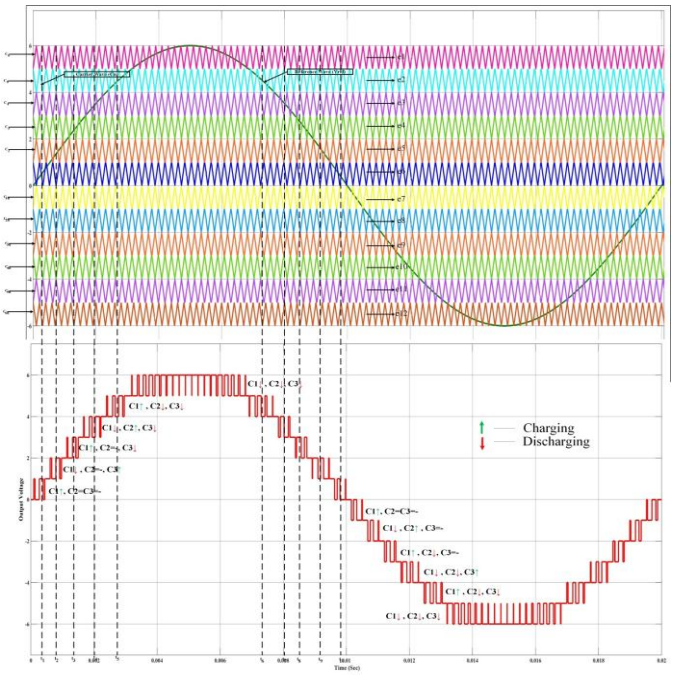

Fig3 States of charging and discharging of Capacitors along with modulation scheme for 13SBSCI topology

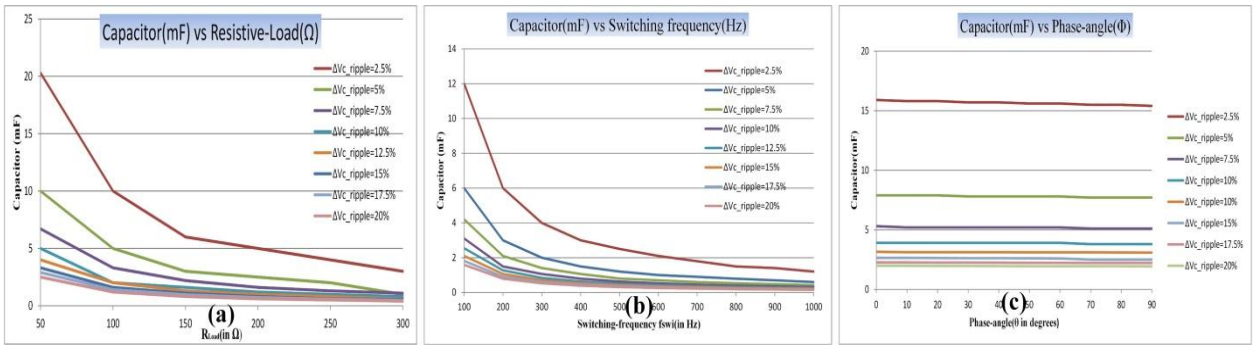

Fig4 Variation in capacitor value under various conditions

For the suggested 13-level topology t_1, t_2, t_3, t_4, t_5, t_6, t_7, t_8, t_9, t_{10} are evaluated with help of Fig3 as follows:

$$t_1 = \frac{\sin^{-1}(1/6)}{2\pi f}, t_2 = \frac{\sin^{-1}(1/3)}{2\pi f}, t_3 = \frac{\sin^{-1}(1/2)}{2\pi f}, t_4 = \frac{\sin^{-1}(2/3)}{2\pi f},$$
$$t_5 = \frac{\sin^{-1}(5/6)}{2\pi f}, t_6 = \frac{\pi - \sin^{-1}(5/6)}{2\pi f},$$

$$t_7 = \frac{\pi - \sin^{-1}(2/3)}{2\pi f}, t_8 = \frac{\pi - \sin^{-1}(1/2)}{2\pi f}, \quad \text{equation 2}$$
$$t_9 = \frac{\pi - \sin^{-1}(1/3)}{2\pi f}, t_{10} = \frac{\pi - \sin^{-1}(1/6)}{2\pi f}$$

If Δv_c percentage is the highest permitted voltage ripple, the ideal capacitance is given by

$$c_{opt} = \frac{\Delta q_c}{\Delta v_c * v_{dc}} \quad \text{equation 3}$$

The ideal capacitance value under the resistive load (RL) condition can be stated as

$$c_{opt} \geq \frac{8}{2 * \pi * 50 * R_L * \Delta v_c} \quad \text{equation 4}$$

It is obvious from equation (4) that the percentage of capacitor voltage ripple (Δv_c) for resistive loads (R_L) is inversely proportional to the magnitude of the ideal capacitor. In order to the size of capacitor will reduces as any one of these factors increases and it is depicted in Fig4(a)(b).

For an inductive load (RL), the ideal capacitance value can be stated as

$$c_{opt} \geq \frac{i_{max}}{2 * \pi * 50 * (\Delta v_c) * v_{dc}} [\cos(0.8481 - \emptyset) - \sin\emptyset] \quad \text{equation 5}$$

It is obvious from equation (5) that the capacitance value of an inductive load is proportional to phase angle depicted in the Fig4(c). By increasing the value of capacitance the phase angle gets increases. Therefore power factor, switching frequency, and load resistance should be selected in such a way that the value of capacitance is selected. Therefore capacitor ripples should be in permissible limit. For the proposed topology the capacitor values are C_1=3300µf, C_2=C_3=4700µf.

3.2. Modulation Scheme:

There are numerous control mechanisms utilized for multilevel inverters. In this article, a straightforward multicarrier level-shifted PWM has been employed. By comparing the signals from 12 carriers (Cn) (e_1, e_2,.....e_{12}) with a sinusoidal signal (V_{ref})., the switching pulse is determined. Each carrier's amplitude and frequency have the same peak to peak value. The modulation scheme for the proposed 13SBSCI is depicted in the Fig3.

4. COMPARITIVE ASSESSMENT

Capacitors ($N_{Capacitor}$), diodes (N_{Diodes}), drivers ($N_{Drivers}$), gain, maximum blocking voltage (MBV), switches, total standing voltage (TSV), and Total cost function (TCF) are compared to highlight the significance of the suggested 13SBSCI design. The findings of the comparison studies between the suggested 13SBSCI design and the existing topologies are displayed in TAB2. The comparisons used to assess the benefits of the suggested 13SBSCItopology primarily took into account the boosting ability, Total standing voltage (TSV), Maximum Blocking Voltage (MBV), and Total cost function (TCF). The Total Standing Voltage

TAB2 Comparative Assessment of 13SBSCI topology with current literatures

Reference	N_{Switch}	N_{Diode}	$N_{Capacitors}$	$N_{Drivers}$	$N_{Sources}$	Gain(G)	TSV	N_{level}	MBV	Cost Function
[6]	16	0	4	16	2	3	34	13	6	10.76
[7]	14	0	2	11	2	2	32	13	6	9.07
[8]	11	0	1	10	2	2	38	13	6	9.23
[9]	19	0	5	19	1	6	39	13	6	6.30
[10]	29	0	5	29	1	6	88	13	6	11.61
[11]	14	2	4	14	2	6	34	13	6	10.46
Proposed	14	0	3	14	1	6	33	13	4	4.92

(TSV) can be calculated as the summation of maximum voltage stress across the each individual switches. The cost function (CF) of an inverter is described as:

$$TCF = \frac{N_{Switches} + N_{Diodes} + N_{Capacitors} + N_{Drivers} + \beta(TSV)}{N_{Level}} * N_{Source} \quad \text{equation 6}$$

The weight factor, which is equal to the importance of switching components, is denoted by the symbol (β). TAB2 compares switched capacitor topologies with various voltage gains at the same voltage levels. The design cost of the inverters is increased by the topology [10]'s extensive use of semiconductor components, which also raises the overall standing voltage. On the other hand, there are fewer switches in the topologies [7] [8] that are put under more strain than the source voltage. To offset the output voltage rise by a factor of six, the total cost function (TCF) is high.

This is an important factor to take into account because the Maximum blocking voltage of the switch is six times larger in [6-11] designs. The required voltage level, according to [9][10], can only be reached employing several capacitors in its construction. The design described in [11] uses several diodes, which raises count of semiconductors usage and raises losses, which is another important concern. In some topologies [6-11] the maximum blocking voltage (MBV) is high which limits to low power applications. Fig5 depicts the comparison assessment of 13SBSCI topology with current literature in terms of component count in Fig5(a), Total cost function (TCF) and TBV in Fig5(b), and gain &MBV in Fig5(c).

5. RESULTS AND DISCUSSION

Using the values listed in TAB3, MATLAB/Simulink tools have been utilized to simulate the proposed 13SBSCI design. In dynamic conditions, the proposed switching capacitor topology was tested. Inductive-resistive load configuration output waveform is shown in Fig. 6.

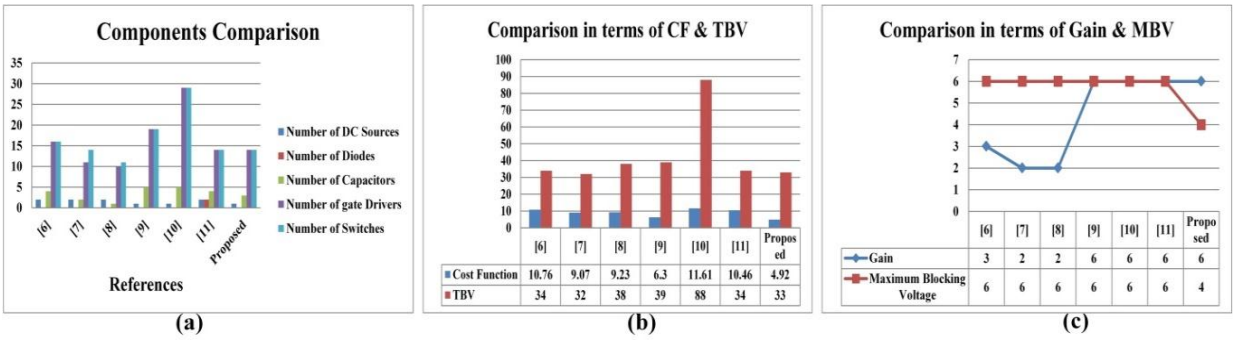

Fig5 Comparative Assessment of 13SBSCI topology with current literatures

TAB3 Parameters for simulation

Parameters	Specification
Source voltage	40V
Switching-Frequency	2500 Hz, 5000 Hz
RL Load (R_0+R_L)	40Ω+50mH, 40Ω, 40Ω+150mH
Fundamental frequency f_o	50Hz
Capacitors C_1 ,C_2 ,C_3	3300uF, 4700uF, 4700uF
Power Switches	IGBT
Voltage ripple (Δv_c)	5%

It is discovered that the load voltage is six times more than the supply voltage when it reaches its maximum. And the waveform of the output voltage in Fig6 illustrates that the design is attached at a load 40Ω+50mH. In this waveform the capacitor C_1 charges to 40V as source voltage and capacitors C_2, C_3 charges to 80V from where natural voltage balancing process will occurs under steady state.

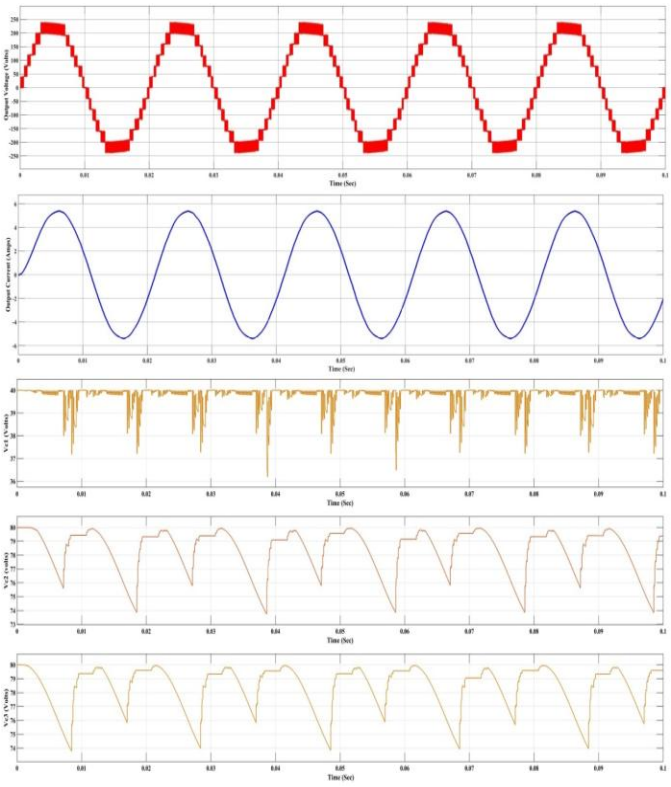

Fig6 Waveform of output voltage and current under steady state condition along with capacitor voltages

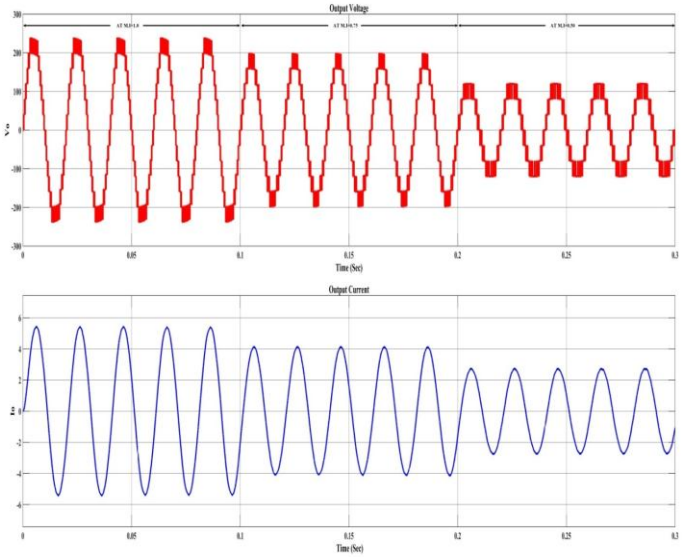

Fig7 waveform of proposed 13SBSCI topology under change in Modulation Index

Fig. 7 illustrates designed topology can function with a range of M.I values (1, 0.75, and 0.50). This enables the planned inverter to have a different number of output levels. Furthermore, in reaction to shifting M.I. values, the output waveform and amplitude change. There are thirteen output levels initially, then eleven, and finally seven. As a result, the proposed SBSCI topology works appreciably for various M.Is. Fig8 depicts the designed topology total harmonic distortion (THD) percentage in current and voltage outputs under various level shift control scheme.

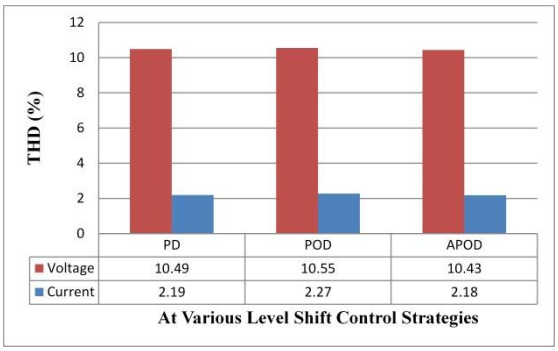

Fig8 Proposed topology THD (%) for various level shift control scheme

Fig. 9 shows how the intended architecture can function with changing in the load. There have been reports that the 13-level is generated by the suggested 13SBSCI architecture with a six-fold increase in step potential from the input voltage. Here system is first operated with 40Ω+50mH, second it is operated at 40Ω, and third it is operated at 40Ω+150mH. As a result, the proposed 13SBSCI works well for step change in load. From Fig10 it illustrates that the designed topology workability under frequency variation of

2500 Hz for 5 cycles and 5000 Hz for next 5 cycles with output voltage, current and trio capacitors output voltage.

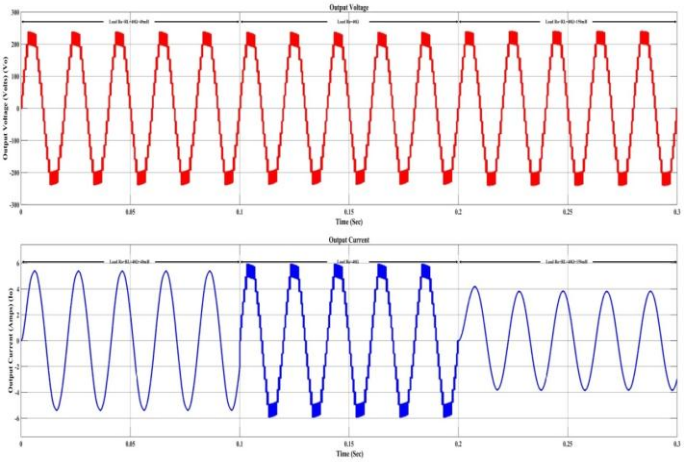

Fig9 Proposed topology workability under step change in load

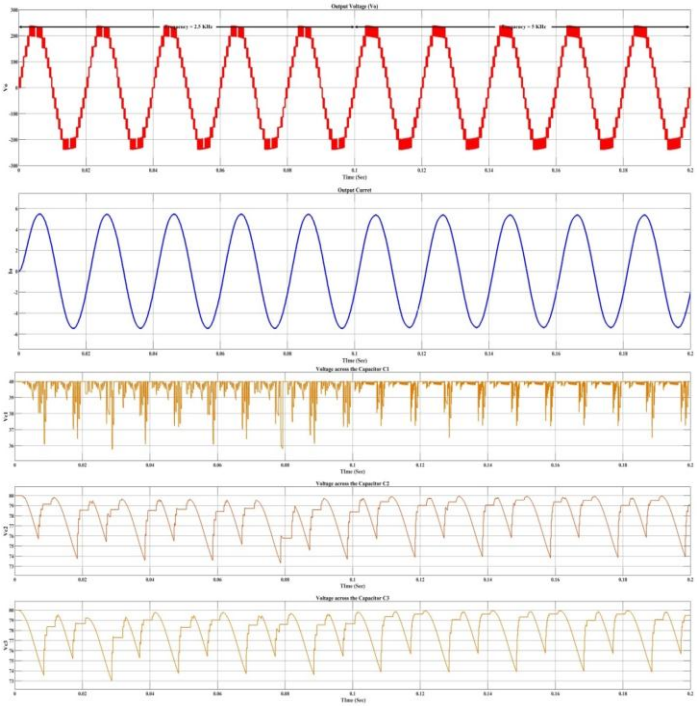

Fig10 Frequency change form 2500 Hz to 5000 Hz of proposed 13SBSCI topology

From Fig11 it depicts that the switching stress voltage across each switched used in designed 13SBSCI topology. The maximum blocking voltage in proposed SBSCI structure is just four times the source voltage. The proposed architecture can therefore be used in high power applications. The aforementioned scenarios demonstrate the suggested switched capacitor topology's superior responsiveness.

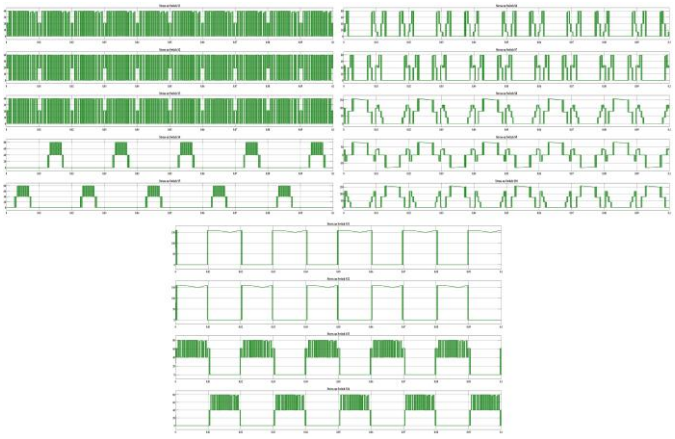

Fig11 Switching stress of proposed 13SBSCI topology

6. CONCLUSION

The topology discussed in this study is a low switch-count, boost-capable, self-voltage-balanced 13-level SBSCI topology. The suggested architecture uses only 14 switches to generate thirteen levels and boosts the output to 6 times from one DC supply. When compared to other switched capacitor topologies that have been previously published, the proposed topology displays a lower TSV and MBV. A detailed investigation of performance comparisons showed that the proposed switched capacitor topology outperforms comparable prior-art. The enhanced voltage boosting capabilities also makes the topology suitable for renewable energy applications. The results of the simulation confirmed the circuit's functionality and showed voltage boosting capability for wide range of M.Is, good voltage and current regulation for load and frequency variation, and reduced switching stress. The proposed switched capacitor topology offers strong structural and functional benefits for high voltage applications.

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