International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 08 Issue: 09 | Sep 2021 www.irjet.net p-ISSN: 2395-0072

Low Power 22nm CMOS Bandgap Voltage Reference Circuit

Deepika B[1], Dr.A.Kiran Gupta[2]

[1]PG Student (M. Tech, VLSI Design and Embedded Systems), Dept. of ECE, DSCE Bangalore, Karnataka
[2]Professor, Dept. of ECE, DSCE, Bangalore, Karnataka

Abstract – *The bandgap circuit is an important component in integrated circuit. The performance of circuits like Digital to Analog(D/A) & Analog to digital(A/D) converters, filters etc. is controlled because of the precision and exactness of circuit's output reference voltage. We need a good bandgap voltage reference(BGVR) circuit with low temperature sensitivity over a large range of temperature. A CMOS BGVR circuit at 22nm is being designed in TANNER EDA tool with input voltage of 0.8V and temperature is varied from -20 °C to 120 °C. Good temperature stability over wide range of temperature variation is obtained.*

Key Words: **CMOS, PTAT, CTAT, Tanner EDA, low power**, **Bandgap Voltage Reference.**

1.INTRODUCTION

Semiconductor technology does not directly offer any electric quantity which is not dependent on ambient temperature. Temperature independency has been envisioned by combining phenomena having opposite temperature coefficients (TCs).

Bandgap Voltage reference circuits are widely used in D/A converters, A/D converters, mixed signal [11] applications, PLL, DRAM. Performance of the circuit is restrained due to accuracy and temperature stability. In traditional BGVR, V_{EB} is subjected to a single first-order compensation. In such case the temperature coefficient appears to be tens ppm/°C. In such cases high-precision ADC, DRAM, etc. are difficult to be satisfied. High-order curvature compensation(CC) techniques [3], [4], [7], [8] have been adopted in recent years but drawback is that for non -linear components of the V_{EB} of high order only single curvature compensation technique is used. This makes difficulty to apply in nanoscale circuits of low voltage due to large TC. Resistors are not driven by op amp and can thus maintain a high loop gain.

Designing a BGVR circuit at 22nm CMOS technology imposes challenges due to second order effects of MOSFETs. In order to obtain better simulated performance, a hybrid adjusted temperature compensation bandgap reference circuit (HTCBR) is proposed [1].

2. DESIGN PRINCIPLE OF BANDGAP

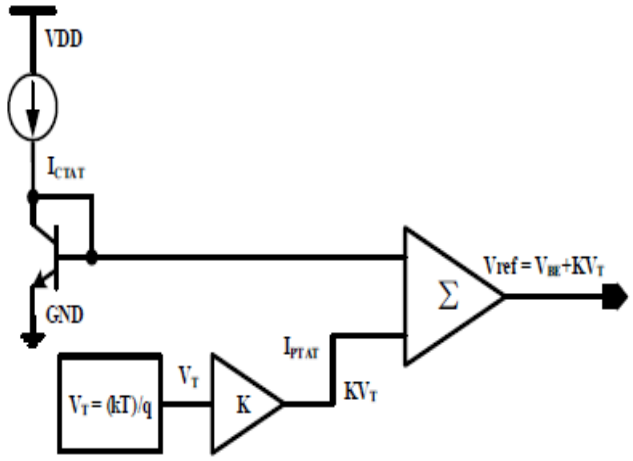

Fig-1: Basic Principle of Bandgap Reference

The operating principle is that two quantities with opposite TC's are added with suitable weightings to obtain zero TC's. Proper identification of positive and negative TC's have to be done. Diode can produce both. CTAT is the voltage complementary to absolute temperature which is the diode voltage. Difference in voltages between diodes which is caused by unequal current densities is PTAT voltage which is *proportional-to- absolute-temperature* voltage. Adding two voltages of opposite TC's with suitable ratio, we obtain a voltage which has zero TC [9], [10]. Fig 1 illustrates the above said principle.

The base-emitter and *pn* junction voltage, V_{BE} exhibit a negative TC. For a constant collector current,

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)\,V_T - E_g/q}{T} \qquad (1)$$

where $V_T = kT/q$, $m = -3/2$, T is the absolute temperature, E_g is the bandgap energy. For current densities, $V_{BE} = V_T \ln(I_C/I_S) = 750$ mV, gives –1.5 mV/K TC at room temperature. To get a such result as shown in Figure 2, we should bias similar two bipolar transistors connected to diodes at different current levels, to obtain current densities of different values.

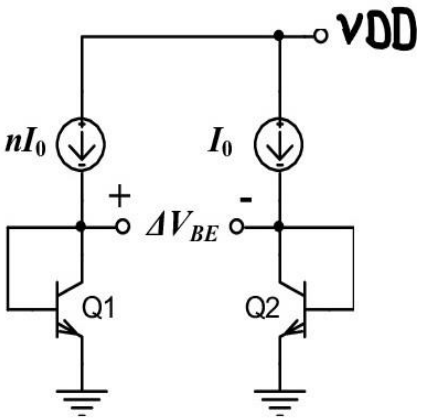

Fig-2: Generation of PTAT voltage.

A zero TC can be obtained if n is choses properly.

$$V_{REF} = V_{BE} + V_T \ln n \qquad (3)$$

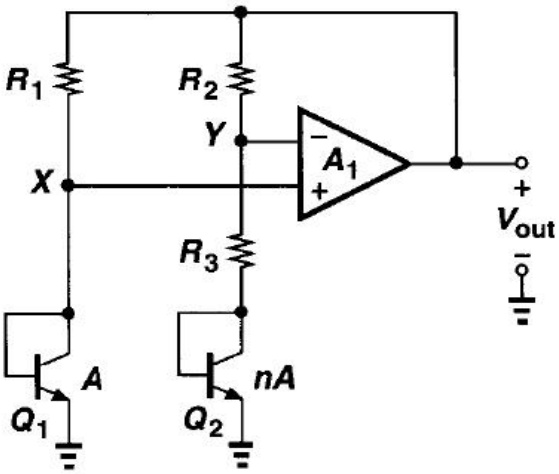

Fig-3: Bipolar Bandgap Reference Circuit

In CMOS technologies, Fig 3 faces three issues. 1. It is tough to realize bipolar transistors with not grounded collector. 2. Op amp driving the feedback resistors should deal with power-gain-stability trade-offs. 3. Amplification of op amp offset by $R2/R3 + 1$ as it appears in Vout, causing temperature drift and error. To solve the issues, we should first look into $R2$ and $R1$ in Fig 3 which provides equal bias currents. In Fig 4, we arrive at the circuit as in Fig 5(a). VBE2 + (1 + $R2/R3$) $V_T \ln n = V$out , $V_T \ln n = V$BE1 – VBE2, for $M2 = M1$.

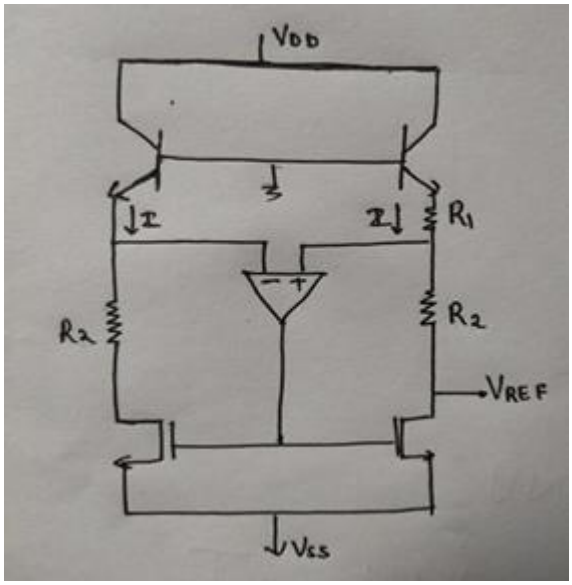

Fig-4: CMOS BGR proposed by Gregorian et alc

Vertical *pnp* structures are constructed from bipolar transistors. With Fig 4, to reduce current mismatch, $R2 = R1$ can be added to make sure VDS2 = VDS1.

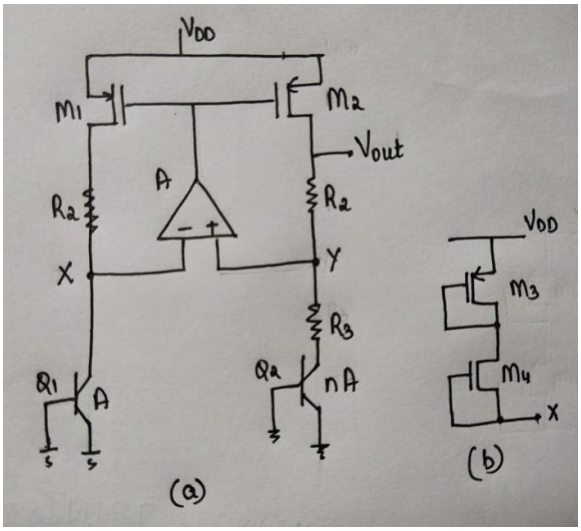

Fig-5: (a) CMOS BGR circuit, (b) Start up circuit

While bandgap reference in Fig 5(a) suffers from several factors: 1. Output may contain thermal (and flicker) noise contribution from the op amp, $M2$ and $M1$, 2. Due to op amp

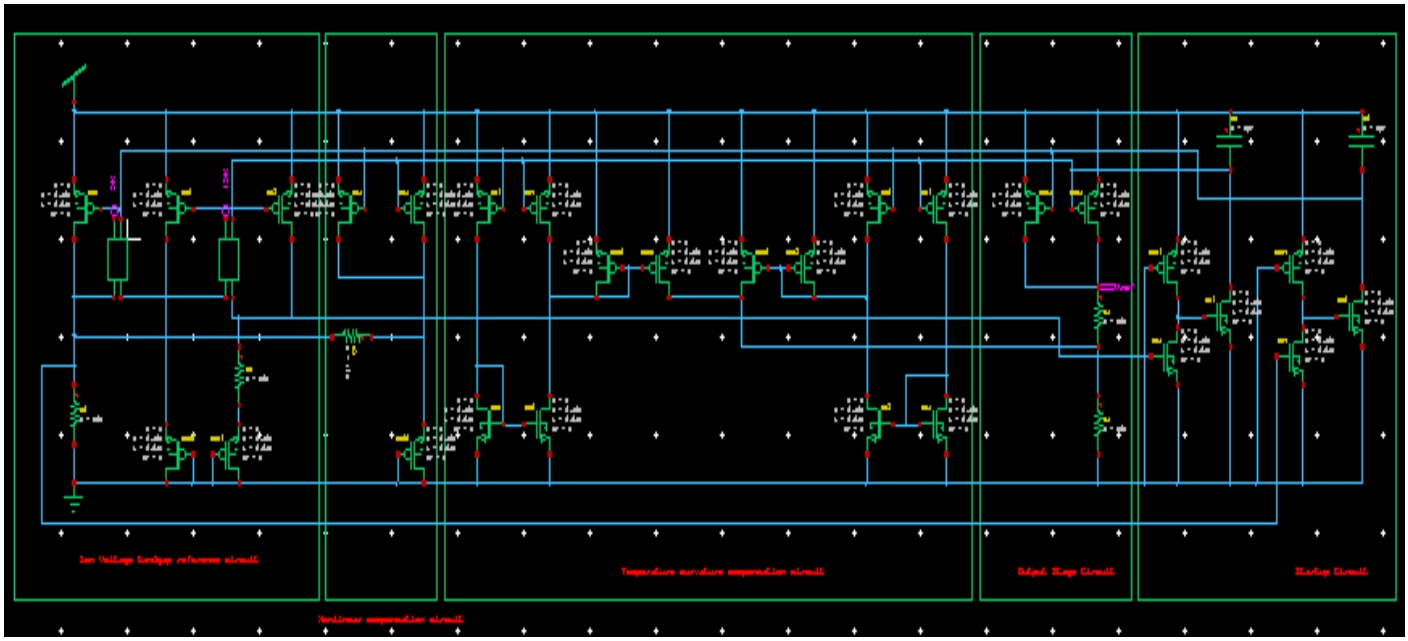

Fig-6: Bandgap Voltage Reference Circuit

the circuit exhibits bad supply rejection, 3. Circuit becomes unstable while driving large load output capacitance. First issue can be solved by using large MOS transistors. Second issue can be solved for high supply rejection by using op amp topology, and start-up circuit is used to solve the third.

3. PROPOSED BANDGAP VOLTAGE REFERENCE CIRCUIT

To get a small TC reference voltage for a wide range of temperature, HTCBR circuit is designed and simulated at 22nm CMOS technology in Tanner EDA tool. Fig 3 shows the proposed topology which consists of a low-voltage bandgap reference circuit, a startup circuit, output stage circuit, a temperature curvature compensation circuit and a nonlinear compensation circuit. Fig 6 shows the proposed circuit.

$$I_{PTAT} = \frac{V_{EB1} - V_{EB2}}{R1} = \frac{V_T \ln(N)}{R1} = \frac{KT \ln(N}{qR1} \qquad (5)$$

$$I_{CTAT} = I_{R2} = \frac{V_{EB1}}{R2}$$

IPTAT and ICTAT [1] are given by the above equations, where the thermal voltage is VT, Boltzmann constant is k, electron charge is q, absolute temperature is T , the emitter-area ratio is N which is the ratio between Q2 and Q1.

V ref is given by,

$$Vref = (R4+R5)\left[\left(\frac{V_{EB1}}{R2} + \frac{V_T \ln(N)}{R1}\right) - \left(\frac{V_{NL}}{R3}\right)\right] \qquad (6)$$

Depending on T temperature compensation is being performed.

$$Vref = \begin{cases} (R4+R5)\left[\left(\frac{V_{EB1}}{R2} + \frac{V_T \ln(N)}{R1}\right) - \left(\frac{V_{NL}}{R3}\right)\right] + A_2(A_1 I_{CTAT} - I_{PTAT})R5 & T < T_1 \quad (7) \\ (R4+R5)\left[\left(\frac{V_{EB1}}{R2} + \frac{V_T \ln(N)}{R1}\right) - \left(\frac{V_{NL}}{R3}\right)\right] & T_1 \le T \le T_2 \quad (8) \\ (R4+R5)\left[\left(\frac{V_{EB1}}{R2} + \frac{V_T \ln(N)}{R1}\right) - \left(\frac{V_{NL}}{R3}\right)\right] + B_2(B_1 I_{PTAT} - I_{CTAT})R5 & T > T_2 \quad (9) \end{cases}$$

3.1. TRANSCONDUCTANCE LNA

The transconductance LNA [2] has two roles: 1. With low noise input voltage should be converted to output current. 2. It should provide a good input matching. Transconductance LNA is designed and simulated at 22nm CMOS technology in Tanner EDA tool. Fig 7 shows the LNA and Fig 8 shows its transient analysis.

4. RESULTS AND DISCUSSION

The HTCBR is designed and simulated in CMOS 22 nm CMOS technology in Tanner EDA tool. Fig. 9 shows variation in output voltage on varying the temperature from -20°C to 120°C for input voltage of 0.8V.

For input voltage of 0.8V, for the temperature variation of -20°C to 120°C, the V ref ranges from 735mv to 741mv. V ref varies closely with the input voltage of 0.8V.

The consumption of power in the proposed topology is shown in table 1 and comparision of the proposed topology against 28nm BGR is shown in table 2.

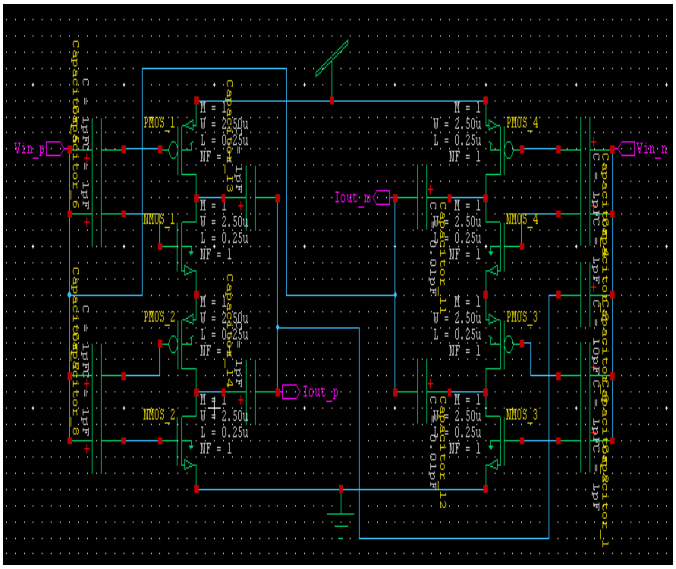

Fig-7: Transconductance LNA

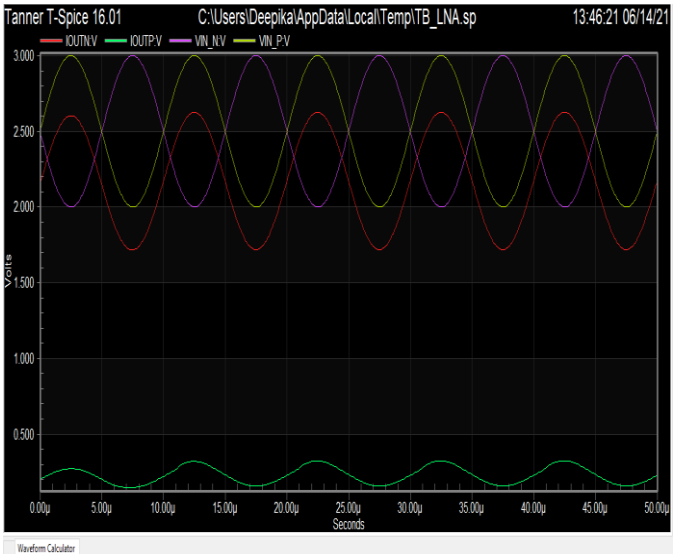

Fig-8: Transient Analysis

Temperature 22nm(°C)	Average Power Consumption(mWatts)
-20	0.4084
-10	0.4111
0	0.1403
10	0.4170
20	0.4200
30	0.4233
40	0.4266
50	0.4301
60	0.4337
70	0.4374
80	0.4412
90	0.4451
100	0.4491
110	0.4532
120	0.4575

Table-1: Power Consumption of BGR

Table-2: Comparision

Low Power BGR		
Technology (nm)	28	22
Supply Voltage (V)	1.05	0.8
Temperature Range	-20°C to 120°C	
Output Voltage(V)	0.987	0.741
MOSFETs	44	44
Area (mm)	1.232	0.968
Power (mW)	0.932	0.457

5. CONCLUSION

This work presents a 22nm BGR simulated in Tanner EDA. For the supply voltage of 0.8V by varying the temperature from -20°C to 120°C, we get an reference output voltage to be 0.741V with power consumption of 0.457m W against 28nm where for the same temperature variation with the supply voltage of 1.05V we get Vref to be 0.987V with power consumption of 0.932m W.

Future work would include working on to lower the power consumption at smaller technology nodes.

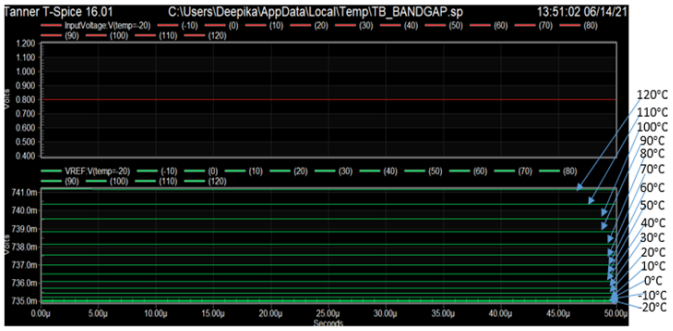

Fig-9: Temperature Sweep Analysis

ACKNOWLEDGEMENT

My sincere thanks to the principal, HOD (Department of ECE) of Dayananda Sagar College of Engineering. I would like to thank Dr. Dinesha P, the Co-Ordinator of VLSI Design and Embedded Systems for the support provided to work on this project. My Sincere gratitude to the guide Dr.A Kiran Gupta for constantly supporting and providing the technical guidance for the project work. I would thank all my friends, who have rendered possible assistance from their end in completion of this work.

6. REFERENCES

[1] Zhanke Yan, Chunming Zhang, Menghai Wang, “Low-Voltage Bandgap Reference Circuit in 28nm CMOS”, IN 2018 IEEE Asia Pacific Conference on Circuits and Systems, pp. 5386-8240.

[2] Omar Elsayed, Amr Abuellil, Ahmed Eladawy, “Highly Linear Low-Power Wireless RF Receiver for WSN” in IEEE transactions on very large scale integration systems(VLSI), pp. 1063-8210. 2019.

[3] C. M. Andreou, S. Koudounas and J. Georgiou, "A Novel Wide- Temperature-Range, 3.9 ppm/°CCMOS Bandgap Reference Circuit," in IEEE Journal of Solid-State Circuits, vol. 47, no. 2, pp. 574-581, Feb. 2012.

[4] Y. Chen, X. Tan, B. Yu, C. Li and Y. Guo, "A new all-in-one bandgap reference and robust zero temperature coefficient (TC) point current reference circuit," 2017 IEEE 12th International Conference on ASIC (ASICON), Guiyang, 2017, pp. 541-544.

[5] A. Samir, L. Girardeau, Y. Bert, E. Kussener, W. Rahajandraibe and H. Barthélemy, "771mV, 173nA, 90nm CMOS resistorless trimmable voltage reference," 2011 IEEE 9th International New Circuits and systems conference, Bordeaux, 2011, pp. 442-445.

[6] Y. Huang, L. Zhu, F. Kong, C. Cheung and L. Najafizadeh, "BiCMOS-Based Compensation: Toward Fully Curvature-Corrected Bandgap Reference Circuits," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 4, pp. 1210-1223, April 2018.

[7] F. Neri, T. Brauner, E. De Mey and C. Schippel, "Low-power, wide supply voltage bandgap reference circuit in 28nm CMOS," 2015 IEEE Jordan Conference on Applied Electrical Engineering and Computing Technologies (AEECT), Amman, 2015, pp. 1-6.

[8] P. Malcovati, F. Maloberti, C. Fiocchi and M. Pruzzi, "Curvature- compensated BiCMOS bandgap with 1-V supply voltage," in IEEE Journal of Solid-State Circuits, vol. 36, no. 7, pp. 1076-1081, Jul 2001.

[9] Y. P. Tsividis, "Accurate analysis of temperature effects in IC-VBE characteristics with application to bandgap reference sources," in IEEE Journal of Solid-State Circuits, vol. 15, no. 6, pp. 1076-1084, Dec. 1980.

[10] R. J. Widlar, "New developments in IC voltage regulators," in IEEE Journal of Solid-State Circuits, vol. 6, no. 1, pp. 2-7, Feb 1971.

[11] J. H. Li, X. b. Zhang and M. y. Yu, "A 1.2-V Piecewise Curvature- Corrected Bandgap Reference in 0.5 um CMOS Process," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 19, no. 6, pp. 1118-1122, June 2011.