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Design and Implementation of Seven Level Inverter with Power Factor Correction

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Abstract: - *The power electronics plays a major role in our day-to-day life. There is not even a device running in our homes without power converter devices encrypted in them. Thus, the use of power converter devices is greatly increased. In this project, a seven-level modified cascaded multilevel inverter is proposed for industrial drive applications. Apart from selecting the conventional level inverters, Multilevel inverters has been chosen for the industrial drive applications as it reduces the total harmonic distortion. The involvement of higher number of switches increases the complexity of the system, which leads to losses in switching, producing huge harmonics and in the end, it entirely reduces the efficiency of the system. The cascaded multilevel inverter involves only fewer switches, where it reduces the complexity of the system which in turn reduces the harmonics and reduces the complexity of the system and in total it reduces the total harmonics distortion. This paper reduces the cost of system and increases the penetration of renewable energy system into distribution system*.

I. Introduction

Inverter is a device which converts DC power into AC. The power in the battery is in DC mode and the motor that drives the wheels usually uses AC power, therefore there should be a conversion from DC to AC by a power converter, inverter is used for this conversion [1]. The two-level is the simplest topology used for this conversion that consists of four switches. Each switch needs an anti-parallel diode, so there should be also four anti-parallel diodes. There are many other topologies for inverters. A multilevel inverter (MLI) is a power electronic system that produces a sinusoidal voltage output from several DC sources. These DC sources can be fuel cells, solar cells, ultra-capacitors, etc. The major function of multilevel inverters is to generate a better sinusoidal voltage and current in the output by using switches in series. Since many switches are put in series the switching angles are important in the multilevel inverters because all of the switches should be switched in such a way that the output voltage and current have low harmonic distortion (THD). Comparing two-level inverter topologies of the same power ratings, MLIs also have the advantage that the harmonic components of line-to-line voltages fed to the load are reduced owing to its switching frequencies. The multilevel inverters have become increasingly attractive for researchers and manufacturers due to their advantages over conventional three-level pulse width modulated (PWM) inverters. The MLI produces improved output waveforms, low EMI, lower total harmonic distortion (THD) and reduced filter size. Multilevel inverter topology requires the least components for a given number of levels. Multilevel inverters can be classified into three types [2]. Diode clamped multilevel inverters [3]-[4], flying capacitor multilevel inverters [5] and cascaded H-bridge multilevel inverter [6]. The THD is decreased by increasing the number of levels. Though, an output voltage with low THD is desirable, increasing the number of levels leads to more hardware, also the control will be more complicated. It is a tradeoff between price, weight, complexity and a very good output voltage with lower THD. Among these multilevel topologies the diode clamped inverters (DCMLI), particularly, the three-level structure has a wide popularity in motor drive applications besides other multi-level inverter topologies. But it has got limitations such as complexity and number of clamping diodes for the DCMLIs, as the level exceeds. The Flying Capacitor Inverters (FCMLI) are based on balancing capacitors on phase buses and generate multilevel output voltage waveform clamped by capacitors instead of diodes. Cascaded H-Bridge MLI topology is based on the series connection of H-bridges with separate DC sources. Since the output terminals of the H bridges are connected in series, the DC sources must be isolated from each other. The need of several sources on the DC side of the inverter makes multilevel technology attractive for photo voltaic applications [6].

The only drawback of the multilevel converter is that it requires a large amount of semiconductor switches. Lower voltage rated switches can also be used in the multilevel converter and as a result the active semiconductor cost is not considerably increased when compared with the two-level cases. On the other hand, each active semiconductor added requires associated gate drive circuitry and adds further complication to the converter mechanical layout. Another disadvantage is that small voltage steps are typically formed by isolated voltage sources or a bank of series capacitors. Isolated voltage sources may not always be readily available and series capacitors require voltage balance. A multilevel converter can be implemented in

different ways, each with advantages and disadvantages. The simplest techniques which involve the parallel or series connection of conventional converters is to form the multilevel waveforms. Complicated structures actually insert converters within converters. Whatever approach is being chosen, the subsequent voltage or current rating of the multilevel converter will become a multiple of the individual switches, and therefore the power rating of the converter can exceed the limit imposed by the individual switching devices. The paper is organized as follows: Different multi-level inverter topologies such as Diode-Clamped inverter, Capacitor Clamped inverter, and Cascaded Multi cell inverter are discussed, initially for understanding the features of the multilevel inverters and the seven-level inverter topology for each configuration is discussed. The comparative study of the seven-level inverter of different topologies are studied.

II. INVERTER TOPOLOGIES

Many topologies, or circuit designs have evolved for creating high power AC from low voltage DC source. This section gives an introduction to the evaluation of different converter topologies which includes: Diode-Clamped Inverter (DCI), Capacitor-Clamped Inverter (CCI), Cascaded Multi-cell Inverters (CMI), Generalized Multilevel Cells (GMI) and Some Emerging Multilevel Inverter Topologies. These are briefly described below. A. Diode-Clamped Inverter This inverter is also called as Neutral-Point Clamped Inverter (NPC). In the NPCMLI topology the use of voltage clamping diodes is essential. A common DC-bus is divided by an even number of bulk capacitors in series with a neutral point in the middle of the line. The number of capacitors depends on the number of voltage levels in the inverter. From this DC-bus, with neutral point and capacitors, there are clamping diodes connected to an (m-1) number of valve pairs, where m is the number of voltage levels in the inverter (voltage levels it can generate) [7]. A simple three-level diode-clamped inverter is shown in Fig. 1(a). In this circuit, the DC-bus voltage is split into three levels by two series-connected bulk capacitors, C1 and C2. The middle point of the two capacitors „n" can be defined as the neutral point. The output voltage van has three states: Vdc/2, 0, and -Vdc/2. For voltage level Vdc/2, switches S1 and S2 need to be turned on; for -Vdc/2, switches S1" and S2" need to be turned on; and for the 0 level, S2 and S1" need to be turned on. The key components that distinguish this circuit from a conventional two-level inverter are D1 and D1". These two diodes clamp the switch voltage to half the level of the DC-bus voltage. When both S1 and S2 turn on, the voltage across a and o is Vdc, i.e., va0 = Vdc. In this case, D1 balances out the voltage sharing between S1"and S2" with S1" blocking the voltage across C1 and S2" blocking the voltage across C2. Therefore, the output voltage van is AC, and va0 is DC. The difference between van and va0 is the voltage across C2, which is Vdc/2. If the output is taken out between a and o, then the circuit becomes a dc/dc converter, which has three output voltage levels: Vdc, Vdc/2 and 0. Fig. 1(b) shows a seven-level diode-clamped converter in which the DC bus consists of six capacitors, C1, C2, C3, C4, C5 and C6. For DC-bus voltage Vdc, the voltage across each capacitor is Vdc/6, and each device voltage stress will be limited to one capacitor voltage level Vdc/6 through clamping diodes. To explain how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point. There are seven switch combinations to synthesize seven level voltages across a and n is given in Table I

TABLE I: SWITCHING STATES FOR A SEVEN LEVEL DIODE CLAMPED INVERTER

V_0	$V_{dc}/2$	$V_{dc}/3$	$V_{dc}/6$	0	$V_{dc}/6$	$V_{dc}/3$	$V_{dc}/2$
S_1	1	0	0	0	0	0	0
S_2	1	1	0	0	0	0	0
S_3	1	1	1	0	0	0	0
S_4	1	1	1	1	0	0	0
S_5	1	1	1	1	1	0	0
S_6	1	1	1	1	1	1	0
S_1"	0	1	1	1	1	1	1
S_2"	0	0	1	1	1	1	1
S_3"	0	0	0	1	1	1	1
S_4"	0	0	0	0	1	1	1
S_5"	0	0	0	0	0	1	1
S_6"	0	0	0	0	0	0	1

Six complementary switch pairs exist in each phase. The complementary switch pair is defined such that turning on one of the switches will exclude the other from being turned on. In this example, the six complementary pairs are (S1; S1‟), (S2; S2‟), (S3; S3‟), (S4 ; S4‟), (S5 ; S5‟) and (S6; S6‟).

Although each active switching device is only required to block a voltage level of Vdc /(m-1), the clamping diodes have different voltage ratings for reverse voltage blocking. Using D1‟ of Fig. 1(b) as an example, when lower devices S2‟- S6‟ are turned on, D1‟ needs to block three capacitor voltages, or 3Vdc/4. Similarly, D3 and D3‟ need to block Vdc/2, and D4 needs to block 3Vdc/4. Assuming that each blocking diode voltage rating is the same as the active device voltage rating, the number of diodes required for each phase will be (m-1) (m-2). This number represents a quadratic increase in m. When m is sufficiently high, the number of diodes required will make the system impractical to implement. If the inverter runs under PWM, the diode reverse recovery of these clamping diodes becomes the major design challenge in high-voltage high-power applications.

III. Work done:

The proposed paperwork consists of following activities: -

1. To understand the working of inverter.
2. To study the power factor correction methods for an inverter.
3. To understand the problems faced by distribution system.
4. To study working and design of inverter.
5. To verify the circuit we used the MATLAB for simulation and correct the circuit.
6. To design 7-level inverter as per desired specifications.
7. To design the power factor correction circuit.
8. To test the output of the model.

1. To understand the working of inverter:

We have studied the working principle of inverter. After this we studied multilevel inverters and their construction. As we choose the 7-level inverter for design hence we studied construction and working of 7 level inverters in detail. Also studied the advantages of 7 level inverter over 2/3 level inverter.

2. To understand the problems faced by distribution system:

As we all know that there are many problems in distribution system. One which is due to low power factor. Hence, we studied the disadvantages of low power factor over high-power factor and harmonic distortion created in the system. Improvement in power system due to 7 level inverters.

3. To study the power factor correction methods for an inverter:

We have studied the disadvantages of low power factor and need to improve it. Studied the various methods of power factor correction.

4. To study working and design of inverter:

Hence, we have designed the whole circuit of 7 level inverter with power factor correction circuit and all the other equipment necessary for design.

5. Used MATLAB simulation to verify the circuit:

We have simulated the circuit diagram using MATLAB and verify the output waveforms as per the requirement.

Comparison between conventional and multilevel inverter:

Table 2 components

Sr. no.	Conventional inverter	Multilevel inverter
1.	Higher THD in output voltage	Low THD in the output voltage
2.	More switching stresses on devices	Reduced switching stresses on devices
3.	No applicable for high voltage application.	Applicable for high voltage application.
4.	Higher voltage level are not produced	Higher voltage level are produced
5.	Since dv/dt is high, the EMI from the system is high	Since dv/dt is low, the EMI from the system is low.
6.	Higher switching frequency is used hence switching losses are high.	Lower switching frequency is used hence switching losses are low.
7.	Power bus structure, control schemes are simple	Control scheme is complex as the no. of levels increases.

Circuit Diagram:

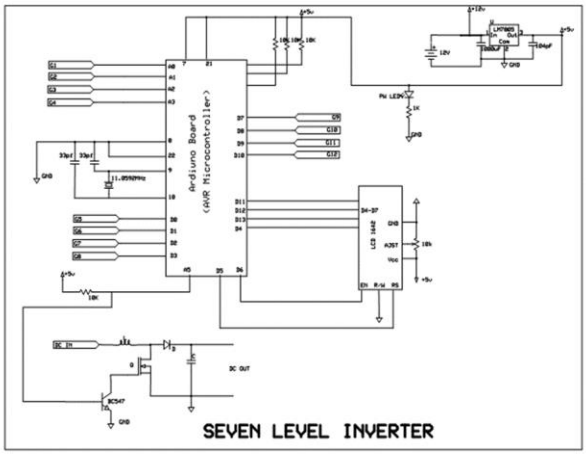

Fig.1 circuit diagram of seven level inverter

Components Required:

Table 3 components

Sr No	Components	Quantity	Specifications
1	MOSFET	12	IRFZ44N
2	IR2110 Driver	6	IR2110
3	Arduino UNO (AVR Microcontroller)	1	-
4	MOSFET	3	IRF450
5	Capacitor	5	470 µf
6	Battery	3	4 V
7	Inductor	2	17mH
8	Regulator	1	7805
9	Resistors	7	10k
10	Capacitor	2	10µf
11	Crystal	2	11.0592MHz
12	Capacitor	4	22pf
13	Diodes	7	IN4007
14	LCD 16×2 display	1	16×2

IV. Future Scopes:

The cascaded 7 level inverter configuration can be installed for other application like SVC system and performance can be studied for large AC system. It is used as a drive for induction motor, shunt active power filter, aerospace and solar powered application, incorporating neuro –fuzzy controller.

The level of inverter configuration can be increased and further improvement of terms of performance and power quality issues can be broadly studied.

V. Conclusion:

In this paper improved power factor seven level inverter is proposed that can meet the requirement of desired power factor. The structure of proposed system consists of H bridge cascaded form, power factor correction circuit. The simulation of seven level inverter with power factor correction is carried out in MATLAB/Simulink to identify level which has comparatively less total harmonic distortion and improved power factor in its output. The feasibility and effectiveness of the proposed system has been successfully evaluated with various simulation studies and practical implementation.

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