International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395-0056
Volume: 08 Issue: 09 | Sep 2021 www.irjet.net p-ISSN: 2395-0072

Low Power SR-Latch Based Flip-Flop Design Using 21 Transistors

Kinga Lhaden Dakpa[1], Thubten Jamtsho[2], Kamal Kumar Chapagai[3]

[1,2,3]*Dept. of Electronics and Communication Engineering, College of Science and Technology, Bhutan*

Abstract - *This paper proposes a design for an edge triggered flip-flop. The design is based on an SR latch and can be used in low voltage and low power applications. It uses a conventional NAND gate flip-flop design whose design flaw is eliminated by removing the redundant logic present in the design. The proposed circuit is designed and simulated using OrCAD PSPICE. The redundant logic was successfully removed with the circuit functioning as per its truth table. The newly designed flip-flop consumes a power of 83.47μW which implies a low power consumption. The proposed circuit can be expected to have a higher speed compared to the conventional design due to the reduction in the number of transistors.*

Key Words: NAND gate, flip-flop, ORCAD, PSPICE, SR latch, edge triggered device

1. INTRODUCTION

Electronics use flip-flops (FF) to store data. Flip-flops or latches are circuits that can remember the information of a state, which allows it to be used as memory. Their efficiency depends on the power consumption and the overall chip area.

Therefore several methods has been implemented to achieve low power consumption such as reducing the supply voltage. For flip-flops, at low supply voltages their performance degrades, therefore supplying a low voltage is not viable for flip-flops design [1].

The design of flip-flops has constantly evolved over the years, based on their target applications. In this paper, the flaws of some classic flip-flop design are studied and a newly proposed efficient design that can be applied in low power applications has been verified.

One of the leading flip-flop designs in the industry is the Transmission gate-based Master Slave flip-flop [2]. This design relies heavily on the clock which increases its workload along with the requirement of inverters to invert clock signals, which leads to more power consumption [3].

A NOR type SR latch-based flip-flop has been proposed recently [1]. However, the requirement of inverted clock signals and the stacked PMOS structure increased its power consumption [4].

The traditional design uses three-input NAND gates which increase the number of transistors and has a redundant logic in the circuit [5]. The redundant logic in the circuit could be simplified by using a newer logic which is described in this paper.

In this paper, a newly presented design of an edge triggered flip-flop which is designed based on a SR Latch is verified. The design consists of six two-input NAND gates and a single-phase clock loading which generally starts increasing the clock signal loading. Due to the lower transistor count and a short circuital path in this design, a smaller layout area is obtained.

2. CONVENTIONAL DESIGN

The conventional flip-flop consists of NAND gate-based SR latch flip-flop consisting of 5 two-input NAND gates and a three-input NAND gate as shown in the Fig. 1.

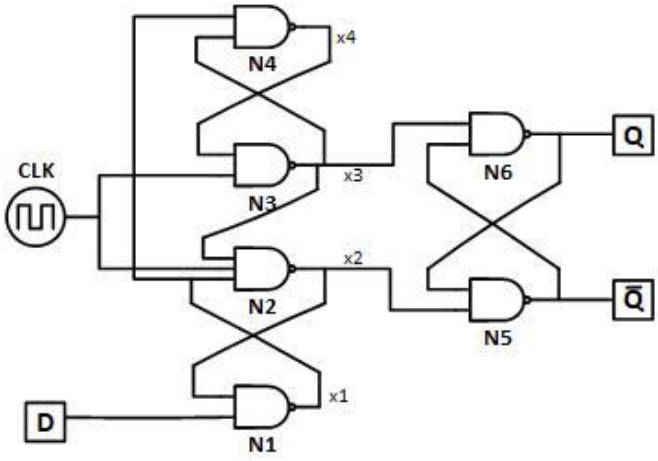

Fig -1: Conventional edge triggered flip-flop [5]

Table -1: Truth table of Conventional Edge Triggered Flip-Flop

D	CLK	X2	X3	Q	$\bar{Q}$
0	0	1	1	P	P’
1	0	1	1	P	P’
0	1	0	1	0	1
1	1	1	0	1	0

In Table 1, P refers to Previous State and P’ refers to the Opposite of Previous State.

2.1. Operation of Conventional Design

Here the gate N4 (uppermost NAND gate) and N3 forms the S Latch and the gates N1 (Lowermost NAND gate) and N2 forms the R Latch. N5 and N6 is the main latch of the flip flop. The input S and R Latch is cross-coupled which means the inputs to the S and R latch is latched by the main SR latch.

When clock is LOW, it causes X2 and X3 to be high, since giving a LOW input to a NAND gate results in a High regardless of the other inputs. Since x2 and x3 are given as inputs to the main latch, it allows the main latch to latch the data (input of S=1 and R=1 to a SR latch results in the same result as previous state).

When Clock is going HIGH, the state of data begins to affect the circuit which means that change in data signal will pass through x2 and x3. The change in x2 and x3 affects the Q at the end of main latch and it usually is equal to Data input given. After the clock becomes HIGH the input Data can no longer affect the results of the main latch. So, we can conclude that the FF is a positive edge triggered D flip-flop.

2.2. Drawback of using Conventional Design

In this Conventional design of a NAND SR latch-based flip-flop, there is a redundant logic and a three input NAND gate which can be eliminated. The redundant logic comes from the fact that two of the inputs for the three input NAND gate (N2) is same, which is x1 or same as value given to D. Therefore, x1 as an input to N2 can be eliminated thereby eliminating the need for the three input NAND gate.

3. PROPOSED DESIGN

The conventional design of an edge triggered flip-flop contains a redundant which can be eliminated by replacing the three-input NAND gate with a two-input NAND gate. The design then consists of 6 two input NAND gates, arranged in a similar way to the conventional design as shown in Fig - 2. N1 and N2 forms the R latch, N3 and N4 forms the S latch and N5 and N6 forms the main latch.

The operation of the proposed flip-flop design is similar in to the conventional flip-flop but with the direct input 'D' to N2 removed. It now has to wait for the 'D' input from x3, which leads to glitches at the node x2. These glitches will increase the power consumption. This problem can be removed by using a method known as Pass Transistor Logic, which is implemented at the transistor level of the design. This design also uses a method known as transistor-sharing, which decreases the number of transistors required by sharing a NMOS transistor requiring the same input.

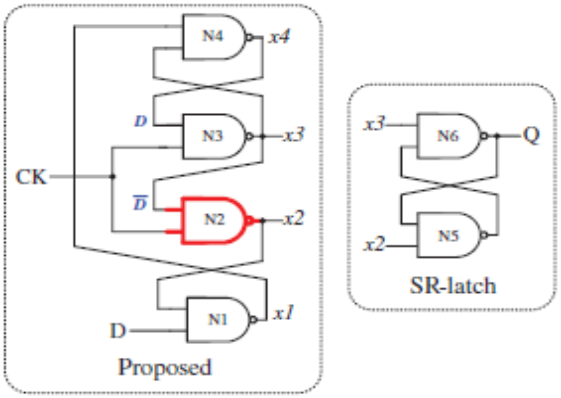

Fig -2: Proposed Design [5]

4. SIMULATION

The transistor level circuit consists of 21 transistors, which forms the 6 NAND gates required for the flip-flop shown in Fig -2. N1, N2, N3 and N4 which forms the S and R latch is simulated in one separate simulation (circuit shown in Fig - 3). N5 and N6 which forms the main SR latch are simulated in another simulation file (circuit shown in Fig - 4). MOSFETs were used as the transistors in the design of the circuits.

5. SIMULATION RESULT

The simulation results show the verification result of the proposed design of an edge triggered flip-flop. The purpose of the circuit in Fig -3 is to not let x2 and x3 go low at the same time. As shown in Fig -5, x2 and x3 alternates between being high and low and being high together but never goes low in the same clock cycle. The second circuit is a simple NAND gate-based SR Latch. This proves that the input latches design works perfectly. As evident in the truth table above, giving input low to S and R is forbidden. Therefore, when x2 and x3 are fed as input to the main SR latch, the data gets latched with changes in clock.

For the Second part of the simulation, the circuit is a SR latch, whose working is confirmed by cross checking the simulation result with a Truth table of SR latch. From the first simulation result (Fig -5), it is found that the results obtained had no clock cycle where x2 and x3 were both low which means that the main latch will only remain in either set or reset or hold state and avoid going into the forbidden state. OrCAD PSCPICE does not allow 21 transistors to be used in a single simulation. Therefore, the conclusion were drawn from the result obtained from the circuits simulated separately. As evident in Fig -5 and Fig - 6, it can be concluded that the newly proposed design is operating successfully.

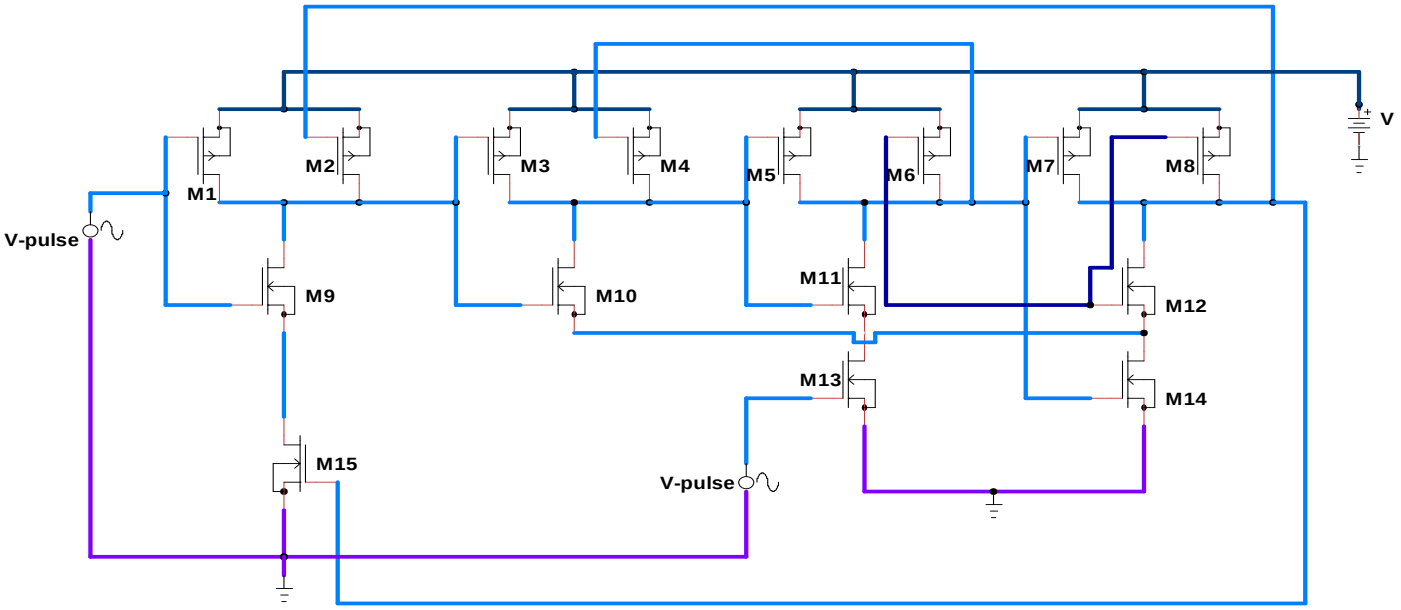

Fig -3: PSPICE circuit of the S and R latch

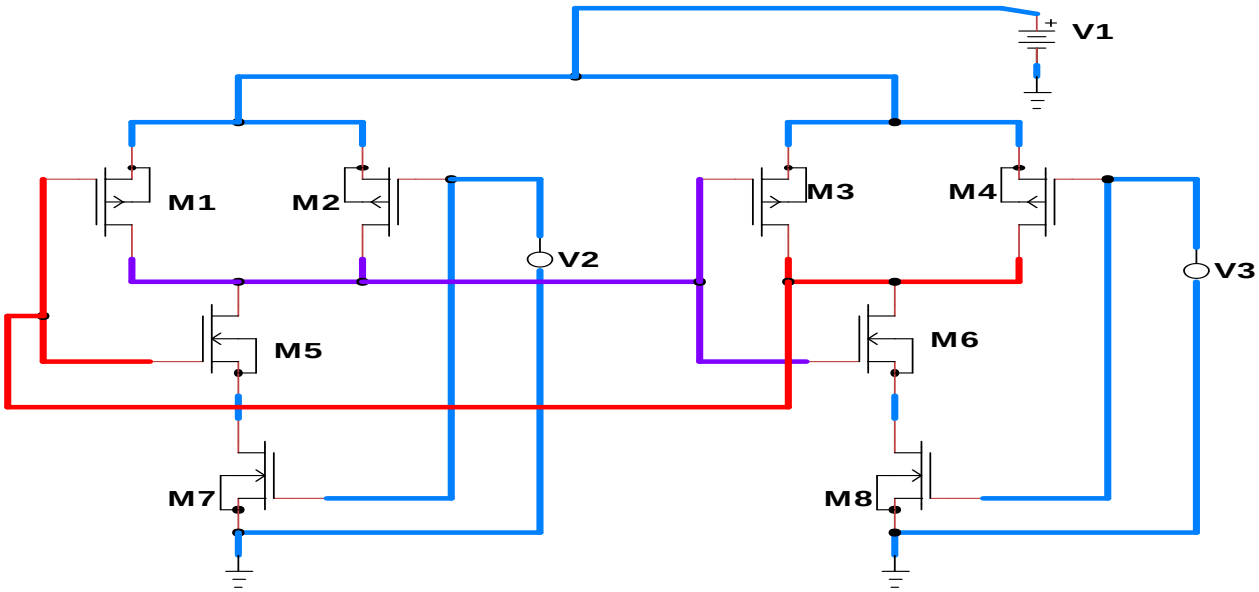

Fig -4: PSPICE circuit of the main SR latch

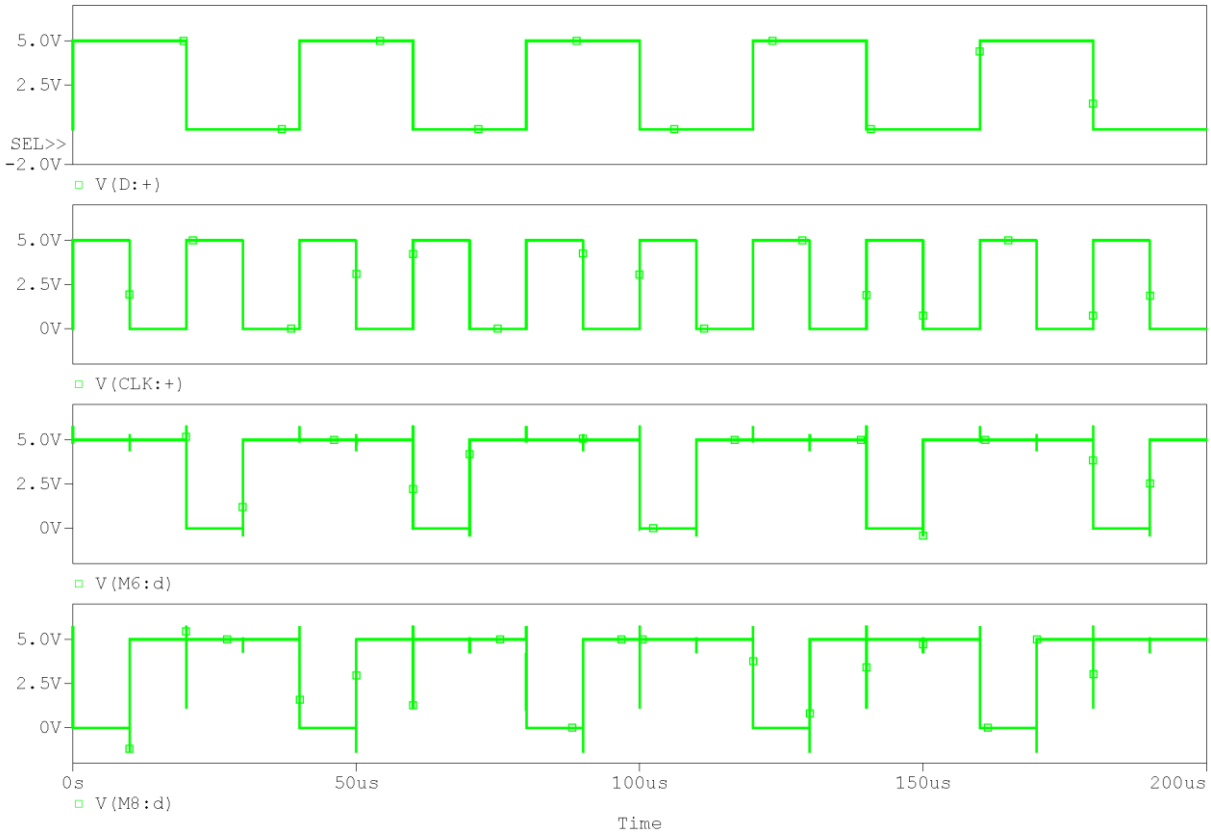

Fig -5: Simulation result of the S and R latch circuit

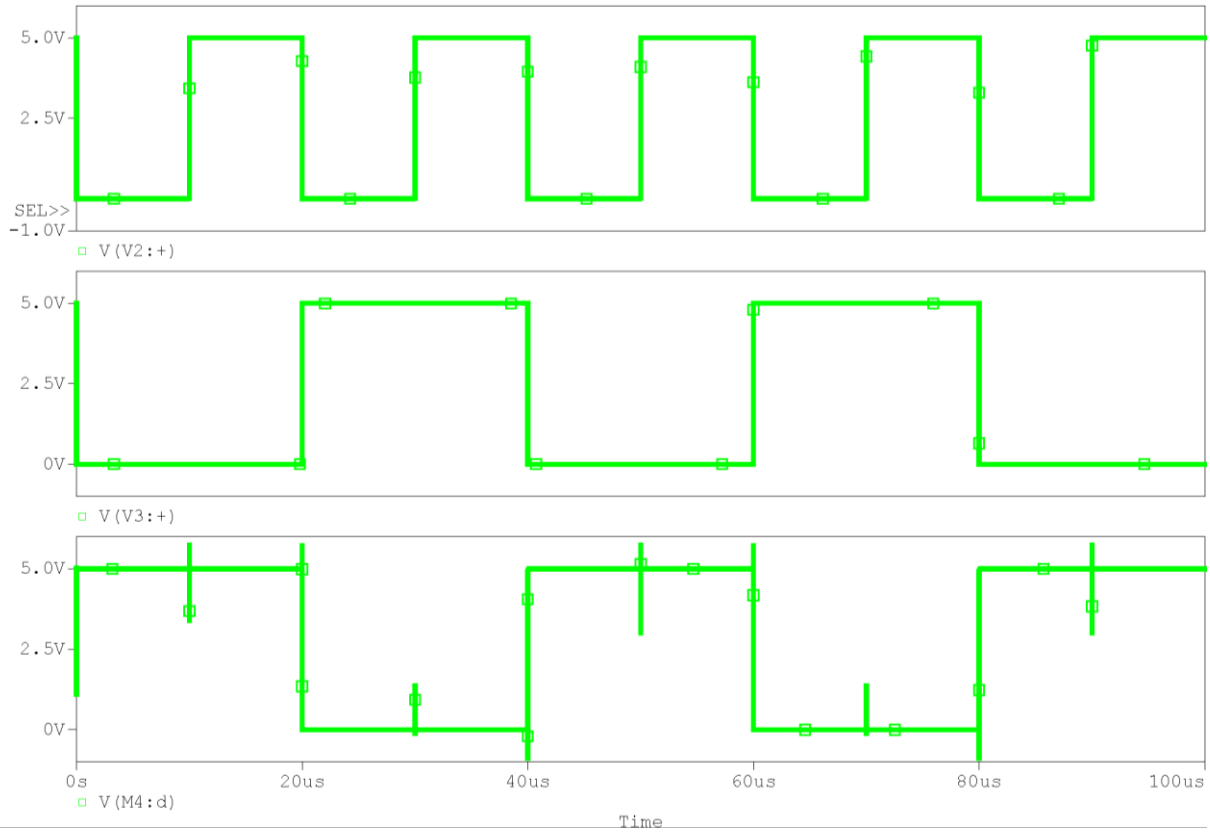

Fig -6: Simulation result of the main SR latch circuit

6. POWER CONSUMPTION

The power consumed by the proposed design is 83.47 µW, which is suitable for low power application.
The power consumed by each component is shown in Table-2 and Table -3.

Table -2: Power consumed by each component in circuit of the S and R latch

Components	Power Consumed
M1	401.6 x 10^{-27} W
M2	8.911 x 10^{-27} W
M3	25.05pW
M4	25.05pW
M5	25.20 x 10^{-21} W
M6	25.20 x 10^{-21} W
M7	8.911 x 10^{-27} W
M8	401.6 x 10^{-27} W
M9	25.05pW
M10	395.5 x 10^{-21} W
M11	6.275pW
M12	25.05pW
M13	6.275pW
M14	890 x 10^{-21} W
M15	98.89 x 10^{-21} W
D	0W
CLK	0W
V3	-112.7pW

Table -3: Power consumed by each component in circuit of the main SR latch

Components	Power Consumed
M1	23.61µW
M2	8.02pW
M3	23.61µW
M4	8.02pW
M5	17.85 µW
M6	17.85 µW
M7	277.3nW
M8	277.3nW
V1	-83.47 µW
V2	0W
V3	0W

7. CONCLUSION

A new design for an edge triggered flip-flop is proposed in this paper which eliminates the redundant logic prominent in the conventional design. Eliminating the redundant logic decreases the number of transistors required and makes circuit simpler. The power consumed would also decrease by the reduction of the number of transistors. The proposed design for an edge triggered flip-flop is based on an SR latch. It consists of a six two-input NAND gates and a single phase clock. The circuit of the proposed design was simulated using OrCAD PSPICE. The simulation of the proposed design was successful with the new design operating without the redundant logic of a conventional design. The power consumed by the proposed design was found to be 83.47 µW. The new design is also expected to operate with a higher speed than that of the conventional design since there is a reduction in the number of transistors which would reduce the delay time.

REFERENCES

[1] Y. Shizuku, T. Hirose, N. Kuroki, M. Numa and M. Okada, "A 24-Transistor Static Flip-Flop Consisting of NORs and Inverters for Low-Power Digital VLSIs," IEEE, Vols. -, no. -, pp. 137-140, 2014.

[2] N. Kawai, S. Takayama, J. Masumi, N. Kikuchi, Y. Itoh, K. Ogawa, A. Ugawa, H. Suzuki and Y. Tanaka, "A Fully Static Topologically-Compressed 21-Transistor Flip-Flop With 75% Power Saving," IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 49, no. 11, pp. 1-8, 2014.

[3] P. Zhao, T. K. Darwish and M. A. Bayoumi, "High-Performance and Low-Power Conditional Discharge Flip-Flop," IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, vol. 12, no. 5, pp. 477-484, 2004.

[4] S. N. Z. C. S. B. M. S. James Tschanz, "Comparative Delay and Energy of Single Edge-Triggered & Dual Edge-Triggered Pulsed Flip-Flops," in Low Power Electronics and Design, International Symposium, Huntington Beach, California, USA, 2001.

[5] J.-F. Lin, M.-Y. Tsai, K.-S. Li, Y.-R. Jiang and a. Y.-S. Cheng, "Low Power SR-Latch Based Flip-Flop Design Using 21 Transistors" in Journal of Low Power Electronics, pp. 1-5,2016