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A Review on Successive Approximation ADC

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Abstract - *This review paper is a study to summarize developments in Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC). The main aim is to provide necessary information on all key factors, options and problems that have to be taken into consideration while designing. The review focuses on detailed explanation on the main components involved that are Sample-and-Hold circuit (S/H), Digital-to-Analog converter (DAC), SAR control logic, asynchronous clock and comparator. The algorithm explored here is a binary search. Various performance parameters like gain error, offset error, Differential (DNL) and Integral (INL) nonlinearities summed up along with the causes and techniques. Numerous architectures like Capacitive (C-2C) or Resistive (R-2R) ladder, Two-stage weighted (TWC) and Binary-weighted capacitance (BWC) briefed with their effects. Parasitic effects, Floating voltage shield (FVS), bootstrapped switching, metastability, delay line, inherent S/H, charge redistribution, antialias and reconstruction filters also reviewed. There have been a lot of designs of various SAR ADC in numerous journals, and hence this review paper would be focusing on some major components, parameters, techniques and errors while designing a SAR ADC.*

Key Words: SAR, ADC, DAC, Comparator, Control Logic, Capacitive arrays, Performance parameters, Clock, Binary search, BWC, C-2C, TWC.

1. INTRODUCTION

Successive approximation register (SAR) Analog-to-Digital converter (ADC) is used to approximate the given analog input with high accuracy, low power and in less time [1][14]. ADC plays a vital role where there is an increase in the demand for digital components. The demand for these circuits is increasing day by day with increasing Internet of Things' (IoT) products, Nuclear Reactors and Medical devices which demand low power consumption for better battery life and high-speed operations [4][5][6][7][8][10][12][13]. Nowadays, technology is transforming the system in becoming compact throughout, this is possible due to the use of Complementary Metal Oxide Semiconductor (CMOS) Field-Effect Transistor (MOSFET) [1][2][3][6]. ADCs result in effective communication where the accuracy of the device is needed. This depends on the resolution of the components in ADC. While the error of the system varies on its linearity. This is achieved by quantizing the input forming a sequential code rather than directly comparing [15].

ADC also plays a vital role in devices where high-speed operations are required. The most generic option for choosing an ADC could be Flash type ADC. But this ADC is too power-hungry. That is due to the high comparator number even at low resolutions [14]. Whereas nowadays the demand is more for low power and high resolution. This demand is due to scaling in the field of CMOS technology and fast lifestyles of people.

2. LITERATURE REVIEW

ADC are important and are used in a signal processing system. Among ADCs, SAR ADC is used in low power, high resolution, area-efficient, simple to implement circuits [7], [12]. The recent development in CMOS SAR ADC made to reduce the power consumption and increase efficiency [4], [7][8][9]. These ADC have high accuracy at a low-to-medium resolution [5]. Due to advancements in technology and manufacturing, various people have designed multi-level structures of SAR ADC. These structures consume low power and components without affecting the resolution [7]. There are designs available based on tunable delays which reduce the errors and factors of mismatching the clock [8]. In some papers, even the time complexity observed to be decreased based on the design by 50% [1]. Capacitance plays a crucial role in deciding the resolution, time and power consumption of a SAR ADC circuit. Majorly papers focus on reducing the number of capacitors involved to reduce the switching and few designs even try to combine two components by using hybrid nature or pipelined designs. There are also other types of ADCs available like flash/half-flash, single/dual-slope, delta-sigma and pipelined ADCs but SAR ADC is the most efficient.

All the reviewed papers propose different architecture, solutions and methods of their own for minimizing power, reducing complexity or increasing efficiency. So, we aim to summarize all the information to enable beginners and designers to choose specific method, architecture or technique according to their own need. This reduces their efforts and saves time greatly rather than going through numerous papers. Because no paper consists of a complete solution to all the needs, every respective author only talks about their own need or problem and how they solved them.

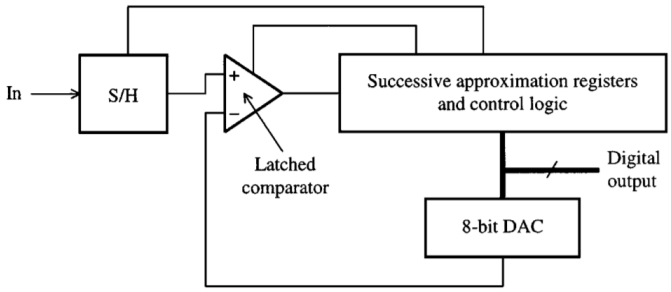


Fig -1: Block Diagram of SAR ADC

3. ARCHITECTURE

The most critical components, as shown in Fig. 1 from [3], while designing a SAR ADC are S/H circuit, DAC, SAR Control Logic and a Comparator. Therefore, anyone targeting to design a SAR ADC circuit for low power, high resolution, more accuracy, compact design, etc., needs to embed these basic building blocks into their schematic. The working of the SAR ADC is in such a way that, first an analog input is received at the S/H circuit. This is then sampled and held for a definite amount of time/cycles. After this process, the Most Significant Bit (MSB) of N bit SAR ADC is forwarded to the comparator where this input is compared with the feedback received from the DAC and the reference voltage (Vref). And according to the comparison, the SAR control logic gives the output which is feedback to the DAC. And this feedback is fed to the comparator until all bits are exhausted or Least Significant Bit (LSB) is reached [1][3][4][5][12][13][14][15]. If the new sample from the DAC is in the vicinity of the previous sample then only LSB can be extracted. This not only saves power but also fewer cycles are required [4]. Fig. 2 from [1] depicts the placement of the main components of SAR ADC. The zoomed picture of the etched printed circuit board is taken from a microscope. The S/H, Comparator, DAC and switches blocks are highlighted accordingly.

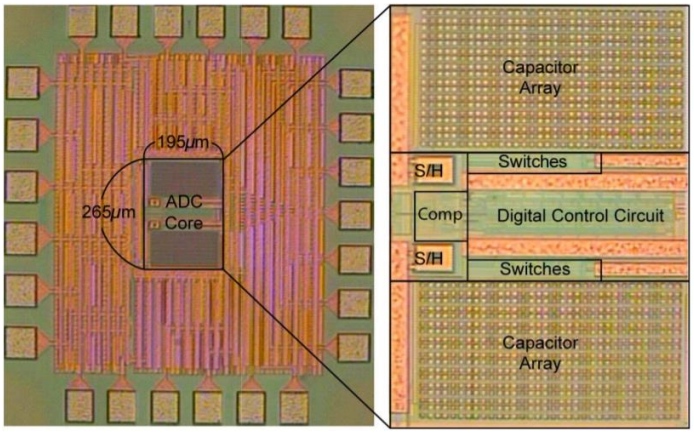


Fig -2: Die micrograph with zoomed view of architecture

4. ALGORITHM

The binary search algorithm is used in almost all the SAR ADCs [4][6][7][9][12][13][14]. Other algorithms that can be used is error-tolerant nonbinary, trial-and-error and some custom search algorithms [1][4]. Let's consider a 4-bit ADC. Hence, after getting an analog input signal, the signal is sampled into the S/H circuit and compared with the output of DAC. Initially, the SAR control logic sets the MSB to '1' and all other bits to '0'. Considering our Vref = 12 volts and input voltage (Vin) = 8.4 volts. Therefore, the control logic registers will set the input of DAC to '1000'. Corresponding with the Vref using formula Vref * (B3 / 2 + B2 / 4 + B1 / 8 + B0 / 16), we get the output voltage from DAC VDAC = 6 volts where B3, B2, B1 and B0 are the output bits from the SAR control logic i.e., MSB to LSB respectively.

Hence, this VDAC is forwarded to the comparator which then compares it to the Vin. According to the output from the comparator, which is either '1' or '0', the output bits of the SAR control logic changes [1][4]. Hence, 6 volts (VDAC) will be compared with 8.4 volts (Vin). If Vin > VDAC then the current bit (B3) will be kept as it is and the next bit (B2) will be set to '1' in the SAR control logic. Therefore, the new output from control logic comes out to be '1100', which will be again converted into VDAC and fed back to the comparator for comparison. If in this decision tree, Vin < VDAC then the current bit is set to '0' and the next bit is set to '1' and fed to the control logic. Thus, the chain goes on one bit at a time until the comparator exhausts the LSB i.e., last bit. It consumes 4 clock cycles to give the final output. Hence, N-bit ADC would require N clock cycles with conversion time (TC) = N * clock timing (TCLK). Therefore, the time required for conversion is independent of the input voltage (Vin) [1][4][12][13][14].

5. SAMPLE-AND-HOLD CIRCUIT

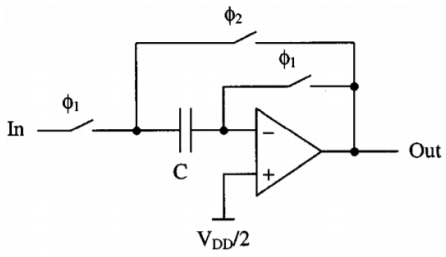


Fig -3: Typical sample-and-hold (S/H) circuit

During the binary search, the sampling of analog input and holding of sampled value is carried out by the S/H circuit [14]. As you can see in Fig. 3 from [3], S/H contains a CMOS which is used as a switch, a transmission gate to pass the voltage to the output and a capacitor [12]. Two signals are applied in the input- one is the analog input which is given to the transmission gate and other is the sampling square wave which is given to the CMOS not gate which is implemented using enhancement-MOSFETs to sample the analog input [3][4][5][10]. Refer Fig. 4(a) from [15] for CMOS layout of

S/H. This layout was made using Microwind simulation software. This software enables designers to construct CMOS layouts of desired width, length, type and placement. Before implementing any CMOS layout, the designer can also simulate his layout in this software to check the voltage or current graphs and waveforms. This can help to detect any anomaly or spikes in the structure and correct them beforehand without investing in the costs of expensive equipment.

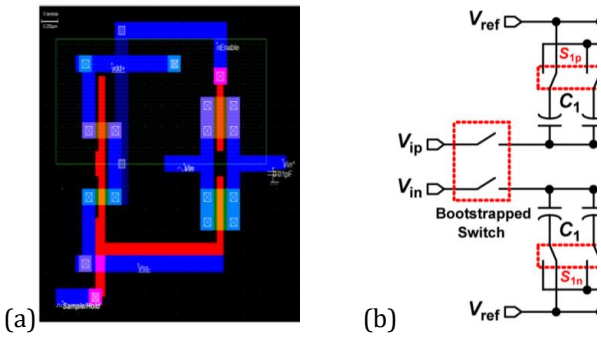


Fig -4: (a) CMOS layout of sample-and-hold (S/H) circuit (b) Bootstrapped switching schematic.

Input is a continuous analog signal, we take its samples, we get a particular digitized value which is held in the output of S/H circuit until the input is sampled again that is the sampling signal turns to low [12][13][14][15]. In the above circuit, two types of signals are there, one is the input analog voltage and other is the sampling voltage. So, depending upon the sampling voltage the waveform is generated. If the sampling voltage is high, the analog voltage is held at a certain level for a certain time depending on the on-time of sampling square signal. S/H is generally implemented using a capacitive array and the difference between consecutive samples is taken [4][5][10].

The sampling of input signal is done on top plates in case of bootstrapped switches, as shown in Fig. 4(b) from [1], in monotonic capacitor switching. This increases the settling speed and input bandwidth. And at the same time, the bottom plates are reset to Vref [1]. For slow-varying samples, we can extract samples from the least significant bits. Hence, results in low power consumption without affecting the linearity [4]. The comparator offset voltage also can be molded as a voltage source in with the S/H circuit output implying the addition of the offset to an analog input. But the major setback to this technique is high power consumption because of the isolated S/H circuit. These types of circuits are called inherent S/H circuits and is generally implemented using a binary-weighted capacitance (BWC) [1][11][12][13][14].

6. DIGITAL-TO-ANALOG CONVERTER

DAC consists of a combination of capacitive arrays majorly. These arrays are either in the form of the BWC or Capacitive ladder (C-2C). Each of the structures has its pros and cons discussed later in this paper. There are architectures which have capacitive DAC that also act as S/H circuit [1]. In DAC containing a BWC array, after sampling the analog input, it is stored in the capacitive array and then compared with the DAC for N cycles [12], as shown in Fig. 5 from [12].

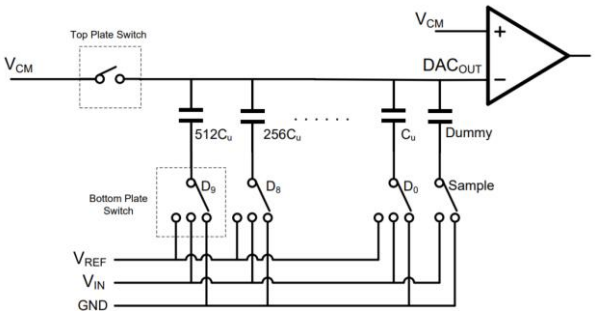


Fig -5: Typical block diagram of DAC

Conclusion In correspondence to each bit cycle in SAR ADC, only one capacitor switch is connected which not only reduces the charge transfer of the DAC network but also of the transitions of the control circuit and switch buffer. This again results in lower power dissipation. In monotonic switching DAC, the number of capacitors required is half of what is required conventionally. Also, the transistors preferred are nMOS instead of pMOS due to 1 / 3RD of the resistance required to switch. This method also eliminates the dependency on voltage discharge, i.e. from Vref / 2 to zero. The major drawback of this method is power consumption in case of unsuccessful attempt in binary search [1].

It is observed that around 75% and 43% less power is consumed for DAC and comparator respectively when simulated for Electrocardiogram (ECG) input signals compared to conventional when a hybrid design is considered. This hybrid has unary adder to on the MSB side and binary at the LSB. In contrary, the digital circuitry consumes 58% more power but the overall power consumption remains 50% less for this circuit [4]. While resetting the phase, an adequate amount of settling time is provided by the decision logic of DAC. And reset pulse-width is highly dependent on this settling time to achieve high speed. By reducing RC time constant using the same sized switches with low equivalent resistance, the settling time decreases from MSB to LSB [5].

Talking about C-2C DAC, it has advantages such as high speed, low power and compact but it introduces a concept of parasitic capacitance. This can be solved using FVS [7]. For fast stable operations, the capacitor DACs can also act as sampling capacitors [9]. In inherent DAC circuits where S/H circuit is embedded, the sampling operation is performed inside the DAC. This process is common nowadays and is called charge redistribution [11][13]. They have fewer mismatch errors comparatively and are fabricated using different architectures discussed ahead. For filtering purpose, one can place antialias and reconstruction filters before and after DAC respectively. Antialias filter is used to remove frequency components above one half of its

sampling rate which alias during the sampling whereas reconstruction filter is an electronic filter used to eliminate frequencies greater than the Nyquist rate [14].

7. COMPARATOR

Comparator consists of two input terminals, as shown in Fig. 6 from [12], VIN+ and VIN- where analog input voltage is supplied. If the voltage on VIN+ is less than VIN- then '0' is obtained on VOUT. But if VIN- is greater than VIN+ then '1' is obtained. Hence, it is sometimes quoted as "single-bit ADC". Comparator is made up of simple logic gates [12].

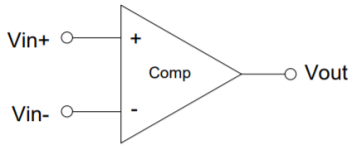


Fig -6: Comparator Block Diagram

In monotonic capacitor switching, the sampling is done on the top plate. This allows comparator to perform the first comparison without any capacitor switching. And hence, this is the main reason for reduced capacitor arrays to 50% in bootstrap switches [1]. A conventional comparator common-mode range is limited to current-voltage (I-V) operations. And while being in the mid-range of supply rails, it may not be possible to switch. Therefore, latched comparator can be used for wide input swing. The offset error, in this case, depends on the MOSFETs and resistors. This offset doesn't affect the overall linearity but affects global offset which can be digitally removed [3][5]. Traditionally, the reset phase terminates the comparator after it is settled with the proper input voltage.

Metastability is a fundamental issue of all the ADCs which relies on comparator for conversion. Using single comparator eliminates the need to calibrate multiple comparators as in the case of flash ADC. Metastability is when a comparator consumes prolonged time approximating an arbitrarily small input. This is solved by setting a minimum base value which causes loss of bits under than certain value. Hence, this can lead to large errors (sparkle codes) which increases exponentially with an increase in sampling frequency [5]. By using two comparators the metastability can be avoided but this requires more area and calibration of offset. So, a comparator with a multi-stage amplifier can be used instead to increase accuracy at comparison time [9]. Propagation delay is said to be the decision time of a comparator whereas the comparison rate is the highest frequency at which correct value is obtained. Due to the large variation of voltage at an internal node, kickback noise is generated at input nodes of the comparator. This is reduced by pre-amplifier before latch and isolation of input nodes using cascade transistors. This type is beneficial to detect small voltage changes and exhibits speed-gain tradeoff. clocked/latched comparators work on positive feedback and amplification [12].

8. CONTROL LOGIC

SAR control logic consists of a ring counter which is spread across two parts, one for the control logic and another for the comparator. These consist of D flip-flops designed using transmission gates. Control logic is dependent on output from the comparator. According to the output, the shift registers in the control logic decide whether to shift the output of the ring counter. This makes this system based on asynchronous clock network. As after output from the previous flip-flop, the next register works at the next cycle's rising edge. Hence, here the output from flip-flop is considered as a clock signal. Reset signal is turned to high after each signal [10], as shown in Fig. 7 from [12].

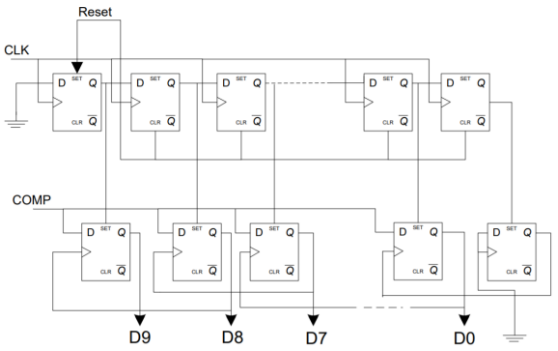


Fig -7: SAR Control Logic block diagram

This method was theorized by Anderson. While there is also one more method by Rossi consisting of N flip-flops and combinational logic [12][13]. The control logic successively resets the bottom plate from MSB to LSB [7]. We know that the algorithm used is a binary search in the SAR control logic. Hence, the logic used is iterative which makes scalability of this technique easy. One can simply add more shift registers to the circuit and implement the same algorithm. This results in higher resolution of ADC but also changes power consumption and propagation delay accordingly. In the same paper, delay line-based control logic is also discussed. In this type, a mutable array containing different clock delay line is used. And according to the RC time constants, each delay element determines it's a delay. Therefore, varying total resistance or capacitance could lead to changed delays. But due to noise of power supplies, there can be jitter in the generated clock. This paper also explores three types of delay line mainly inverter-based, current-starved based and capacitive controlled [12].

9. ASYNCHRONOUS CLOCK

In SAR ADC, an asynchronous clock is used [1]. It makes average conversion time shorter as compared to synchronous [5]. In an N bit SAR ADC, the time complexity required is N cycles to approximate one input voltage. Hence, it is necessary to select the clock according to the application else it will consume more time and power. For selecting proper clock duration, Resolution has to be calculated using Vref / (2N) [4]. The reason for not selecting a synchronous

clock is due to its limitation on high-frequency application. As this type of clock heavily relies on the clock to divide equal slots for conversions. Hence, an internal asynchronous clock of N bits ADC will operate at least (N * sampling clock) and would require (N * clock power) where highest clock rate is the sampling frequency. Except for the N clock cycles required to obtain output, additional M cycles are required at start to sample the analog input signal [7]. And this accounts to be about 15% of required clock power as compared to more than 50% of a synchronous clock.

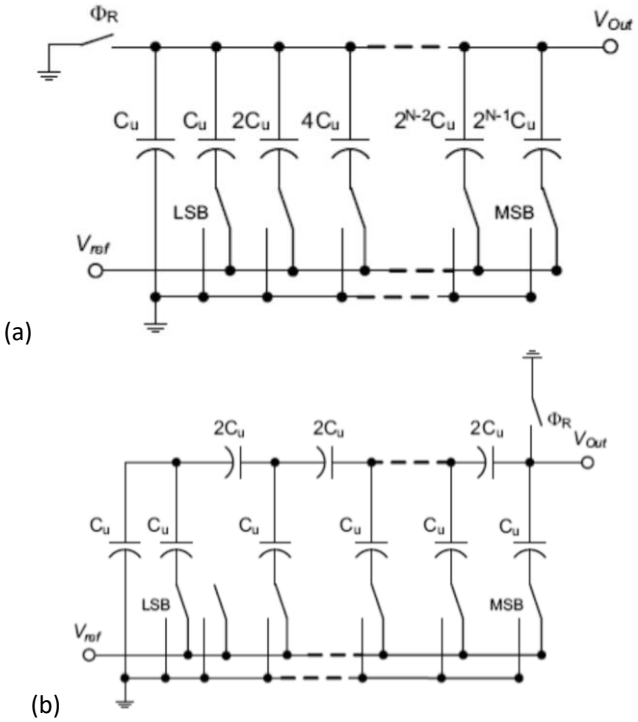
One important fundamental issue is related to metastability. Hence, to avoid this degradation of an effective number of bits (ENOB) asynchronous clock is used which supports simple algorithm for metastability detection [5][9]. If there is a continuous change at output voltage then the regulated clocked current mirror (RCCM) can be used dynamically while providing constant current [6]. Similarly, a two-stage pipelined structured could be used consisting of two DACs and asynchronous clocks for flexible clocking scheme and allocating available time to sub-DACs which reduced the ENOB loss as less as 0.42 bit at sampling frequency 10KHz [8]. But while designing multi-level architecture ensure to take into consideration clock bootstrapping which results in a larger area at extremely low voltage to reduce on-resistance. This is because of the continuous charging and discharging of the bootstrapped capacitors [7]. Hence, one of the disadvantages of this is prolonged decision time resulting in the metastable state [9]. Coupling clocks for a multi-level circuit, spurs are created. Spurs are harmonics of input frequency due to nonlinearities in the ADC or at subharmonics of sampling frequency. And the Spurious-free dynamic range (SFDR) is the ratio of the input signal to peak spur component [11]. And to avoid any missing code after assigning a fixed delay for each operation, one can use DAC's tunable delay element to get access to variable redistributable time for switched-capacitor [8].

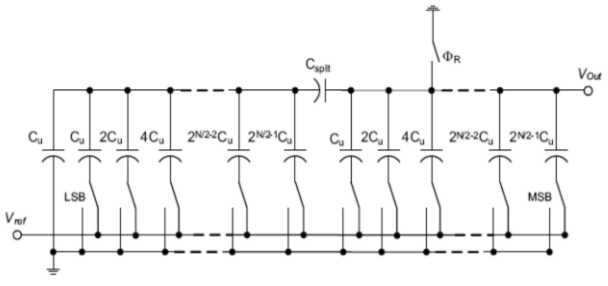
10. CAPACITIVE ARRAY

In SAR ADC capacitance is used in both acquisitions as well as conversion phase. In the conversion phase at the start, the analog input voltage is stored inside the sample-and-hold capacitor. The capacitive DAC consist of an array of binary capacitors, so at the start when the reference and S/H switch is open no comparison happens. After turning ON the switches, the S/H capacitor charges the capacitive array depending on the number of bits. This is known as redistribution mode [12]. This arrays' capacitance is compared with the reference voltage (Vref) one channel at a time by toggling the switches. The comparison is possible because of the grounding/inverted design of the array. With each cycle, only the comparing capacitor is connected to the Vref and all remaining to the ground. And after comparison through a comparator, the value is stored in SAR. Hence, the analog input is converted to binary and is compared using Vref [1][2][3][4][12].

Two methods of manufacturing these capacitive arrays could be Metal-Insulator-Metal (MIM) and Metal-Oxide-Metal (MOM). And by enclosing the top plate into the bottom plate in a sandwich capacitor reduces the parasitic capacitance. And since capacitors occupy most of the area in SAR ADC, the increasing unit capacitance can improve area efficiency [1]. Switching scheme efficiency can be determined by the average energy required for charging and discharging the capacitors [2]. Conventionally, the value of each capacitor can be given by $C_i = C_0 * 2^{N-i}$ where N is the converter resolution and C0 is the unit capacitance along with one extra capacitor C0 at LSB [4].

The major architectures of capacitive arrays are Binary-weighted capacitance (BWC), Two-stage weighted capacitance (TWC) and Capacitive ladder (C-2C), as shown in Fig. 8(a), 8(b) and 8(c) from [12]. There are also resistive ladder arrays but as we know resistor consumes more power and also mismatching error. BWC is nothing but the conventional capacitive array whose capacitor formula is mentioned above. And based on the formula, the total capacitance comes out to be $C0 * 2^N$. In TWC array, the BWC is sub-divided into two smaller BWC. This sub-division is coupled by a coupling capacitor. About C-2C ladder, it can be said to be an extension of TWC. The main motive of this architecture is high-speed by reducing per capacitance value drastically [12].





(c)

Fig -8: (a) BWC array (b) C-2C ladder (c) TWC array

11. PERFORMANCE PARAMETERS

Performance parameters can be classified as elements due to which the output efficiency/linearity is dependent. The main parameters when talking about ADC are offset error, gain error, Differential (DNL) and Integral (INL) nonlinearity [1][2][3][5][6][7][9][11][12]. One of the major parameters discussed above was parasitic capacitance which affects the linearity of the ADC [7]. Parasitic capacitance is the unwanted stray/virtual capacitance is built when electronic components or conducting tracks are brought close to each other. Due to this C-2C are restricted to low resolution but FVS can help reduce this, as shown in Fig. 9 from [7]. In parasitic capacitance, it is only generated over the bottom plate. The negligible effect is observed on the top plate and hence similar voltage is created to those floating nodes through the use of secondary capacitor array. This largely reduces the voltage drop between the plates and overall linearity is improved [1][5][7].

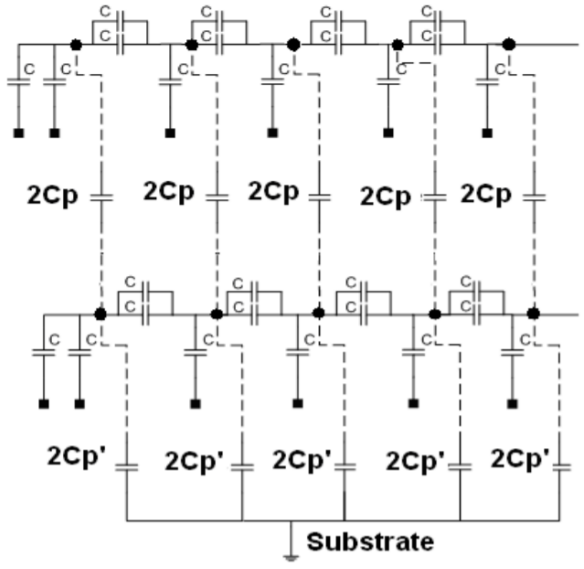
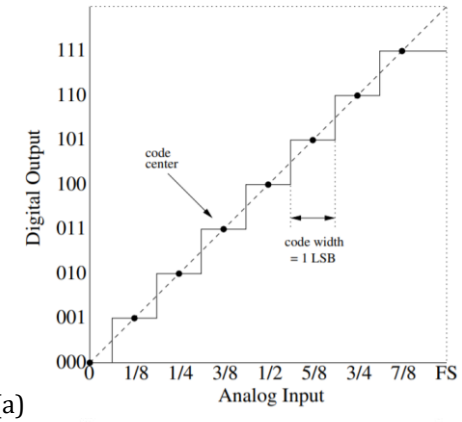
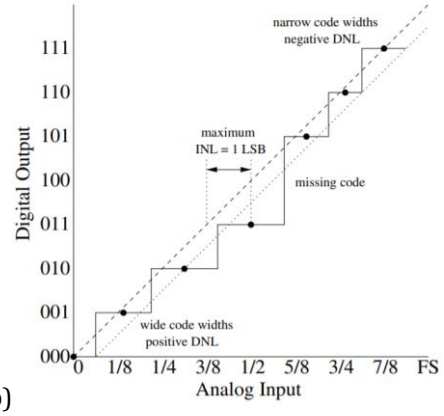


Fig -9: FVS C-2C DAC to avoid Parasitic Capacitance

Gaussian distributed (N (0, σ2)) is the variation in unit capacitance where σ is the standard deviation of matching [2]. This mismatching can be because of offset error, i.e. deviation of ADC output at zero. The deviation of actual transition voltage from half of LSB. Similarly, gain error can be defined as a change in slope from original, i.e. full-scale voltage. Both these linear errors can be eliminated by calibration. But due to nonlinearity in the system, there can be a deviation of the transfer function, as shown in Fig. 10 from [11].



(a)

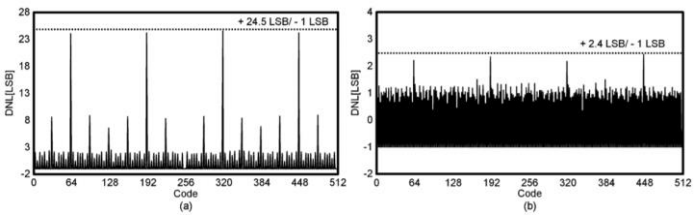


(b)

Fig -10: Characteristics
(a) Ideal ADC
(b) ADC with nonlinearities

This introduces the DNL and INL factors. DNL refers to the transition of code width. Positive and negative DNL corresponds to narrow and wide width respectively. Whereas INL is the distance between the best fit line and the code. And where ever the code is missing, DNL equals '-1' [11][12]. Therefore, based on these parameters the performance of a SAR ADC can be evaluated, as shown in Fig. 11 from [9]. On the left side, it shows waveform without calibration and binary search where right shows with calibration and binary search. So, we can see how much calibration affects the final performance of a DAC.

(a)



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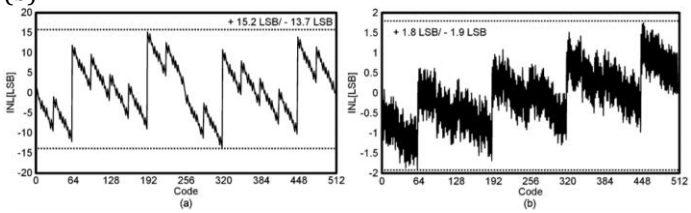

Fig -11: Performance of
(a) DNL parameter
(b) INL parameter

12. CONCLUSIONS

SAR ADC is indeed one of the most efficient ADC available. This is because of its Power efficiency, complexity, Conversion Rate which is hundreds of times better than conventional Flash, Delta-sigma or Dual slope ADCs. This impacts the overall efficiency and its flexibility. This paper stated it's a basic architecture which are S/H circuit, Comparator, SAR control logic and DAC. Along with the binary search algorithm, the building blocks were studied thoroughly through various references and effects of each parameter were presented. Many solutions like FVS, pipelining to fundamental issues of parasitic effect, metastability, jitters and mismatching were provided. Different internal architectures of capacitive arrays namely BWC, TWC and C-2C and also how sampling, holding and comparison is done on the component level was reviewed. And finally, parameters for judging the performance of ADC including offset error, gain error, DNL and INL were briefed. This paper consists of technological advancements over about span of a decade and tries to summarize all the aspects.

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