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Advance Dynamic Voltage Restorer

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Abstract - *A power electronics switching based ac-ac proposed converter. It Compensates both the voltage sag and swell and used as dynamic voltage restorer. trying to minimized demerit of conventional dynamic voltage restorer. It can achieve proper switching of electronics switches as means turn on and commutation methods. It can archives using power MOSFET's without body diode connected. External diode can provide proper reverse recovery features can prevent relevant loss and increase reliability.*

Key Words: DVR,dynamic voltage restorer, power electronics, Voltage sag and swell, DVR, commutation, MOSFET.

1.INTRODUCTION

The fast developments in power electronic technology have made it possible to mitigate voltage disturbances in power system. There are different types of disturbances occurring in power system, voltage sag is known to produce the most devastating impact on the loads. Studies show that 92% of all disturbances in the electrical power distribution systems are voltage sags, transients, and momentary interruptions. The need for better power quality has prompted the end users to install power conditioning equipment to mitigate voltage sags. One such series custom power device is dynamic voltage restorer (DVR). It consists of a voltage source inverter (VSI) to inject voltage in series with the line, injection transformer, and a dc link, where the energy is stored using dc capacitors or battery energy storage. DVR is not adequate for compensating deep and long-duration voltage sags. Contradictory to this, as per the sensitive load concern, deep and long-duration sags are more vulnerable than shallow and short-duration sags. The magnitude and ride-through capability of the compensator depend on the size and capacity of the storage device. Poor reliability of the storage devices and variation in the dc bus voltage may compromise the sag compensation performance. A system-wide addition of DVRs is hindered because of high cost, in particular, due to the expensive energy storage devices. Use of batteries has raised many environmental concerns. Further, the voltage regulation of the dc link demands the use of a separate ac–dc converter, which requires one more stage of power conversion. Thus, the compensator size, cost, control complexity, and power losses will increase. The DVR based on a direct ac-ac converter saves the bulky DC-link capacitors and the additional ac-dc power-processing stage[3][7].

The traditional buck, inverting buck-boost, non-inverting buck-boost, and the Cuk direct PWM ac-ac converters are the common topologies. However, they have unipolar voltage gains and can compensate either voltage sag or swell [1][4]. The ac-ac converters with bipolar voltage gain can compensate both voltage sag and swell. The Z-source ac-ac converters have bipolar voltage gains; however, the sharp rise and fall in its gain during the NIB operation is quite challenging for the controller. In addition, the high voltage and current stresses of the switches decrease its efficiency. Above drawback can be overcome to new propose of dual-buck structure.

Recently, new single-phase and three-phase ac-ac converters using the dual-buck structure are proposed. They do not have short-circuit and open-circuit issues, and they do not require RC snubbers and soft commutation strategies [1][2][3]. Further, they can use MOSFETs without their body diodes conducting. However, they generate circulating currents, and to limit their circulating currents they require coupled inductors. To decrease the magnetic volume of the coupled inductors in, the separate coupled inductors are integrated into one core in. To further decrease the magnetic volume, the filter inductor in is eliminated by utilizing the leakage inductance of the integrated coupled inductor in In, cascaded multilevel converter based on the single-phase converter is proposed. The converters in generate circulating currents, and to eliminate their circulating currents, modified ac-ac converters using separate filter inductors are proposed in[5]. However, all of these converters have unipolar voltage gains and can compensate either voltage sag or swell in a DVR. In, a high-frequency isolated double step-down ac-ac converter is proposed. It has a buck function with a bipolar voltage gain. However, its output peak voltage cannot exceed half of the input peak voltage; therefore, its range to compensate voltage sag or swell is limited. Further, it is associated with the circulating current of, which decreases the efficiency.

In our paper we model of advance DVR simulate in MATLAB software.

2. PRAPOSED CONVERTER

Fig. 3 shows the schematic diagram of the proposed converter. a MOSFET is connected in series with an external diode, and each cell is connected to a separate inductor. Therefore, the proposed converter has no shoot-through issues. The inductors (L1–L4) store energy, oppose shoot-through, and avoid current flow through the body diodes of the MOSFETs (S1–S8). The current freewheeling external

diodes (D1–D8) of good reverse recovery features can be used, owing to which the reverse recovery loss and issues can be minimized. As aforementioned, the proposed ac-ac converter has no shoot-through concerns; therefore, large dead-time in the gating signals and RC snubbers are not required. C1–C4 are attached to avoid voltage spikes in unwanted dead-times between the switches. They also serve as filtering capacitors. In this paper, L1–L4 are assumed to have the identical inductance L, and the operating modes are shown only for $vo > 0$.

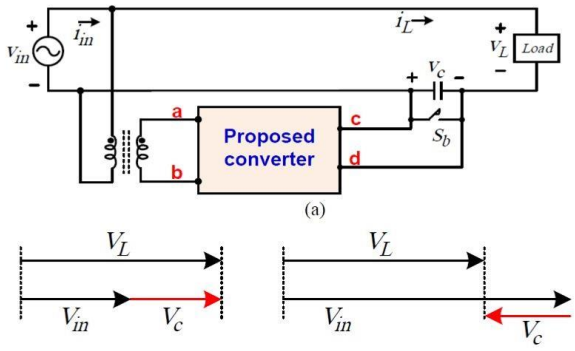


Fig-1: (a) Proposed DVR. (b) Vectors associated with Vin, Vc, and VLQ

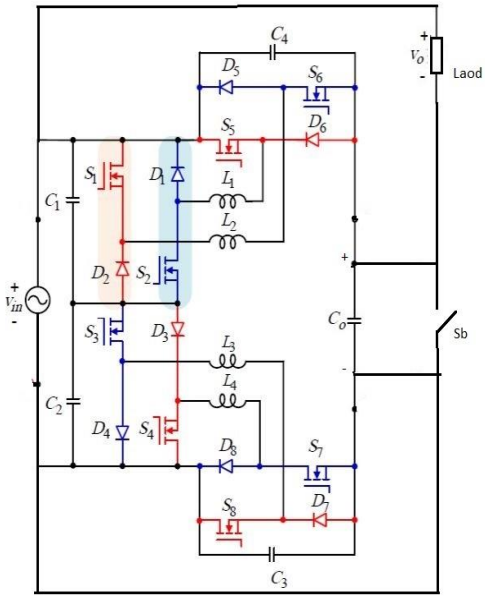


Fig -2: Circuit diagram of Advance Dynamic Voltage Restorer

3. INVERTING AND NONINVERTING OPERTION

The gate-signal generation in an INIBB operation is shown in Fig. 3, where D2 is the ON time of S1, S4, S6, and S7 in one switching cycle. All the switches are switched at a high frequency. In this operation, an output voltage greater or lower than the input voltage, and in-phase or out-of-phase to the input voltage can be obtained. In this operation, the converter has two operating modes in a switching cycle.

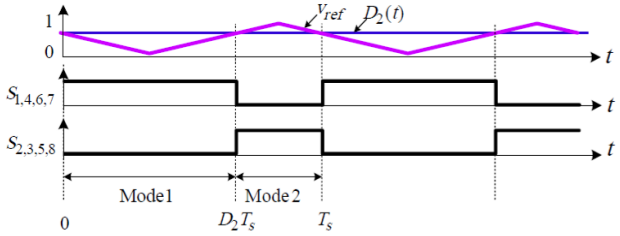


Fig-3: (a) Gate-signal generation in Inverting and non-inverting operation.

A. Mode 1 [0 – D2 Ts]

As shown in Fig. 4(a), S1, S4, S6, S7 are ON, and S2, S3, S5, S8 are OFF.

$$\frac{di_{L2}}{dt} = \frac{v_{in} - v_o}{2L}, \quad \frac{dv_{C_o}}{dt} = -\frac{i_{L2} - i_o}{C} \tag{1}$$

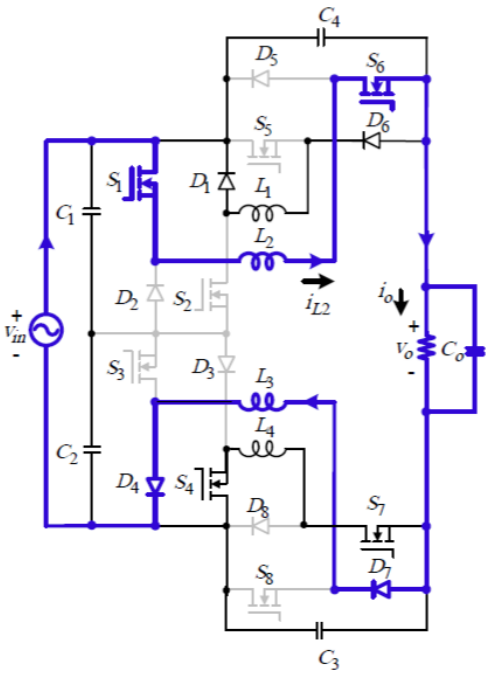


Fig -4: (a)Circuit diagram of Advance Dynamic Voltage Restorer

B. Mode 2 [D2 Ts – Ts]

As shown in Fig. 4(b), S1, S4, S6, S7 are OFF, and S2, S3, S5, S8 are ON.

$$\frac{di_{L2}}{dt} = -\frac{v_{in}}{2L}, \quad \frac{dv_{C_o}}{dt} = -\frac{i_o}{C} \tag{2}$$

The voltage gain (MC) in an INIBB operation can be obtained as

$$M_C = \frac{v_o}{v_{in}} = \frac{2D_2 - 1}{D_2} \quad (3)$$

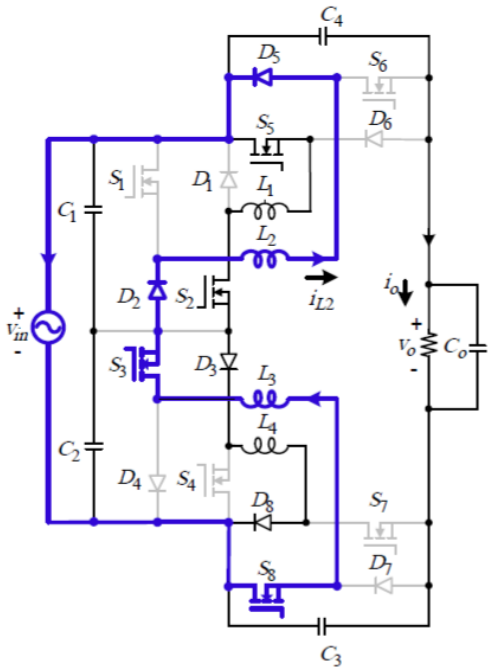


Fig -4: (b)Circuit diagram of Advance Dynamic Voltage Restorer

4. SWITCH VOLTAGE AND CURRENT STRESSES

In this section, the voltage and current stresses of the switches are normalized to Vo and Io , respectively, and the results are expressed in terms of voltage gain (G).

1) Voltage stress: The INIBB has NIB and IBB operations. In the NIB operation, the normalized voltage stresses are obtained as

$$\begin{cases} \frac{V_{stress(S_{1-4})}^{inibb(nib)}}{V_o} = \frac{1}{G}, \frac{V_{stress(S_{5-8})}^{inibb(nib)}}{V_o} = \frac{1}{G} - 1 \end{cases} \quad (4)$$

In an IBB operation, G is negative. Thus, by inputting negative G in (4), the normalized voltage stresses are obtained as

$$\begin{cases} \frac{V_{stress(S_{1-4})}^{inibb(ibb)}}{V_o} = -\frac{1}{G} \\ \frac{V_{stress(S_{5-8})}^{inibb(ibb)}}{V_o} = -\frac{1}{G} + 1 \end{cases} \quad (5)$$

2) Current stress:

$$\frac{I_{stress(S_{1-8})}^{inibb}}{I_o} = 2 - G \quad (6)$$

5. PARAMETER DESIGN

In this section, the guidelines for the parameter selection are given.

1) As given in Table I, the peak input voltage Vin =[110 – 200] V, the peak output voltage Vo = 155.5 V,and the switching frequency fsw = 50 kHz. In the buck operation $Vin.max$=200 V, in the boost operation $Vin.min$=110 V.

2) The maximum voltage stress of $S1$–$S4$ is $Vin.max$, and that of $S5$–$S8$ is $Vin.max$+Vo=355.5V.

3) To obtain the same Vo=155.5 V in various operations, the duty ratios can be obtained as

$$\begin{cases} D_{min} = \frac{V_o}{V_{in.max}} = 0.78 \\ D_{1.min} = \frac{1}{1 + \left(\frac{V_{in.max}}{V_o}\right)} = 0.44 \\ D_{1.max} = \frac{1}{1 + \left(\frac{V_{in.min}}{V_o}\right)} = 0.58 \end{cases} \quad (7)$$

4) The peak output current is obtained as

$$Io = 2Po/Vo = 3.86A \quad (8)$$

5) Using (7) and (8), the inductor currents in various operations can be obtained as,

$$I_{inibb}^{ibu} = \frac{I_o}{D_2^{ibu}} = 10.7\ A, \qquad I_{inibb}^{ibo} = \frac{I_o}{D_2^{ibo}} = 13.3\ A \quad (9)$$

Thus,
the maximum current stress is 13.3 A in the IBo mode of an INIBB operation.

6) By considering inductor current ripple ki=25% of the currents in (9), the inductances can be obtained as.

$$L_{inibb}^{nib} = \frac{V_{in.max} \cdot (1 - D_2^{nib})}{2 \cdot f_{sw} \cdot k_i \cdot I_{inbb}^{nib}} = 0.306\ mH$$

$$L_{inibb}^{ibu} = \frac{V_{in.max} \cdot (1 - D_2^{ibu})}{2 \cdot f_{sw} \cdot k_i \cdot I_{inbb}^{ibu}} = 0.478\ mH$$

$$L_{inibb}^{ibo} = \frac{V_{in.min} \cdot (1 - D_2^{ibo})}{2 \cdot f_{sw} \cdot k_i \cdot I_{inibb}^{ibo}} = 0.235\ mH \quad (10)$$

The maximum required inductance is 0.478 mH in the buck mode of an INIBB operation.

(7)The capacitance of Co to maintain an output voltage ripple kv=6 % of vo in various operating modes can be obtained.

$$C_{inibb}^{ibu} = \frac{I_o \cdot (1 - D_2^{ibu})}{f_{sw} \cdot k_v \cdot V_o} = 5.31\ \mu F$$

$$C_{inibb}^{ibo} = \frac{I_o \cdot (1 - D_2^{ibo})}{f_{sw} \cdot k_v \cdot V_o} = 5.89\ \mu F \quad (11)$$

Therefore, the inductance of each inductor is chosen as 0.5 mH, and the capacitance of the output capacitor is chosen as 6.8 μF.

Output voltage	155 Vpeak/50Hz
Input voltage	110-200Vpeak/50Hz
Output power	300W
Switching frequency	50KHz
MOSFET S1–S8	47N60CFD
Diode D1–D8	RHRG306
Inductor L1–L4	0.5 mH
Capacitors C1–C4	2.2 µF
Output capacitor Co	6.8 µF
Controller	TMS320F28335

TABLE- 1: ELECTRICAL SPECIFICATIONS

6. DVR

Fig. 13(a) shows the proposed DVR, and Fig. 13(b) shows the vectors associated with the voltages. In Fig. 13(a), vL is the load voltage, vin is the input voltage, vc is the output voltage of the converter, and VL, Vin, and Vc are their peak values. As shown, when Vin<VL, the converter generates a positive Vc=VL–Vin , which is then added to Vin to compensate voltage sag. Similarly, when Vin>VL, the converter generates a negative Vc, which is then added to Vin to compensate voltage swell. From Fig. 13(a), we obtain

$$vL = vin + vC \quad (12)$$

The output voltages of the converters (vo=vc) INIBB operations are given in (3).By using vo=vc from these equations in (12), the load voltage can be obtained as

$$v_{L3} = \left(1 + \frac{2D_2 - 1}{D_2}\right) \cdot v_{in} \quad (13)$$

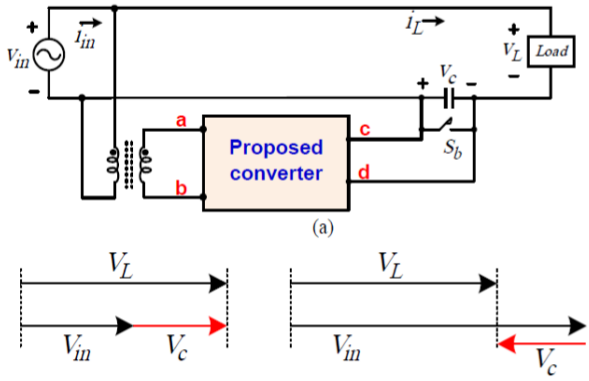


Fig -5: (a) Proposed DVR. (b) Vectors associated with Vin, Vc, and VL

The load voltage gain (vL/vin) from (25) is plotted in Fig. 14.In NIB operation, only the voltage sag can be compensated, and a maximum of 50% voltage sag can be compensated. In an IBB operation, only the voltage swell can be compensated, and ideally 100% voltage swell can be compensated. In an INIBB operation, the voltage sag can be compensated for $D2$ > 0.5, and the voltage swell can be compensated for $D2$ < 0.5. Ideally, in an INIBB operation, 50% voltage sag and 100% voltage swell can be compensated. Thus, to compensate both the input voltage sag and swell, two operations can be used: 1) INIBB operation with one control variable $D2$.

A. Bypass Mode

In practice, when Vin = 0.9$Vref$ – 1.1$Vref$, the input voltage is considered in the nominal range, and the bypass mode is activated. In the bypass mode, switch Sb in Fig. 5(a) is turned ON and the switches of the converter do not need to be actively controlled. Thus, the gate lock operation is implemented and all the converter switches are turned OFF. When Vin is not in the range (0.9$Vref$ – 1.1$Vref$), Sb is turned OFF and the converter is activated and controlled by a closed-loop controller. In closed-loop control, VL is compared with $Vref$. To obtain VL from vL , the widely used peak voltage detector shown in Fig. 6 is used. As shown in

Fig. 7, VL is then compared with $Vref$ to obtain an error signal $e(t)$, which is given into a PI Controller . The PI controller compensates $e(t)$ and a control signal $u(t)$ is generated. In Fig. 7, Kp and Ki are the proportional and integral gains of the PI controller, respectively.

B. Operation

The control block diagram in an INIBB operation is shown in Fig. 17. VL is compared with $Vref$ and an error signal $e(t)$ is obtained, which is given into the PI controller. The PI controller compensates the $e(t)$ as shown in Fig. 16, and the control signal $D2(t)$ is generated. $D2(t)$ is compared with a carrier signal [see Fig. 8] to obtain the switching signals.

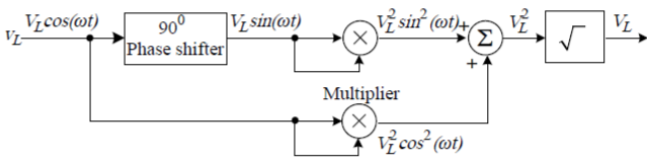


Fig -6: Peak voltage detector [8].

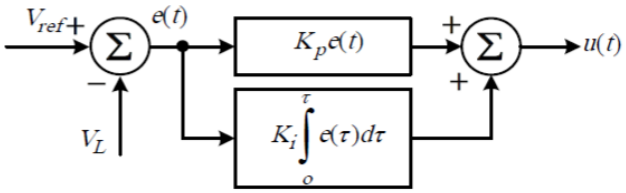


Fig -7: Block diagram of PI controller.

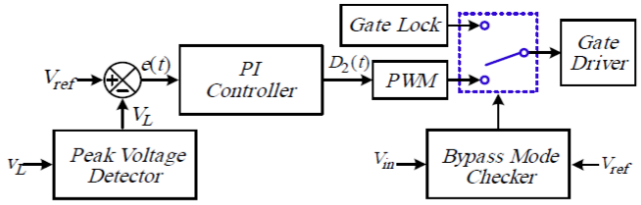


Fig -7:. Block diagram of the closed-loop control in INIBB operation for DVR.

7. EXPERIMENTAL RESULTS

A 300-W laboratory prototype is fabricated and tested successfully. The design specifications of the converter are

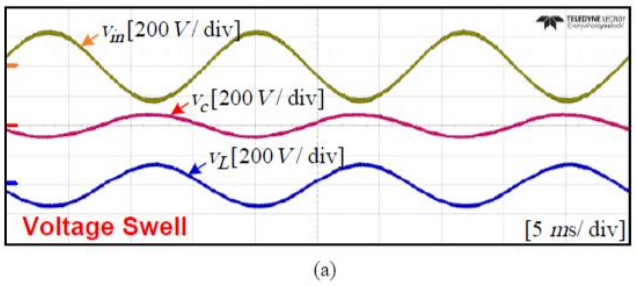
given in Table I. During the experiments, safe commutation is achieved without using soft commutation techniques and lossy snubbers. The experimental results in Figs. 19–24 are obtained with resistive loads.

1) Non-inverting buck mode: Fig. 22 shows the results in the non-inverting buck mode when Vin = 198 Vpk , Vo = 155.5 Vpk, and D2= 0.825.

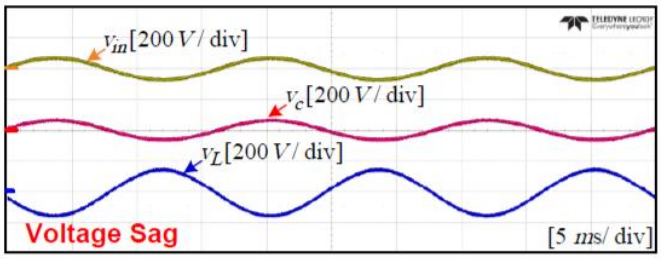
2) Inverting buck mode: Fig. 23 shows the results in the inverting buck mode when Vin = 198 Vpk, Vo = 155.5 Vpk, and D2= 0.3589.

3) Inverting boost mode: Fig. 24 shows the results in the inverting boost mode when Vin = 113 Vpk, Vo = 155.5 Vpk, and D2= 0.296.

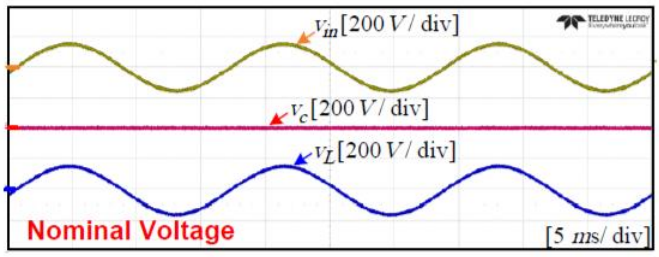
Fig. 26 shows the experimental results with non-linear load in NIB operation. The non-linear load consists of a full-wave diode rectifier followed by a DC-link capacitor of 470 µF. To verify the operation of the proposed DVR [see Fig. 13(a)], the experimental results under the input voltage swell, voltage sag, and nominal voltage are provided in Fig. 27. The load voltage vL is regulated at 155 Vpk .



(a)



(b)



(c)

Fig-9: Experimental results of the proposed DVR.

Nominal Voltage: As shown in Fig. 9(c), when Vin = 155 Vpk (nominal value), switches ($S1 - S8$) are turned OFF, and

(Sb) is turned ON to bypass vin to vL. As shown in Fig. 9, for all the three cases, VL is regulated at 155 Vpk, which verifies the operation of the proposed DVR.

8. CONCLUSION

In this paper, a Advance Dynamic Voltage Restorer is proposed. It combined the operations of non-inverting buck and inverting buck-boost converters in one structure. Similar to the buck converter, it has a inverting non-inverting buck-boost operation. In addition, it has an extra operation, in which the output voltage higher or lower than the input voltage that is in-phase or out-of-phase with the input voltage can be obtained. Thus, the proposed converter can compensate both voltage sag and swell when used in a DVR.

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