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Space-Vector Modulation of a Three-Level NPC-Inverter

Sudhanshu Bhatnagar[1], Shivang Tiwari[2], Tarun Mahawar[3], Saumya Pancholi[4], Bharat Modi[5]

[1,2,3,4]UG Student, Department of Electrical Engineering, SKIT, Jaipur, 302017(India)
[5]Associate Professor, Department of Electrical Engineering, SKIT, Jaipur, 302017(India)

Abstract: Multilevel inverter consists of several power switches having capacitive voltage source. It generates collective step voltage waveform with variable-frequency phase and amplitude. It offers several advantages compared to a standard 2-level inverter in terms of reduced harmonic distortion in output waveform without using any type of filter circuit, lower switching frequency hence higher efficiency is achieved, and reduced stress from the load. A multilevel inverter is utilized in applications that require a lot of power and good power quality. This paper introduces a 3-level Neutral-Point-Clamp inverter using space vector pulse width modulation approach as a control strategy simulation model developed and designed in MATLAB software. SVM methodology determines the pulse width modulated signals for inverter switches to bring out the desired 3-phase voltage.

Keywords: **N**eutral-Point-Clamped, Space Vector Modulation (SVM), Multilevel Inverter

1. INTRODUCTION

Researchers are particularly interested in multilevel inverters in applications involving high power such as use and big motor drive applications (Peng, 2000) [1]. Due to the limits of normal output inverters in managing big power conversions, the multilayer inverter's input is amplified. Multilevel inverters can be upgraded using multiple three-phase bridges or by increasing the number of switching devices per phase, to increase the number of levels.

The concept of a Multilevel inverter involves the use of a series of switching devices in the series to perform power transformations in small increments of power steps by combining the power of stairs from several levels of DC capacitor voltages (Skvarenina, 2002; Soto and Green, 2002; Rodriguez et al., 2002) [2][3][4].

The benefits of a multilevel inverter include reduced dv/dt stresses on switching devices due to small voltage step increments, reduced electromagnetic compatibility (EMC) when operating at high voltage (Skvarenina, 2002) [2], smaller rating of semiconductor devices (Lai and Shyu, 2002) [5], and better output voltage features such as less distortion, lower harmonics content, and lower dv/dt (Feng and Agelidis, 2004; Peng, 2000) [6]. In addition, flexible phase switches required for most high-voltage inverters are less required, thus helping to reduce costs.

As the number of levels increases, so does the number of switching devices and other components, making the inverter more complex and expensive. One of the drawbacks of multilevel inverters is this. To control and synchronize the switching devices, a complex controller with a properly related gate drive circuit is required. The greater the number of levels, the greater the number of DC capacitors used, which may cause voltage imbalance among the DC capacitors, resulting in overvoltage in one or more of the switches. However, the situation can be improved by employing voltage clamping or a capacitor charge control circuit. (Mouton, 2002) [7].

The majority of research on multilevel inverters focuses on the modulation techniques used to control the switching devices in the inverters. Voltage imbalance in series stacking capacitors has been investigated, and a comparison study of the performance of each type of multilevel inverters, such as the Neutral-Point-Clamped (NPC), Flying Capacitor (FC), and H bridge cascaded (HBC), has also been performed and analyzed.

McGrath and Holmes (2002) [8], investigated PWM strategies for the Diode Clamped inverter, Cascaded inverter, and hybrid inverter in their paper. It had been identified that for Diode Clamped inverter, Phase Disposition (PD) Pulse-Width-Modulation (PWM) outperformed Alternative Phase Opposition Disposition (APOD) PWM in terms of spectral performance. This is because significant harmonics energy was placed in the main carrier component and these components were cancelled between phase legs when the line-to-line voltages were formed. It was also discovered that the APOD PWM of the Diode Clamped inverter achieved similar harmonic performance as the Phase Shifted Carrier (PSC) PWM of the cascaded inverter and three-level hybrid inverter. Based on the research, an equivalent PD PWM strategy for cascaded inverters and hybrid inverters was developed, which will provide similar harmonic performance as PD PWM for Diode Clamped inverters.

In their research, Gupta and Khambadkone (2005) [9], proposed a simple Space Vector Pulse Width Modulation (SVPWM) for operating a 3-level NPC inverter at higher modulation indices, including an over-modulation region with neutral point balancing. As per the experimental results, the proposed scheme works well for any type of load and is computationally simple, enabling it to be implemented in a DSP or microcontroller.

Nguyen et al. (2005) [10] investigated a 3-dimensional Space Vector Modulation (SVM) scheme for a 3-level NPC converter to solve the problem of voltage imbalance in the NPC converter. As per simulation and practical results, the proposed scheme exceeds the traditional 2-dimensional scheme in terms of harmonics performance. The benefits of low harmonics and fewer switching transients may allow for cost and size reductions.

Besides these aspects of the investigation, the harmonics contents of the voltage and current output of the multilevel inverters are of considerable interest in this work. Multiple researches have been carried for various types of multilevel inverters and control strategies.

Zambra et al. (2008) [11] compared three topologies of PWM multilevel inverters used to drive a 500kVA/4.16kV induction motor. Neutral Point's performance, the total harmonic distortion, first-order distortion factor, semiconductor power losses distribution, and heat-sink volume of clamped, symmetrical cascaded, and hybrid asymmetrical cascaded multilevel inverters have been studied.

This paper is organized as follows: In section 2, a brief review of the Neutral-point-clamped (NPC) multilevel inverter and its working principle is presented. Next, the applied algorithm is explained in detail in section 3. In section 4, the Simulink model developed is presented. Simulation results are provided in section 5 to emphasize the effectiveness of the method. Finally, some conclusions are provided at the end of the paper.

2. NEUTRAL-POINT-CLAMPED (NPC) MULTILEVEL INVERTER

The Neutral-Point- Clamped multilevel inverter, also referred to as the Diode Clamped multilevel inverter, is one amongst the multilevel structures that has attracted a plenty of attention and is widely used. Nabae et al. proposed this structure for the primary time in 1980. (Krug et. al., 2004; Marchasoni and Mazzucchelli, 1993) [12] [13].

A multilevel inverter is a power electronic device that can provide the desired alternating voltage level at the output by taking multiple lower-level DC voltages as input. These inverters are the industry's preferred choice for high voltage and high-power applications. Multilevel inverter technology has recently emerged as a critical alternative in the field of high-power medium-voltage energy control. Several multilevel structures exist, including the cascaded H-bridge inverter, Neutral point clamped inverters, flying capacitor multilevel inverter, and modular multilevel inverter. Multilevel inverters are preferred mainly because of three reasons, higher voltage can be generated using the device of a lower rating, increased number of voltage level produce better voltage waveform, and switching frequency can be reduced for the PWM operation. Figure 1 shows a 3-level npc multilevel inverter.

NPC multilevel inverters, in essence, synthesize a small step of staircase output voltage from several levels of DC capacitor voltages. An m-level NPC inverter is made of (m-1) DC bus capacitors, 2(m-1) switching devices per phase, and 2(m-2) clamping diodes per phase. Figure 1 depicts the structure of a three-level NPC. The DC bus voltage is divided into three levels by the use of two DC capacitors, C1 and C2. Each capacitor has a voltage of Vdc/2 volts, and each voltage stress is limited to one capacitor level by clamping diodes (Chaturvedi et. al., 2005; Lai and Peng, 1996) [14][15]. Table 1 shows the three states of the output voltage, V_{AN}.

Additional switching devices can increase the number of levels, and with these additions, the inverter will be able to achieve higher AC voltage, producing more voltage steps that approach sinusoidal with minimal harmonics distortion. During inverter operation, the switches near the centre tap are switched on for a longer period than the switches further away from the centre tap, as shown in Table 1. Switching time decreases as the switch is moved away from the centre tap. The clamping diode is another distinction between traditional 2-level and multilevel NPC. Clamping diodes, D1 and D4, clamped the DC bus voltage into three voltage levels, +Vdc/2, 0, and -Vdc/2, in the case of a three-level NPC inverter using Space Vector Modulation.

Diode, D4 balance between power separation between S4in and S4out, with S4in blocking voltage across C1 and S4out blocking voltage across C2.

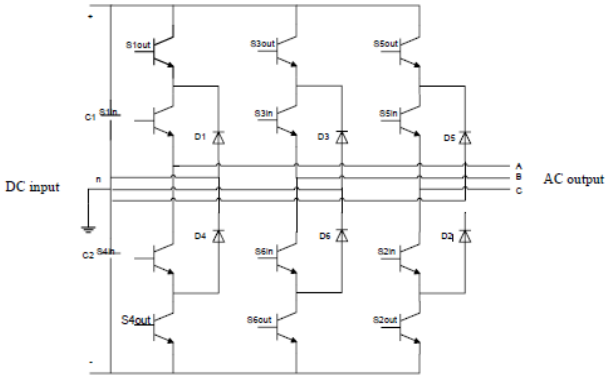

Figure 1: 3-Level Neutral-Point-Clamped Inverter

Table 1: 3-level NPC inverter output voltage levels and their switching states for phase A

Voltage Level, V_{AN}	Switches Functioning
-Vdc/2	S4in, S4out
0	S1out, S4in
+Vdc/2	S1in, S1out

The NPC Inverter offers the following advantages (Rashid, 2001; Lai and Peng, 2016) [15][16].

- With a high level of m, the degree of harmonics content distortion is so low that no filter is required.
- The active flow of energy can be controlled.
- The efficiency is high because all devices are switched to the default frequency.
- The control system is simple in the internal back and forth system.

While the drawbacks are (Rashid, 2001) [16].

- The number of reinforcing diodes increases exponentially with increasing volume.
- It becomes increasingly difficult to control the power flow of the converter.

3. SPACE VECTOR MODULATION

SVM (space vector modulation) is a pulse width modulation (PWM) control algorithm. It is used to generate alternating current (AC) waveforms, which are then used to power three-phase AC motors at varying speeds from DC.

However, multilevel topologies require a large number of switching devices which makes it more complex their modulation schemes. Three steps are involved in the implementation of an SVM 1) Identifying the triangle in which the reference vector's tip point is located. 2) Duty cycle calculation for each triangle. 3) Identifying switching states under the desired switching sequence. [17].

A reference signal V_{ref} is sampled with a frequency fs to implement space vector modulation (Ts = 1/fs). Using the abg transform, the reference signal can be generated from three separate phase references. The reference vector is then created by combining two adjacent active switching vectors and one or both zero vectors. There are several strategies for determining the order of the vectors and which zero vector(s) to use. The harmonic content and switching losses will be affected by the strategy chosen.

Space Vector Modulation is a technique in which the reference voltage is represented as a reference vector that the power converter generates (Franquelo et. al, 2008) [18]. Each inverter leg has three switching states for the operation of a three-level inverter: [P], [O], and [N]. [P] indicates that the upper two switches in leg A are turned on and that the inverter terminal voltage, VAN, is +Vdc/2, whereas [N] indicates that the lower two switches are turned on and that the terminal voltage is -Vdc/2. The switching state [O] indicates that the inner two switches are turned on and the terminal voltage is equal to zero. The NPC inverter has a total of 27 switching state combinations [19].

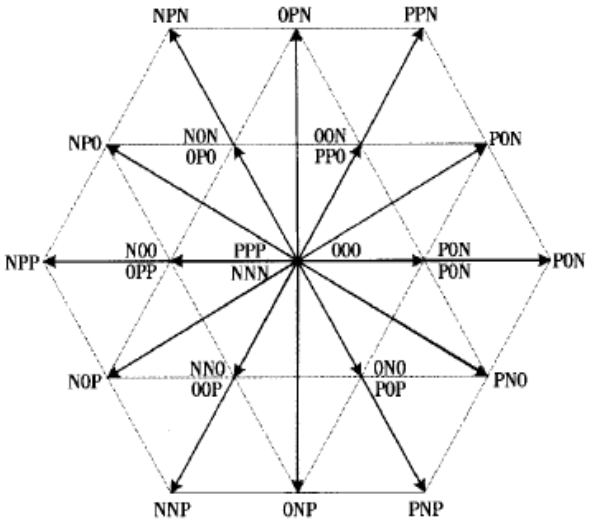

Figure 2: All possible combination of svm for 3-level inverter.

Few advantages of SVM technique are:

- Because the harmonic content of the output is reduced, this vector modulation method produces an optimal output current or voltage.
- It gives us the advantage of producing fewer harmonics in Vt by utilizing the voltage or peak of voltage Va.

Few disadvantages also exist:

- It incurs switching losses because it performs switching.
- One disadvantage is the reduction in volume.

4. MATLAB/SIMULINK SIMULATION MODEL

As shown in Figure 3, the three-phase, three-level NPC multilevel inverter is made up of twelve IGBTs and six reinforcing diodes. The reinforcing diodes are wired in such a way that they block the voltage's return voltage. - capacitor. Two capacitors can be used to divide the DC link voltage into three power levels, namely + Vdc, 0V, and Vdc, hence the name 3-level.

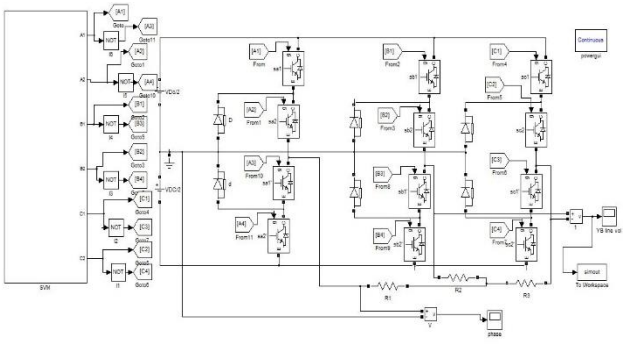

Figure 3: Simulation model of 3-level npc inverter

The 3-level NPC inverter requires twelve signals for this function. These signals must be calibrated to the alternating current supply voltage. Because MATLAB / Simulink lacks such a block-set, a new block is designed

and upgraded using the Simulink Toolbox's block set. The IGBTs' gate signal sequence and operating angle are also determined. Figure 4 depicts a sophisticated simulation model of a space vector algorithm subsystem.

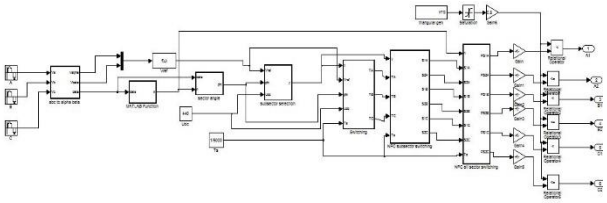

Figure 4: Simulation model of space vector modulation algorithm

Table 2: Used Components

S. No.	Component Used	Value	Quantity
1	Diode	0.001 ohm each	6
2	IGBT	1e-3 each	12
3	Voltage Source	230V	2
4	Power gui	N/A	N/A
5	Solver- ode45	N/A	N/A

5. RESULT AND DISCUSSION

To assess the efficacy of the proposed SVM method, numerical simulations were run in the MATLAB/Simulink environment. The alternating current voltage sources are set to 230V, and the switching frequency is 314 Hz. Figure 5 shows the modulated line-to-neutral output voltage obtained, while Figure 6 shows the line-to-line output voltage obtained with three-level topologies during steady-state operation. The desired output frequency is 50 Hz. As can be seen, the proposed method works well for 3-level inverters, and the voltage waveform approaches a sinusoidal shape as the inverter level increases. As can be seen, aside from the fundamental component, there are no low-order harmonic components, allowing for smaller output filters. Furthermore, as the inverter level increases, the THD decreases significantly.

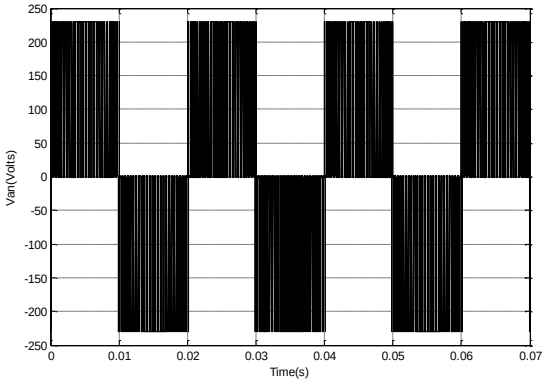

Figure 5: Simulated line-to-neutral voltage of 3-level npc inverter

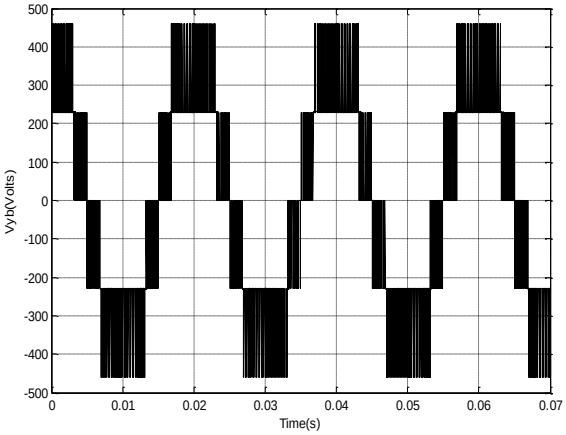

Figure 6: Simulated line-to-line voltage of 3-level npc inverter

THD values for those three parameters, line-to-line voltage, VLL, line-to-neutral voltage, VLN, and current line IL without using any filter are made, calculated, and placed in Table 3 of the simulation model.

Table 3: Simulation results of line-to-line voltage, line-to-neutral voltage, and line current THDs

Simulation of 3-level NPC inverter			
THD (%)	V_{LL}	V_{LN}	I_L
	13.36	29.44	29.44

The simulation model's results were then compared to several types of multilevel inverters with various control strategies investigated by other. Table 4 summarizes the comparison. Table 4 demonstrates that the proposed SVM 3-level NPC inverter outperforms the competition.

Table 4: Comparison of the proposed inverter model with another researcher's inverter model

Parameter of THD value	Proposed SVM 3-level NPC inverter	SWPM 3-level [Panagis *et. al.*, 2008]	PWM 3-level NPC [Zambra *et. al.*, 2008]	SVM 3-level NPC [Chaturvedi, Jain and Agrawal, 2005]
Line-to-line Voltage, V_{LL} (%)	13.36	56.47	N/A	16.46
Line-to-neutral Voltage, V_{LN} (%)	29.44	N/A	39.2	N/A
Line current, I_L (%)	29.44	N/A	N/A	N/A

6. CONCLUSION

The low-content harmonics content of the 3-level filter inverter simulation model is successfully designed and enhanced. The results obtained from the simulation model are visible. The THD voltage values of the proposed inverter are lower than those of the same inverter using different techniques. The Effectiveness of the proposed SVM method has been verified during

steady-state and transient operation of a 3-level inverter. This method can also be extended to any number of levels. It can be observed the multi-level inverter offered low harmonics and high efficiency which is suitable for high voltage and high-power applications. The results mentioned above show that the proposed optimized SVM algorithm with the reduced switching number in elementary cycle patterns makes it possible to reduce the heating of switches and enhance the harmonic content of the inverter output line voltage wave.

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