FET Structures for Future Technology Nodes

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***Abstract -** The Field Effect Transistors (FET) is considered as the bedrock of modern electronics. With the growing technological advancements, it is necessary to have a replacement to silicon based devices, as they have shown significant drawbacks in lower technological nodes. The Graphene Nano Ribbon (GNR) based devices can be used as a replacement for conventional silicon based devices. The GNRFET can be scaled down to low nanometer ranges. The benefits of FET geometries can also be used to scale down the device. In this work, device scaling is done for the GNRFE and different geometries are compared. Also the geometrical benefit of back gate geometry is utilized to aggressively scale the structure to sub-3 nm technology node.*

***Key Words*: Scaling, back-gate geometry, grapheme Nano ribbon, GNRFET, VLSI, nanotechnology, CGP.**

1. INTRODUCTION

The world is being advanced every day. New technologies and ideas are being invented and numerous researches are going on. The electronics field is always being equipped with new changes. Each new invention is changing the face of world and electronics. One main field of interest in electronics is the scaling of devices. The sizes of devices have reached up to very lower dimensions, and are expected to be smaller in the coming era. With the basic device being scaled, the electronics equipment's are being reduced in size and are easy to be handled by the end users. The scaling is done accordingly to Moore's law and now the progress in silicon technology continues to outpace the historic pace of Moore's Law, but the end of device scaling now seem to be only a few years away [1]. As scaling beyond today's state-of-the-art sub-10 nm technology nodes becomes increasingly challenging, it remains unclear how transistors will scale to future sub-3 nm technology nodes [1],[-2]. Even if CGP is scales to a large extend, the required shrinking of the physical spacing between the gate and the source/drain of the FET result in increased parasitic capacitance, degrading potential energy-delay product (EDP) benefits [3],[4]. The scaling of device can also give rise to increased short channel effects (SCE) in FETs and can eventually cause degradation of performance and efficiency of FETs.

Because of these reasons, it is necessary to search for beyond-silicon emerging nanotechnologies to supplement silicon CMOS. Therefore, it is of intense interest to find new molecular-scale devices that might complement basic silicon platform by providing it with new capabilities - or that might even replace existing silicon technology and allow device scaling to continue to the atomic scale. The allotropes of carbon make a good substitute to be used instead of silicon. It is found that digital VLSI circuits fabricated from GNRFETs can achieve better properties vs. silicon CMOS [3]. GNRFET in all geometries shows better properties when compared to silicon FETs. The structures shows lower internal parasitic capacitance along with lower affection of short channel effects (SCEs).

The designing of FET have reached much different geometry including double-gate, tri-gate, gate-all-around etc. These structures were designed to obtain better properties and functionality and also to withstand scaling. The firstly designed back-gate FET geometries actually provide major advantages that have not been exploited for highly scaled technologies: (1) back-gate FETs enable physical scaling beyond the limits of both top-gate and gate-all-around FET geometries, and (2) back-gate FETs simultaneously provide significant reduction in parasitic capacitances compared to top-gate and other geometries[1]. These advantages can be used to design a back-gate FET, which belongs in the lower nanometre dimension. This work includes designing of different geometries of back gate GNRFET at lower nanometre dimensions. A back-gate FET, with 30-nm CGP, that falls to 3-nm node is designed. A comparison of both GNRFETs is done to know the advantages.

2. GRAPHENE NANO RIBBON (GNR)

Graphene nano ribbons (GNR) are strips of graphene fabricated as sheets at lower nanometer dimensions, with a width less than 100 nm and thickness of 1 – 2 nm. GNR sheets consist of a single layer of atoms making it a monolayer structure. The atoms form a dense honeycomb two-dimensional lattice crystal structure. GNR possess all properties of graphene including good mechanical, thermal and optical properties, high selectivity and sensitivity, optical transparency, good flexibility and elasticity highest ballistic and electron speed and also possess tensile strength ten times that of steel, making it ideal for use in electronic applications when compared to other traditional materials. The most prevalent and significant property being its electrical conductivity. The graphene can be arranged in any geometry according to the application and need. It can be wrapped up into 0-D fullerenes, folded into 1-D nanotubes or stacked into 3-D graphite. GNR is considered one of the most promising models for future nano electronics.

2.1 SCALING

The structural properties of GNRs depend on the structure of the ribbon sheets. The properties depend mainly on how the molecules or ions are arranged in the sheet. The electronic structure of GNR is not the same as those of 2D graphene and depends on the edge states. According to this edge state, the sheets will have different edge properties. The edge structures include armchair or zigzag, which have different properties. So the edge structure can be designed to alter the electronic properties of GNR. GNR and CNT possess similar properties as both are allotropes of carbon. But when comparing both the results shows that GNR can be a promising alternative to CNTs. The GNRs help to overcome the chirality challenges of CNT as a nano scale device. The conductivity is also determined by the edge state. GNRs with predominantly armchair edges are observed to be semiconducting, while GNRs with predominantly zigzag edges demonstrate metallic properties.

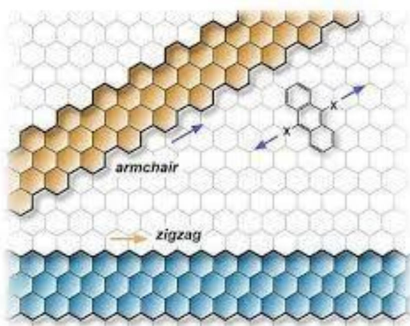

Fig -1: Graphene Nano Ribbon structure showing arm-chair and zigzag edge structures.

3. GRAPHENE NANO RIBBON FIELD EFFECT TRANSISTOR (GNRFET)

The Graphene nano ribbon field effect transistor (GNRFET) is a modified version of FET, where the channel region will be replaced with graphene nano ribbon. GNRFET is a three-terminal device, composed of a source, drain, and a top or back gate. Unlike a silicon-based transistor, the GFET has a thin graphene channel between the source and drain metal electrodes. Similar to silicon FETs, the gate in a GNRFET controls the flow of electrons or holes across its channel. Since the transistor channel is just one atom thick, all the current flows on its surface, hence providing high sensitivity. GNRFET does not face any alignment and transfer-related issues experienced by other devices.

Different geometries of GNRFET including, back-gate, top-gate, double-gate and tri-gate FETs are designed using TCAD Silvaco software. The models are compared based on their affinity to short channel effects (SCE) including drain induced barrier lowering (DIBL), sub-threshold slope (SS), threshold voltage, current values and ration, leakage current and internal capacitance.

3.1 BACK GATE GNRFET

Back gate graphene nano ribbon FET is a transistor with structure similar to conventional FET, with its gate on the back side and GNR channel. Back gate FETs enable physical scaling beyond the limit of other geometries and it also has less capacitance. These benefits can be used to design a lower dimension back gate GNRFET that can be used in the coming technology nodes.

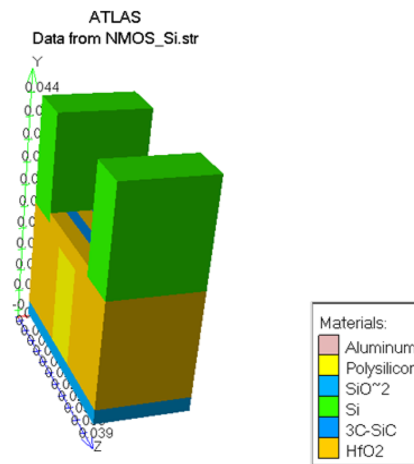

Fig -2: Structure of Back gate GNRFET and the materials used.

As the gate region is occupied in the back side of the FET, the interaction between source and drain with gate will be less, thus reducing the capacitance between them without compromise in functionality.

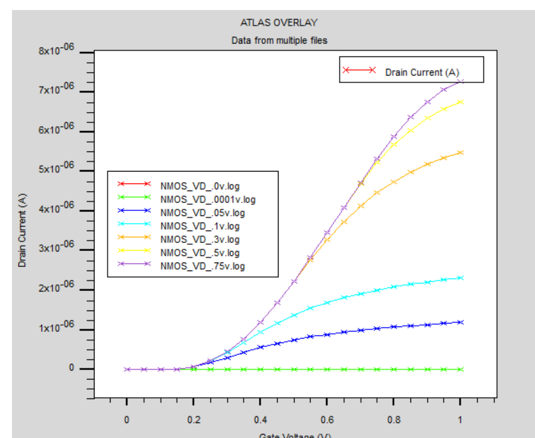

Fig -3: $I_D - V_{GS}$ characteristics of back gate GNRFET.

3.2 BACK GATE GRAPHENE NANO RIBBON FET WITH NEGATIVE L_{SP}

The geometry of back-gate FET can be utilized to design a FET scaled to the lower dimensions. Back-gate geometry enables physical scaling beyond the limits, when compared to other prominent FET geometries used. It allows the contacted gate pitch (CGP) of the structure to be reduced to much lower nanometer ranges. The CGP reduction can be made without much adverse affection in the structure or functionality. Back-gate FETs enable further reduced CGP, enabling more highly- scaled technology nodes. CGP is equal to the gate pitch between two FETs connected in series with a shared source/drain contact. It is equal to the sum of the source/drain contact length (L_C), the physical gate length (L_G), and the two spacer regions ($2L_{SP}$) that separate the gate from the source/drain

$$CGP = L_C + L_G + 2L_{SP}. \quad (1)$$

The scaled down structure can be obtained by adjusting the structural geometry of FET. The back gate FET with 30nm CGP can be obtained by arranging the FET structure in such a way that it does not have spacer regions. For back-gate FETs, the spacer regions are not necessary to avoid unintended electrical contact between the gate and the source and drain, since the back-gate is on a physically separate plane beneath the source and drain. Therefore, there can be intentional overlap between the gate with the source and drain (which mathematically corresponds to $L_{SP} < 0$). Thus, CGP can be reduced by decreasing L_{SP} even without improving fabrication techniques for scaling L_C and L_G.

The corresponding parameters selected for the back gate FET with 30 nm CGP is channel length, LC = 20nm, height of channel, HC = 2nm, gate length, L_G = 18nm, height of gate, H_G = 8nm, spacer region, L_{SP} = 4nm.

$$CGP = 20 + 18 – (2*4)$$
$$CGP = 38 – 8$$
$$CGP = 30nm$$

The physical channel length becomes

$$L_{CH} = CGP – L_C \quad (2)$$
$$L_{CH} = 30 – 20 = 10nm$$

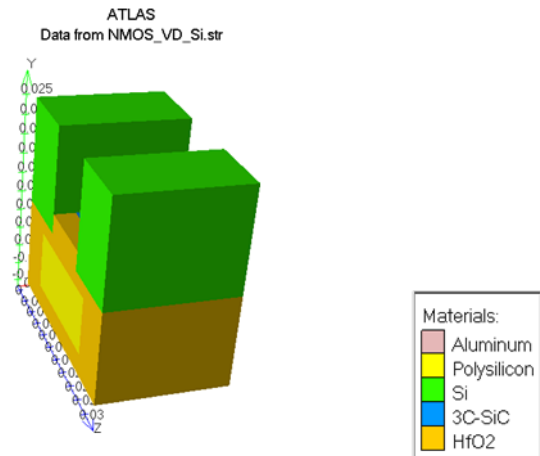

Fig -4: Structure of GNR-Back-Gate FET with 30 nm CGP and negative L_{SP} and the materials used.

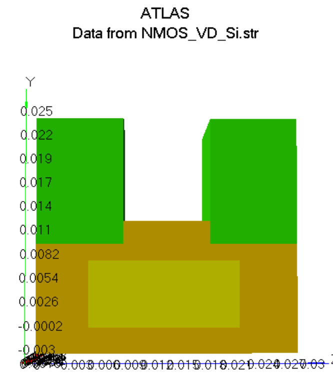

Fig -5: Side view of GNR-Back-Gate FET with 30 nm CGP and negative L_{SP}showing overlapping gate and source and drain.

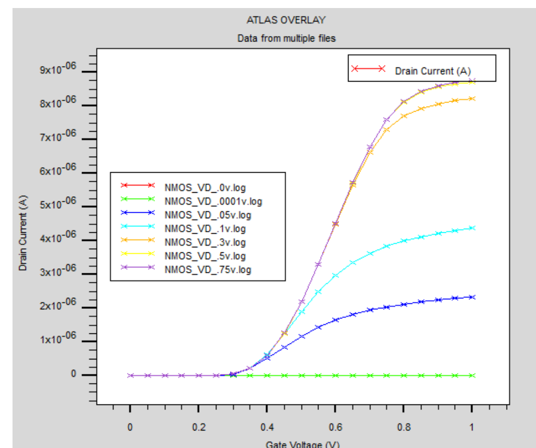

Fig -6: $I_D – V_{GS}$ characteristics of back gate GNRFET with negative L_{SP}.

The structure is designed in to be used in lower 3-nm technology nodes. The structure is occupied with a channel length of 10nm only, overall making a CGP of 30 nm by adjusting the structure in order by removing the spacer regions.

4. OBSERVATION

The back gate GNRFET was designed and the geometrical benefit of the back gate is utilized to design a back gate GNRFET with 30 nm CGP that can be used in the lower 3-nm technological nodes. TCAS Silvaco tool is used for the designing of structures. Table -1 show the corresponding results obtained from the structures. For both the structures, drain induced barrier lowering (DIBL), sub-threshold slope (SS), on-current (I_{ON}), off-current (I_{OFF}), ration, leakage current and parasitic capacitance is obtained.

Table -1: GNRFET parameter values obtained.

PARAMETERS	BACK GATE GNRFET	BACK GATE GNR FET WITH NEGATIVE L_{SP}
V_T AT V_D=0.75V	V_T = 0.218V.	V_T = 0.324 V
DIBL	11.39 mVV^{-1}	33.7 mVV^{-1}
SS	59.04 mV/dec	62.074 mV/dec
I_{ON}	5.324 $*10^{-6}$ A	7.601 $*10^{-6}$ A
I_{OFF}	3.955$*10^{-11}$ A	3.413$*10^{-12}$ A
I_{ON}/I_{OFF}	13.4588 $*10^4$	22.26 $* 10^5$
LEAKAGE CURRENT	7.269 $* 10^{-06}$ A	8.750 $* 10^{-6}$ A
Gate- to-Source Capacitance, C_{GS}	1.885$* 10^{-18}$ F	1.66 $* 10^{-18}$ F
Gate-to-Drain Capacitance, C_{GD}	8.495$*10^{-18}$ F	1.125 $*10^{-18}$ F
Gate-to-Body Capacitance, C_{GB}	5.532 $*10^{-18}$ F	3.324 $*10^{-18}$ F

Both the GNRFETs give better result, close to the ideal value needed. The result shows that even though the back gate GNRFET is designed at lower dimensions, it shows close results to the conventional back gate GNRFET. Both the structures have low threshold value and low DIBL. the lower nm back-gate FET also show lower DIBL, even at 10 nm channel length. For both structures SS is close to ideal value. Better value of on-current, low value of off-current is obtained and better ratio is obtained. Both structures also give low values of parasitic capacitance. The negative LSP back gate GNRFET provide high on-current, low off-current and a high ratio of I_{ON}/I_{OFF} when compared to the back gate FET. It also provides less internal parasitic capacitance to that of the regular GNRFET.

5. CONCLUSION

The demonstration of different geometries of back gate GNRFET is done in this work. The work demonstrates a new path for realizing aggressively scaled technology nodes, enabling continued scaling to future sub-3 nm technology nodes. The structures are found to be with better properties. The back gate FET, with negative spacer region also shows better properties and advancement. The GNRFET back gate structures prove to be used in the coming future technology nodes. However, the structures are having more than expected leakage current. Methods such as reducing width or other lector techniques should be adopted to avoid this. The structures with all other property benefits prove to be a better device to be used in the coming era of electronics.

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