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# Hardware Implementation of Synchronous Forward Converter with Digital Control using FPGA

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**Abstract -** *For building high power DC-DC converter, forward converter is best suitable. Digital technology plays vital role in power electronic industry which provides novel technology to control the DC-DC converter considered in this project. Closed loop control of the forward converter is built with reprogrammable FPGA A3P250- VQ100 in this project. The MOSFET gate pulses, to drive the Main MOSFET and synchronous MOSFETs at secondary side with required delay is programmed using FPGA. Lossless Snubber is designed to reset the Transformer core. This helps to operate the converter considered with reduced voltage stress across the main MOSFET and with wide input voltage range of 18-50V. The novel technique with FPGA is verified to have the overall efficiency of the converter greater than 80% by hardware implementation the diodes at the secondary side are replaced by synchronous rectifier because of the low forward voltage drop in comparison with the diodes. The output voltage for voltage feedback is sensed through isolated magnetic feedback generator. The voltage sensed is converted to digital value by 12 bit ADC by track and hold process. The paper focuses on the design of 150W DC-Dc forward Converter by digital control along with over current protection, input side under voltage and over voltage protection.*

***Key Words***: Synchronous Rectifier, Digital Control, FPGA, ADC, Voltage Mode Control

## 1. INTRODUCTION

For space applications, the power density of SMPS is very critical as it determines the size and weight of the system. Reliability, robustness and low cost are other important factors. In recent years linear supplies based on analog control and switch mode power supplies were used in space. Digital electronics Invasion has enabled engineers to experiment on power systems for en-cashing flexible and configuration changes [1]. In the electronic systems, there are two mechanisms namely analogue and digital. Analogue controllers are used in the system where signals at every point in the system are a continuous function of time. Mainly this controller is consists of resistors, capacitor, transistors, etc. The UC1875 is an example of analogue controller, which is a pulse width modulation controller used in such application. This IC provides control by phase shifting one half bridge with other, by keeping constant frequency PWM. It has 0 to 50% duty cycle. Microcontrollers like Atmega, 8051 series, aurdino etc., was used earlier where a trade-off between speed/performance and price can be thought of. For critical applications where speed/performance is of utmost importance, FPGA is used. FPGA is a reconfigurable system that provides a way out to solve complex problems by integrating the speed of hardware with the flexibility of software to enhance system performance [2]. VHDL can be used for implementation of code of the control in digital domain. Depending on the duty cycle requirement PWM control circuits in the defined codes produce varied duty by operation of flip-flops [3]. Diode losses in forward converter are very high in high current applications. These losses occur on the secondary side. Synchronous rectification provides a method to decrease the losses associated with the diodes. This is achieved by replacing diodes with synchronous MOSFET. Flux reset during the off period can be achieved without losses by connecting lossless snubber across the primary main MOSFET. Lossless snubber also decreases the stress of voltage on the main MOSFET and increase the range of duty cycle. It also provides zero voltage switching during turn off [4]. The forward converter with synchronous rectification can be optimized with higher efficiency, by forward drop of the body diode in Synchronous rectifier. Robustness of the system can be improved by the utilization of prevention of negative current. This can further be enhanced by the capabilities of digital control. Digital control has higher flexibility and efficiency in comparison with the analog synchronous rectification method [5].

### 1.1 Designed Converter Specification

Forward topology is best suitable for designing to support the 30A output current, due to lesser, transformer size and input Peak current. The designing of the closed loop controller is easy to implement due to its simpler structure. The specifications of the converter proposed are as follows,

| | |
|---|---|
| Input voltage | : 18V – 50V |
| Nominal input voltage | : 28V |
| Output voltage | : 5V |
| Output ripple voltage | : ± 50mV |
| Output current | : 0A – 30A |
| Switching frequency | : 122 kHz |
| Efficiency | : greater than 80% at 30A |

Protection : Over current protection

Under input voltage protection

Over input voltage protection

### 1.2 Block Diagram

The block diagram of the converter is shown in Fig-1. The raw bus voltage which varies between 18V to 50V is connected to the primary winding through EMI filter. There are three secondary windings one is used to build the 5V output voltage, second to power the FPGA and third to power the secondary MOSFET driver.

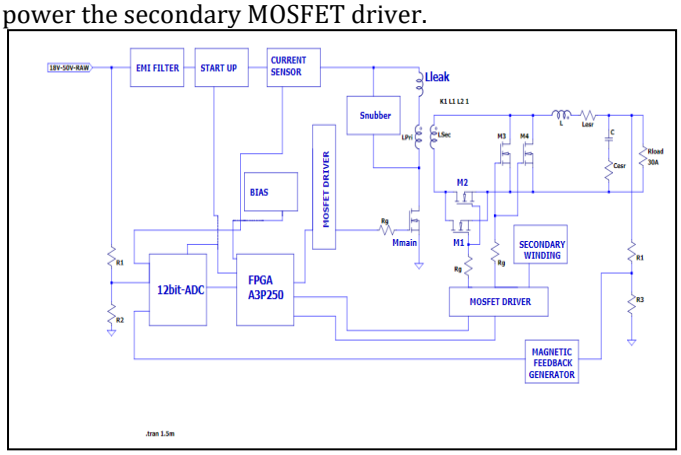


**Fig -1**: Block Diagram of Proposed Converter

The converter is turned ON by applying 60ms pulse to the start-up circuit. This circuit generate the 12V for 60ms and this voltage helps to power the Quad power regulator. The FPGA generates the gate pulses within 60ms and switch the main MOSFET and develop the voltage at the bias winding and continue to power the FPGA. The FPGA varies the duty cycle, based on digital data from the ADC ADC128S102. The ADC sense this output voltage by using the isolated feedback generator i.e UC1901 through voltage divider. The PWM pulses from the FPGA are applied to the MOSFET driver UCC21222 to drive the MOSFET. UCC21222 is isolated MOSFET driver which helps to drive the synchronous rectifiers. The ADC sense the input voltage through the resistor divider circuit and input current through current transformer and converts this analog data into digital data and sends to FPGA. The FPGA has reference values with which the sensed data from the ADC is compared. If the value exceeds the reference value the FPGA stops the gate pulses and converter turned off. The converter also can be turned off by applying the turn off command. FPGA sense this command and stop the generation of the pulses.

### 1.3 Voltage Mode Control

Voltage mode control is basic control method shown in Fig-2, in which feedback loop senses the output voltage. The output voltage with the reference voltage is compared by Error amplifier and differential error voltage is generated. PWM generator compares the differential voltage with the ramp wave, due to which pulses are generated. The PWM signal pulse width is varied for control of output voltage to the required value for input Voltage variations.

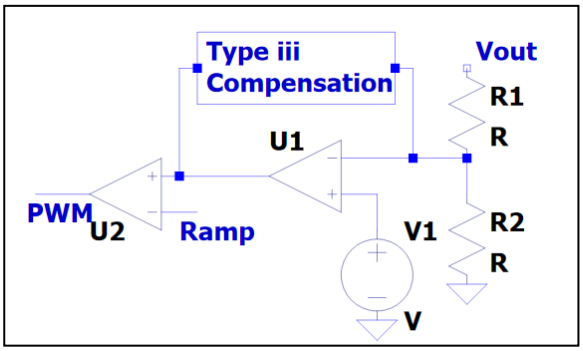


**Fig -2**: Voltage Mode Control

### 1.4 Lossless Snubber

The lossless snubber circuit is connected to the circuit as shown in the Fig-3. During OFF time the magnetizing energy and the leakage energy stored charges the capacitor C2 through D3 . After charging, this energy is discharged to the source by resonating with the time period of LC circuit caused by Lm magnetizing inductance and snubber capacitor C2. So, the stored leakage and magnetizing energy is fed to the source without any power dissipation during turn off period. Finally, when Vds of MOSFET is clamped to Vin voltage across C2 will be at Vin voltage.

Once main switch is on the the voltage across C2 resonates through the inductor of snubber circuit L3 and becomes – Vin. With negative voltage of -Vin across C2 will cause the the zero turn off switching in the, MOSFET. The recycle of magnetizing energy followed by snubber protection for the primary MOSFET is achieved by using lossless snubber. The design of snubber is taken care for the proper recycle of magnetizing energy within that cycle. The time constant of L3 and C2 is chosen precisely to achieve.

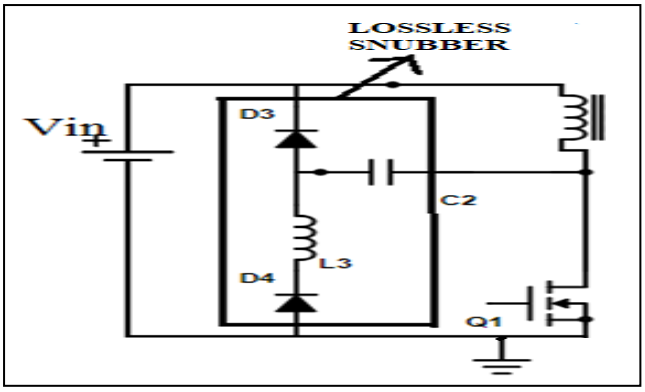


**Fig -3**: Lossless Snubber

## 2. METHODOLOGY

In Synchronous forward converter voltage mode control technique is implemented by using FPGA. The FPGA has Programmable logic units, which can be connected together to achieve regulation of the output voltage with the closed loop control to 5V against input voltage variation between 18V to 50V and output load between 0A to 30A. The FPGA has inbuilt Digital PID controller, Digital ramp and Comparator. The Digital PID controller is equivalent to the Type-iii compensation circuit. All these units are programmed to the FPGA using VHDL coding. The FPGA receives the information through the Analog to Digital Converter. FPGA has 80MHz clock as a reference clock. It provides timing reference to the basic blocks inside the FPGA. Mainly generates the gate pulses to the Main MOSFET and Secondary side MOSFET of synchronous rectifier. The timing diagram are as shown in Fig-4. The timing diagram indicates that the Main MOSFET and M1, M2 MOSFETs turn on simultaneously and M3 and M4 are complementary to the Main MOSFET with 100ns delay.

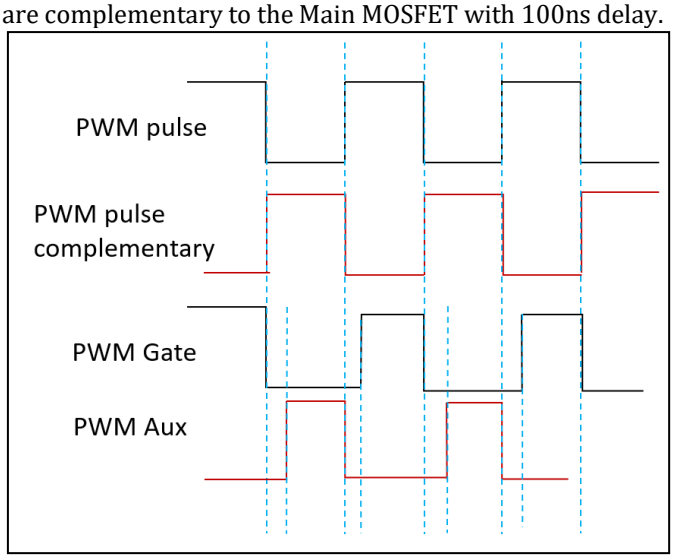


**Fig - 4**: PWM pulse timing Diagram

### 2.1 Analog to Digital Conversion

The ADC128S102 texas made ADC is used to convert the analog signals to the digital signals as shown in Fig-5. It indicates the analog voltage in 12bit binary number. It can sense the eight analog signals through eight channel. The feedback signal is sensed through channel 0 of the ADC. Channel 1 and 2 sense the under voltage/ Over voltage and primary current respectively. FPGA enable the ADC by making CS bar 0 and disable by making CS bar to high. SCLK is the reference clock given by FPGA to the ADC. The sample rate of the ADC is depending on this clock. The 16 clock cycles are required for the single sample. In first 4 falling edges the ADC is in track and hold mode and from 5th falling edge it gives out 12 bit data with MSB first. The address of the next sensing channel is feed in to the ADC's register by FPGA through Din pin from first 8 clock cycles. The three channels are allocated to sense the feedback signal, input raw voltage and Input current. This data is taken by the FPGA to compare it with the digital ramp generated.

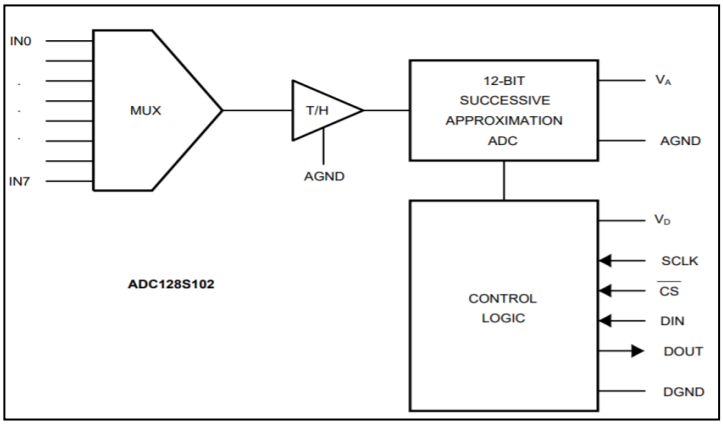


**Fig -5**: Analog to Digital Converter

### 2.2 Digital PWM Generation

The Command signal from the Digital PID controller of FPGA is compared with the counter. The program is written in such a way that PWM gate pulse is high until the counter value is less than command signal value and low when the value is higher than the command signal. As the commanding signal value changes the duty cycle of the gate pulse changes. The duty cycle is adjusted to achieve the required output voltage.

## 3. DESIGN OF CONVERTER

The preliminary calculation of duty cycle range and the expected input current drawn by the converter is calculated by assuming maximum duty and minimum obtainable efficiency respectively. The minimum duty cycle is calculated by using output voltage gain equation as below:

| | | |
|---|---|---|
| Minimum input Voltage | Vin_min=16 Volts | (1) |
| Maximum input Voltage | Vin_max=50 Volts | (2) |
| Switching Frequency | F_sw=122kHz | (3) |
| Switching Period | T_sw=(1/F_sw )=8.9µs | (4) |
| Maximum Duty Cycle | D_max=0.65 And η=0.88 | (5) |
| Minimum Duty Cycle | D_min=0.208 | (6) |

Input Flat topped pulsed current is given by,

$I\_pft=(P\_out/((\eta.Vin\_min.D\_max ) ))=16.65$ (7)

The Average input current is given by,

$I\_avg=P\_out/(\eta.V\_min )=10.824A$ (8)

### 3.1 Output Filter Calculation

The output filter section consists of inductor in series for current smoothening and capacitor in parallel for reduction in the output ripple voltage. The inductor value is designed by assuming suitable output inductor current ripple of less than 10% and is calculated by the following equation.

Inductor (L)

$$L = \frac{V_o.(1-D_{min}).T_s}{\Delta i_L} = 11.55\mu H \quad (9)$$

The output filter capacitor is calculated by assuming suitable output voltage ripple less than 10% and is given by,

Capacitor(C)

$$C = \frac{1-D_{min}}{8.L.F_{sw}^2.\Delta V_o} = 32.48\mu F \quad (10)$$

The filter capacitors five times more than the calculated value is connected at the output side. Four number of 220uf capacitors are connected instead of one bulk capacitor which will decrease the total ESR value and reduces the maximum ripple peak to peak voltage.

### 3.2 Transformer Design

The initial design of transformer is done by calculating area product required by the magnetic core for the designed converter specification. The area product for the forward converter is given by equation

Area Product Calculation

$$A_p = \frac{\sqrt{D_{max}}.P_{out}.\left(1+\frac{1}{\eta}\right)}{K_w.B_m.F_{sw}.J.10^{-6}} = 4.557e3\ mm^4 \quad (11)$$

Where (window factor) Kw = 0.4, (current density) J = 6 Amp/mm^2, (flux density) Bm = 0.12 Tesla is assumed and (output power) Pout = 150 Watts

With the above calculated value of area product suitable ferrite core equal to or greater (60%) than the above area product is selected.

Selected pot core = 0R43019UG

The output Voltage in Forward Converter is given by

$$V_o = \left(V_{inmin} * \left(\frac{N_s}{N_p}\right) - V_d\right) * D_{max} \quad (12)$$

Thus the turns ratio of the converter considering a drop 0.55 is calculated as

$$\text{Turns Ratio} = \frac{(Vd * D_{max} + V_o)}{D_{max} * V_{min}} \quad (13)$$

Turns Ratio = 0.5

The number of primary turns is given by,

$$N_p = \frac{V_{in(min)}.D_{max}}{B_m A_c F_{sw} * e - 6} \quad (14)$$

N_p=3.163 rounded to 4 turns

N_s=turns ratio*Np

N_s=2

### 3.3 Lossless Snubber Design

Lossless Snubber is selected for recovering the leakage power loss from the MOSFET. It reduces switching OFF loss in MOSFET. Lossless snubber contains two diode, one inductor (Lsnubber) and one capacitor (Csnubber). Time constant of Lsnubber and Csnubber should be less than the minimum ON time of MOSFET.

T_(on(min))=D_min*T_s*0.5 (15)

T_(on(min))=5.2e-7

L_snubber=1.03µH C_snubber=0.1µF

## 4. HARDWARE DETAILS

The components considered for the hardware implementation are given in the Table-1, the values are considered from the design section.

**Table -1:** Parameters of Hardware Prototype

| Components with Values | | | |
|---|---|---|---|
| Filter Inductor | 11.55uH | Filter Capacitor | 220uF |
| Pri Inductance | 106uH | Sec Inductance | 26uH |
| Snubber Inductor | 1.03uH | Snubber Capacitor | 0.1uF |
| Driver IC | UCC2122 | FPGA | PRoASIC 3 A3P250-VQ100 |
| ADC | ACC128S1202 | MOSFET | IPP110N20NA, FDP047AN08A0 |

### 4.1 Experimental Set up

Fig-6 shows the test setup arrangement of the implemented converter and the equipment used are as follows:

1. DSO for capturing waveform.
2. Multi-meter for output voltage measurement.
3. Electronic load.
4. Output connector.
5. DC power supplies.

6 & 7. Multi-meter for input voltage and current measurement.

8. Converter.
9. Heat sink.

The input to the converter is given by linear regulated DC power supply. Multi-meter is connected in series between DC supply and converter input for input current measurement. Similarly, multi-meter is connected in parallel across the input terminals for voltage measurement. DSO is used to capture waveforms across different components. Programmable electronic load is connected across the output terminals to load the converter for different constant current

output conditions. Converter is mounted on the metal heat sink to dissipate heat generated from the converter.

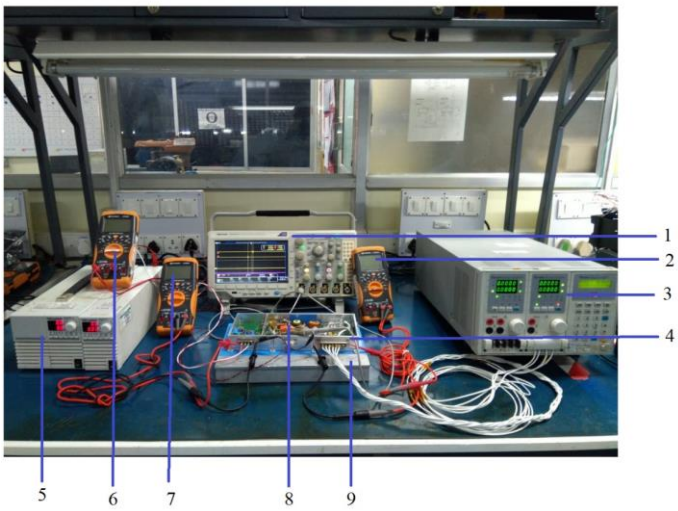


**Fig -6**: Experimental Set up of Hardware

### 4.2 Results and Waveforms

The table-2 verifies that specification of efficiency of the converter maintained greater than 80% at all line voltage variation and line regulation less than $\pm 1\%$.

**Table -2:** Efficiency Tabulation

| Vin (V) | Input power (W) | Output power (W) | Efficiency (%) | % Line Regulation |
|---|---|---|---|---|
| 18 | 171.56 | 149.73 | 87.28 | 0.02 |
| 28 | 168.11 | 149.70 | 89.05 | |
| 50 | 167.75 | 149.73 | 89.26 | |

The table-2 verifies the ripple voltage lies within 50mV for various load variations.

**Table -3:** Ripple Voltage Tabulation

| Ripple voltage ΔVpk-pk(mV) | | | |
|---|---|---|---|
| No load | 10% load | 50% load | 100% load |
| 18.40 | 16.60 | 18.40 | 18.40 |
| 26.00 | 28.40 | 27.60 | 28.00 |
| 37.60 | 38.00 | 42.80 | 47.60 |

Waveform in Fig-7, shows the drain source voltage across the main MOSFET at nominal Voltage of 28V, maximum stress of 88.75V is obtained.

**Fig -7**: Drain Source Voltage across main MOSFET

Fig – 8 shows the complimentary gate signals of forward and freewheeling MOSFET.

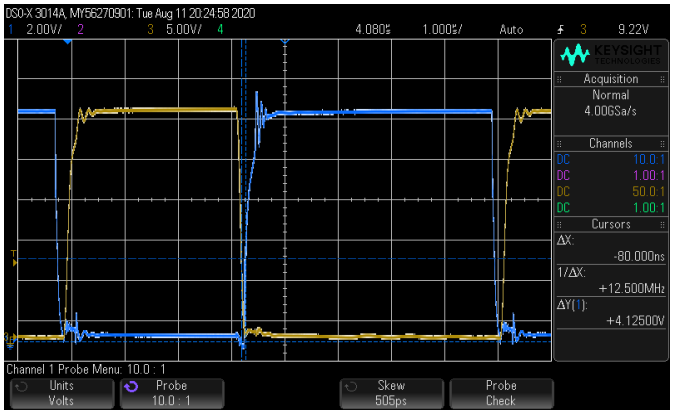

**Fig -8**: Complimentary Gate Signals

Fig- 9 Shows the output voltage waveform with overshoot of 5.1875V at input Voltage of 28V.

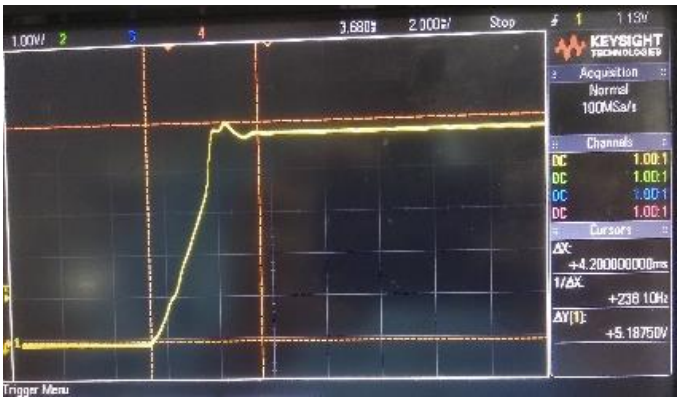

**Fig -9**: Output Voltage with overshoot

## 5. CONCLUSIONS

The synchronous forward converter with lossless snubber is designed in this project with voltage mode control by digital control using FPGA. High efficiencies greater than 80% are achieved at all load conditions with full load current being 30A. For reset of transformer and reducing the stress across the MOSFET, lossless snubber is implemented. The results are verified through drain source voltage waveforms. Hardware prototype is implemented and tested for varying

load and line conditions. From test results load and line regulation less than ±1% are verified.

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