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Low Power Carry Skip Adder Design using Full Swing GDI Technique

Akshatha K.S.[1], Dr.H.V. Manjunath[2]

[1]PG Student (M. Tech, VLSI Design and Embedded Systems), Dept of ECE, DSCE Bangalore, Karnataka
[2]Professor, Dept of ECE, DSCE, Bangalore, Karnataka

Abstract – *The main parameters in any logic circuit designs are Power consumption and chip area. The full swing gate diffusion input (FS-GDI) technique is considered to be more effective for low power digital design supporting smaller area consumption and reduced power intake in contrast to CMOS technique. It also maintains a less complex logic design and with minimum transistors many logic gates can be designed. In this project comparison is done between conventional carry skip adder and proposed full-swing gate diffusion input (FS-GDI) carry skip adder in terms of transistors count and power consumption. Schematic and implementation of project is done in cadence virtuoso at 45nm technology.*

***Key Words*: Carry Skip Adder, FS-GDI, Full Adder, Low Power, Cadence**

1.INTRODUCTION

The most widely used constituent in digital integrated circuit design is Adder, which is the basic building block in Arithmetic and Logical Unit which performs an important part in addition, subtraction and multiplication. Adders are available in various types according to the needs; which can be simple or complex architectures. The Ripple Carry Adder (RCA) has Full Adders (FA) in series. Since the carry ripples in every stage of the full adder to produce the sum, it is considered as the slowest adder. In carry skip adder (CSKA), time needed in propagating the carry will be limited by skipping over a group of consecutive stages of adder. The carry generate propagate logic is used in reduction of adder critical path delay. The CSKA will have lesser critical path delay when compared to RCA and similar power consumption and area. The CSKA will have lesser power delay product (PDP) when compared to CSLA and PPA.

Because of the huge usage of digital integrated circuit in transportable devices like smartphone, laptops and many other electronic devices, the want for reduction in power intake, small chip circuit, increase in speed are to be considered while deciding on VLSI design having good performance. The full swing gate diffusion input (FS-GDI) technique is used to achieve low power and less area in comparison to various logic patterns using only 2 transistors. FS-GDI design method has become a promising opportunity other than static CMOS logic and it can be carried out in well-known CMOS system for diverse combination circuits. The traditional GDI gates might be afflicted by threshold voltage (VTH) drops which reduce current drive impacting performance of gate and develops direct path static power dissipation. For this reason, FS-GDI technique came into existence.

2. CARRY SKIP ADDER

The carry-skip adder decreases the delay by skipping over stages of consecutive adder. The speed of this adder is similar to CLA and it consumes minimum power and area. The Uniform sized carry skip adder divides the words to be added into groups of equal size of k-bits. Carry Propagate pi signals may be used within a group of bits to accelerate the carry propagation. If all the pi signals within the group are pi=1, carry bypasses the entire group as depicted in fig. 1. The delay will be reduced when compared to ripple carry adder by following this way [1].

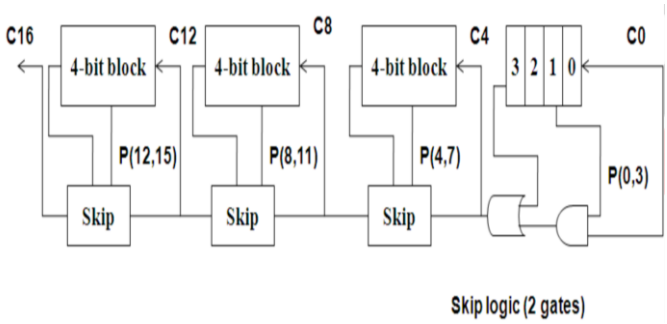

Fig-1: 16-Bit Carry Skip Adder Block Diagram

3. GATE DIFFUSION INPUT TECHNIQUE

The GDI cell is like standard CMOS inverter. The difference is that it has three inputs G, P and N as shown in fig. 2. By changing the inputs of GDI cell, complex Boolean functions are implemented using simple GDI cell [2]. The different logic functions realization using GDI is given in table 1.

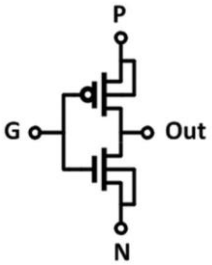

Fig-2: Original GDI cell

Table-1: Different Logic Functions Realization using GDI

N	P	G	OUT	Function
0	B	A	$\overline{A}B$	F1
B	1	A	$\overline{A}$+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\overline{A}B$+AC	MUX
0	1	A	$\overline{A}$	NOT
$\overline{B}$	B	A	$\overline{A}B$+A$\overline{B}$	XOR
B	$\overline{B}$	A	$\overline{A}$ $\overline{B}$+AB	XNOR

Power consumption and propagation delay put off are progressed. But the output voltage has non full swing because of the threshold drop. To solve this problem modified gate diffusion input (M-GDI) was proposed, where NMOS and PMOS bulks are linked with gnd and Vdd permanently, as presented in fig. 3[3].

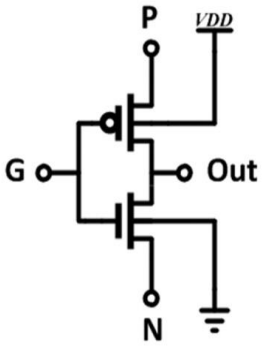

Fig-3: Modified GDI cell

The Full Swing GDI gates are introduced to enhance the output voltage swing of the circuit. To lessen the F1 and F2 gates output voltage swing, swing restoration (SR) transistor is included. These gates are just like NAND and NOR gates of CMOS as depicted in fig. 4[4].

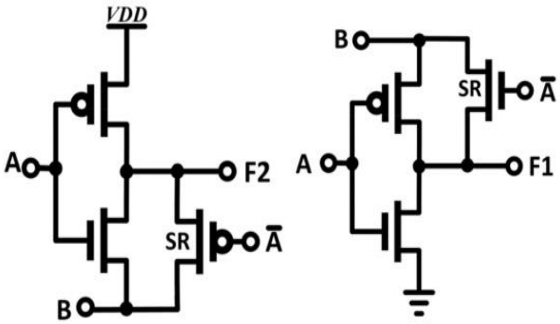

Fig-4: Full-Swing GDI gates (a) F2 (b) F1

4. DESIGN METHODOLOGY

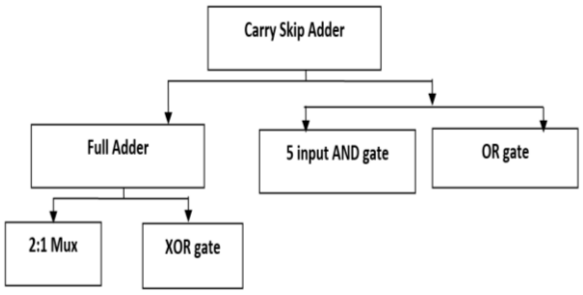

Fig-5: Hierarchy of a Carry Skip Adder

The hierarchical approach used in designing carry skip adder is depicted in fig. 5. This approach involves the concepts of regularity, modularity and locality. This approach is also called "Divide and Conquer" technique involving dividing a module into sub-modules and repeating this action till the smaller parts of the sub modules is manageable. The hierarchical approach of carry skip adder is mainly divided into full adder and skip logic. The full adder in turn consists of 2:1 mux and XOR gate. The skip logic is made up of 5 input AND gate and OR gate. So, by using the architecture in fig. 1, the concepts like regularity, modularity and locality are maintained.

5. FS-GDI 1-BIT FULL ADDER

The 1-bit full adder consists of 3 inputs and 2 outputs. A and B are the first two inputs called operands, Cin is the third input carried from the previous stage which is less significant. The Sum and Carry expressions are given by eq. 1 and eq. 2 respectively.

$$Sum = A \text{ XOR } B \text{ XOR } Cin \quad \text{eq. 1}$$

$$Cout = A \text{ (A XNOR B)} + \text{(A XOR B) } Cin \quad \text{eq. 2}$$

The FS-GDI full adder includes 18T to enforce 1-bit full adder. It includes 2 XOR gates producing sum and single mux producing Cout as depicted in fig. 6. and full adder truth table is presented in the table 2.

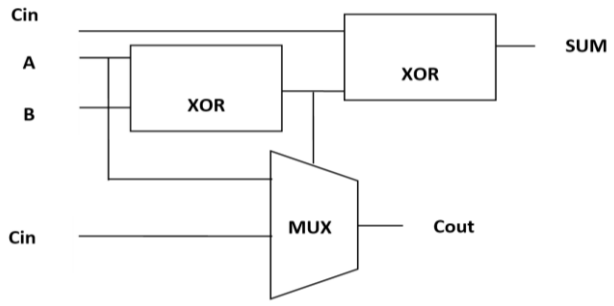

Fig-6: Full Adder Block Diagram

TABLE-2: Full Adder Truth Table

A	B	Cin	SUM	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The schematic is designed using pmos1v and nmos1v from 45nm GPDK. The pmos transistor size is twice the size of nmos transistor i.e. (W/L)p=240nm/45nm and (W/L)n=120nm/45nm. This sizing is used for all the pmos1v and nmos1v transistor. The schematic of inverter, FS-GDI XOR, FS-GDI 2:1 Mux and FS-GDI full adder is shown from fig. 7 to fig. 10 respectively.

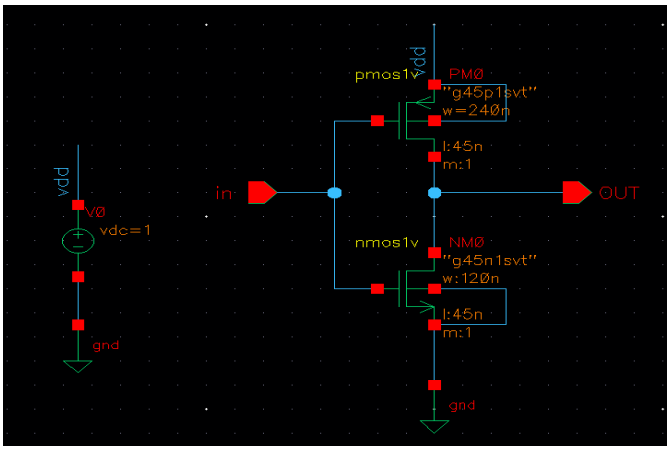

Fig-7: Schematic of Inverter

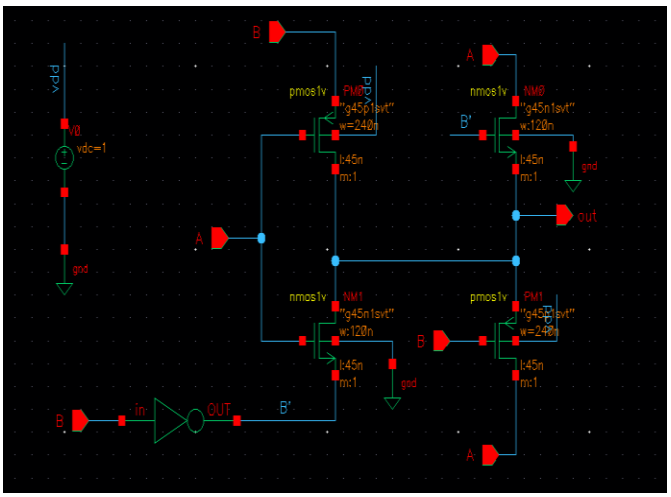

Fig-8: FS-GDI XOR Gate Schematic

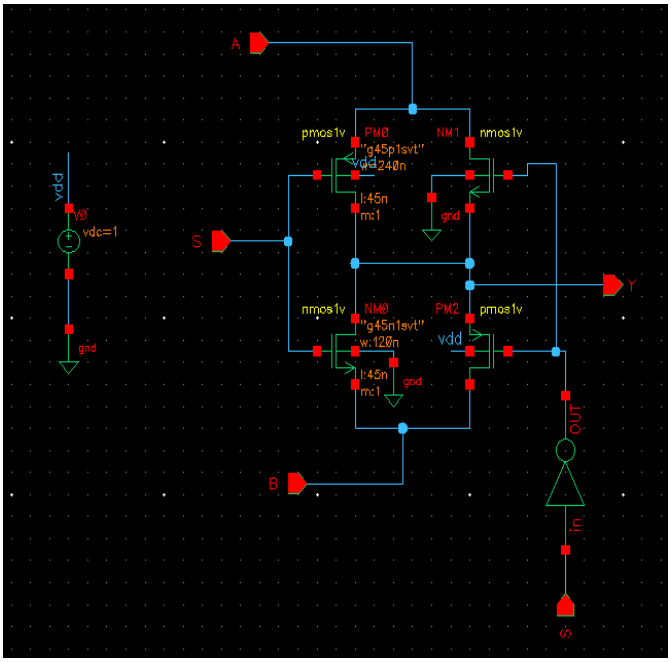

Fig-9: FS-GDI 2:1 Mux Schematic

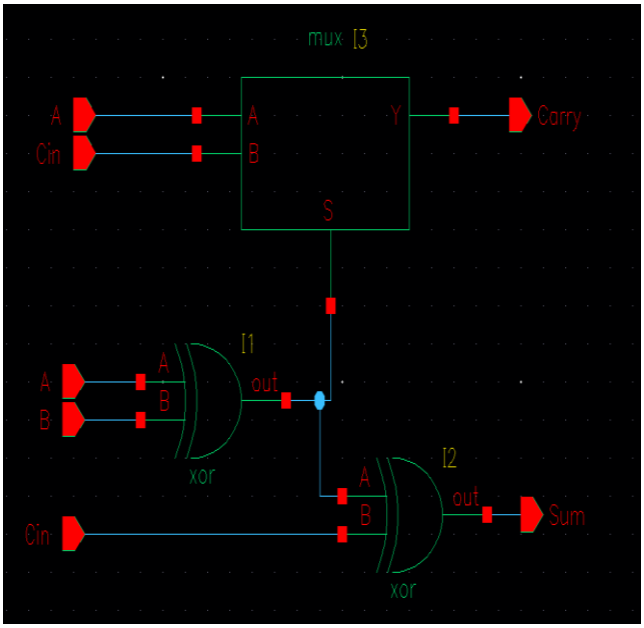

Fig-10: FS-GDI Full Adder(1-Bit) Schematic

6. SKIP LOGIC

The OR gate and AND gate together forms the Skip logic. The input configuration of AND gate is based on the bit configuration of CSKA. The 16-bit carry skip adder skip logic consists of OR gate and 5-Input AND gate as depicted in fig. 11 and fig. 12 respectively. The schematic of 16-Bit CSKA using FS-GDI Technique is depicted in fig. 13.

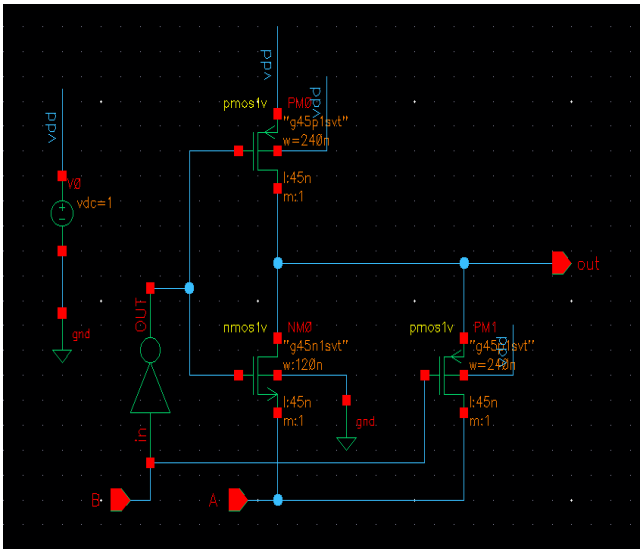

Fig-11: FS-GDI XOR Gate Schematic

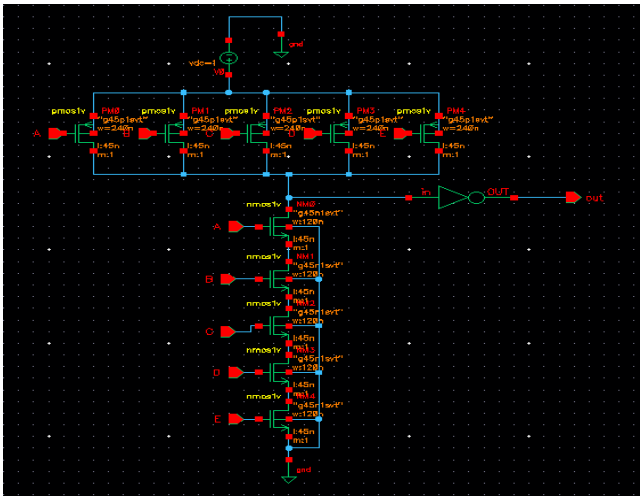

Fig-12: CMOS 5-Input AND gate Schematic

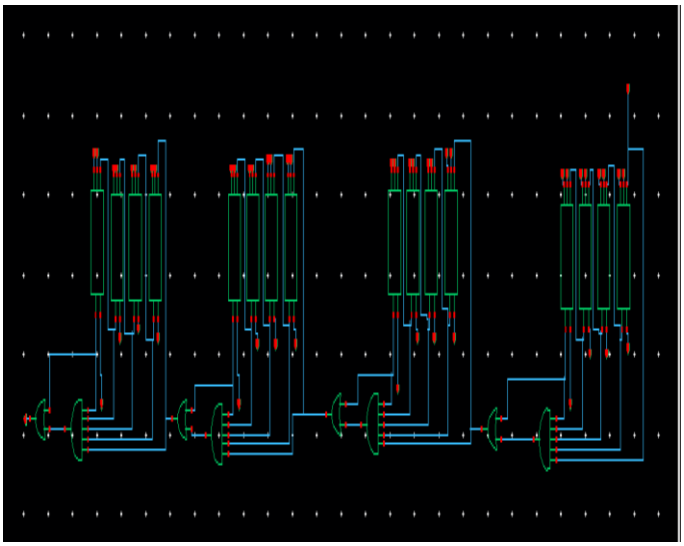

Fig-13: Schematic of 16-Bit CSKA using FS-GDI Technique

7. RESULTS AND DISCUSSION

The test circuit of 16-bit FS-GDI Carry skip adder is depicted in the fig. 14. The specifications of designed circuits in 45nm technology are given in Table 3. The transient response waveforms are shown from fig. 15 to fig. 21.

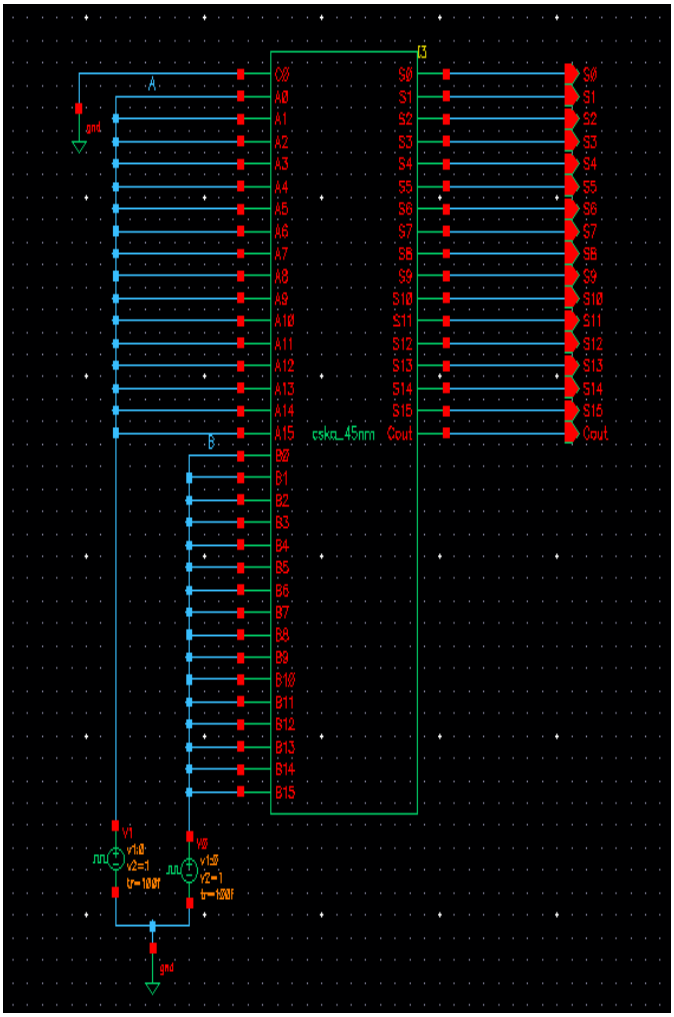

Fig-14: Test Circuit of FS-GDI 16-bit Carry Skip Adder

Table-3: Specifications of designed circuits in 45nm Technology

Specification	pmos1v	nmos1v
Library name	Gpdk 45	Gpdk 45
Length	45nm	45nm
Total width	240nm	120nm
Finger width	240nm	120nm
Rise time/Fall time	100fs/100fs	
Supply Voltage	1 V	

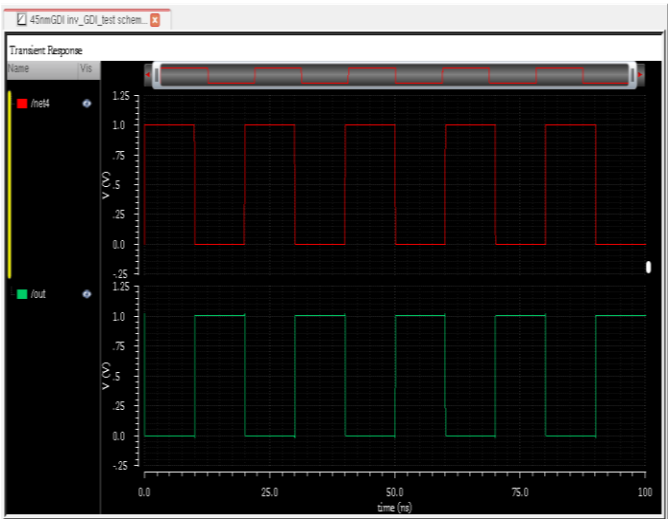

Fig-15: Transient response of Inverter

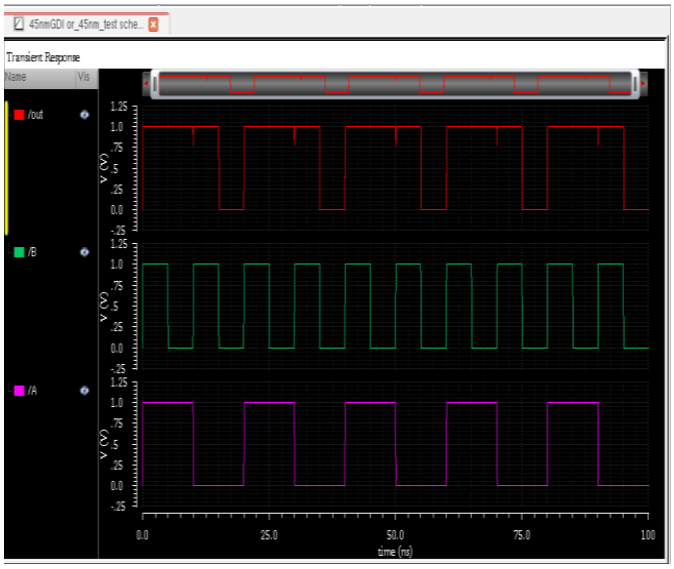

Fig-16: Transient response of FS-GDI OR gate

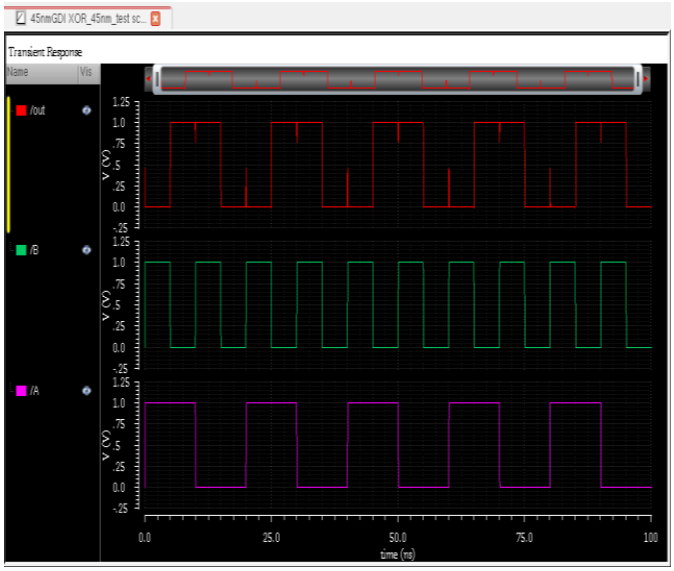

Fig-17: Transient response of FS-GDI XOR gate

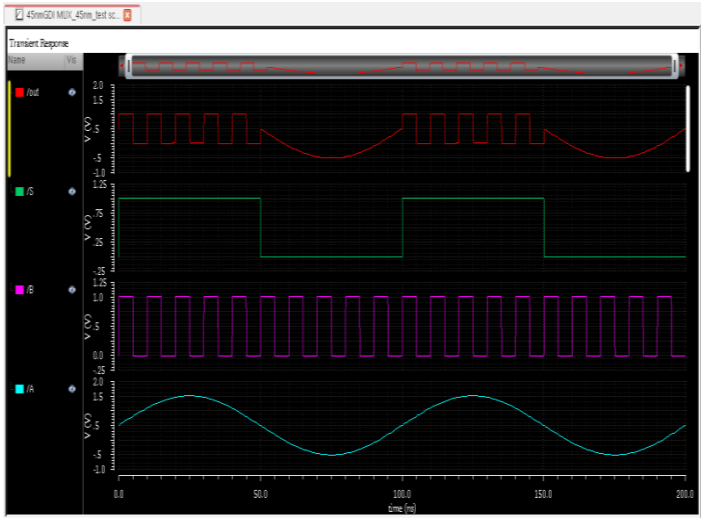

Fig-18: Transient response of FS-GDI 2:1 MUX

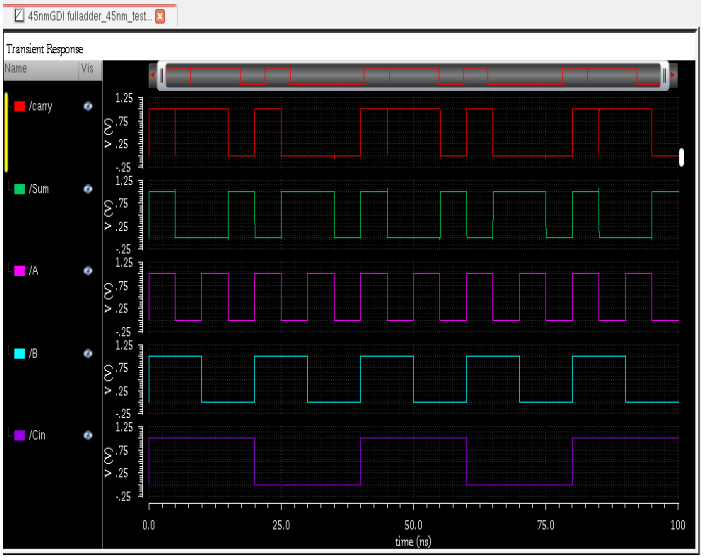

Fig-19: Transient response of FS-GDI 1- Bit Full Adder

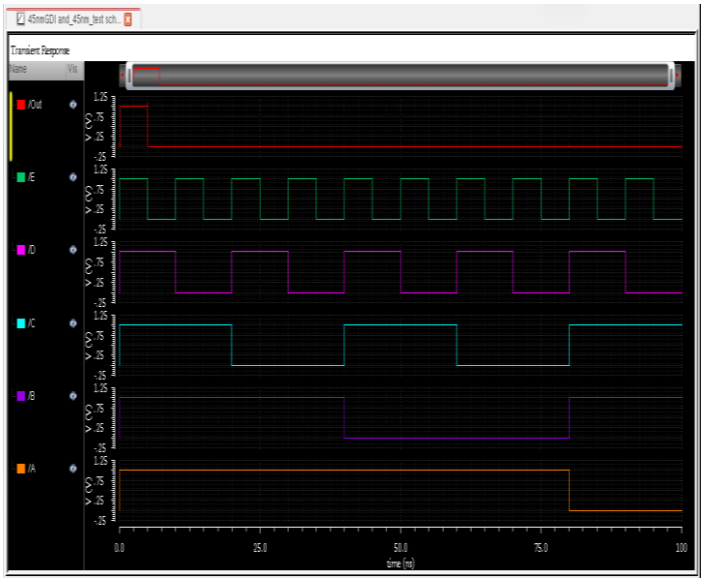

Fig-20: Transient response of CMOS 5-Input AND gate

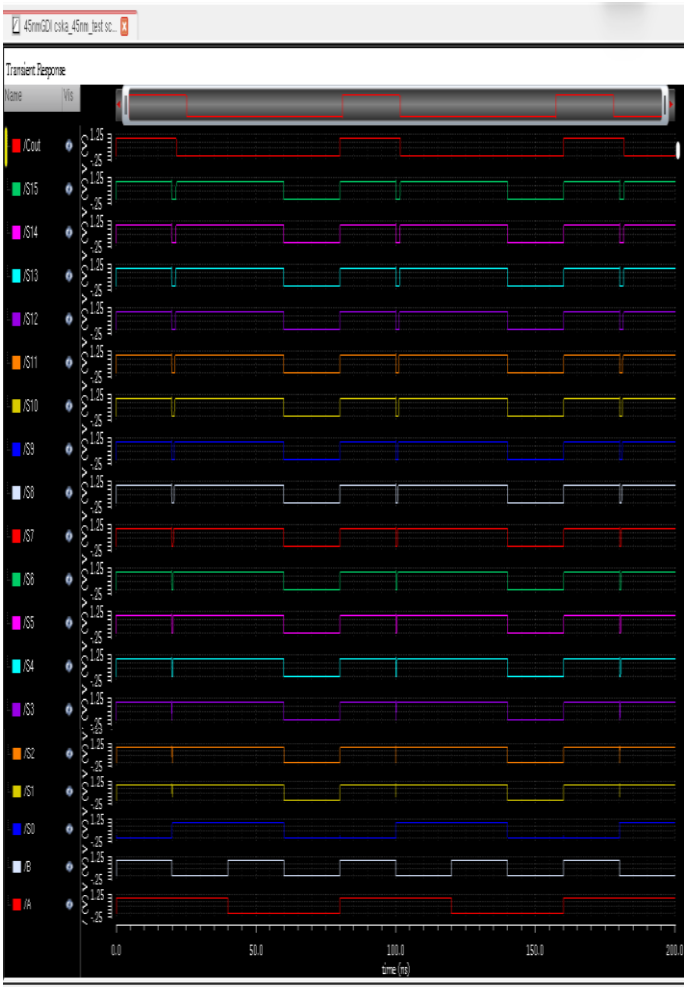

Fig-21: Transient response of FS-GDI 16-bit Carry Skip Adder

Table-4: Comparison wrt Transistor Count

	No. of Transistors	
	CMOS	FS-GDI
NOT	2	2
OR	6	5
AND	6	5
XOR	14	6
2:1Mux	12	6
1-Bit Full adder	28	18
16-Bit Carry skip adder	520	356

Table 4 gives the comparison between designed CMOS and designed FS-GDI carry skip adder transistors count. From this it can be concluded that the FS-GDI utilizes less transistors in contrast to traditional CMOS.

Table-5: Power consumption comparison of full adder(1-bit)

Design	No. of Transistors	Power (nW)	Technology
Ahmad [5] CMOS	28	351.1	45nm
D. Shindi [6] GDI-PTL	10	8100	45nm
Shoba [7] FS-GDI	18	927.9	45nm
Badry [8] FS-GDI	16	693.5	65nm
Badry [9] FS-GDI	18	4000	65nm
Proposed FS-GDI Full Adder	18	247.8	45nm

Table-6: Power consumption comparison of 16-bit carry skip adder (CSKA)

Design	Power (uW)	Technology
S. Patel 2019 [10]	15.53	65nm
Arun Sekar 2019 [11]	12.31	45nm
Aradhya 2019 [12]	8.97	45nm
Proposed FSGDI CSKA	1.55	45nm

Table 5 and Table 6 gives the power consumption comparison of full adder(1-bit) and 16-bit carry skip adder (CSKA) respectively. From these two tables, it can be seen that the full adder and CSKA implemented with FS-GDI logic consumes less power when compared to other full adder and carry skip adders in the literature.

8. CONCLUSION

This work presents 16-bit carry skip adder designed in 45nm technology using Full Swing GDI technique. The simulations are done in Cadence Virtuoso simulator and there was improvement in transistor count and power consumption by maintaining the full swing operations. From the results, it can be concluded that the proposed 16-bit FS-GDI carry skip adder is a good approach for low power VLSI applications. Future work is to design the 32-bit and 64-bit CSKA by using the designed 16-bit CSKA as a building block.

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