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HIGH-THROUGHPUT LOW-POWER AREA-EFFICIENT OUTPHASING MODULATOR BASED ON UNROLLED AND PIPELINED RADIX-2 CORDIC

Dr. Nagaraju .N[1], Abinaya .C[2], Archana .C[3], Dhivya Dharshini .J[4], Jeevana .K[5]

[1]Associate Professor, [2,3,4,5]UG Students, Department of Electronics and Communication Engineering, Adhiyamaan College of Engineering, Hosur, Tamil Nadu, India.

nnagaece@gmail.com[1] , abinayathejashwini@gmail.com[2], carchanahsr@gmail.com[3], dhivyajai.1708@gmail.com[4] , jeevanakalyan244@gmail.com[5]

Abstract- *VLSI affords IC designers the ability to design utilizing less space, this demands to place more components while increasingly utilizing less space translates into a lower margin for error. Achieving both high linearity and high efficiency together in a Power Amplifier (PA) system is challenging. To solve this problem, out-phasing has become one of the most popular efficiency enhancement techniques. CORDIC (Coordinate Rotation Digital Computer) is a hardware-efficient iterative method which uses rotations to calculate a wide range of elementary functions. At the algorithm level, CORDIC shows advantages in both throughput and number of logic gates. FPGA implementation evaluates its EVM (Error Vector Magnitude), PSD (Power Spectral Density), and ACPR (Adjacent Channel Power Ratio) for millimeter-wave application. In the proposed system, architecture can be applied to out-phasing transmitters based on both IQ and phase modulation. Here the customized model of Clocked Radix-2 CORDIC (Coordinate Rotation Digital Computer) design is evaluated. In many advanced CORDIC architectures in, unrolled and pipelined radix-2 CORDIC suits the OPM (Out Phasing Modulator) requirement. CORDIC is proposed to deal with the low efficiency in the trigonometric calculation. Therefore, proposed model achieves high throughput, low power area and reduced architecture. This work will be implemented using VHDL and synthesized using XILINX ISE.*

***Key Words*: Coordinate Rotation Digital Computer (CORDIC), energy efficient, high throughput, millimeter-wave transmitter, out phasing modulator (OPM).**

1.INTRODUCTION

1.1 OVERVIEW

Wireless communication involves transfer of information without any physical connection between two or more points. Because of this absence of any 'physical infrastructure', wireless communication has certain advantages. This would often include collapsing distance or space. The main advantage of a wireless network over a wired one is that users can move around freely within the area of the network with their laptops, handheld devices, etc. and get an internet connection. The need for low-power or efficient output designs are becoming a major issue in high-performance digital system for communication purposes. The proposed model is to achieve high throughput and low power area reduced architecture for milli-meter wave applications. Here, the CORDIC-based OPM will be applied as part of the low-power millimeter-wave out phasing transmitter. Hence the customized model of Clocked Radix-2 CORDIC design is evaluated. The most demanding requirements are satisfied at a reasonable cost of area and power consumption.

VLSI affords IC designers the ability to design utilizing less space, this demands to place more components while increasingly utilizing less space translates into a lower margin for error. Achieving both high linearity and high efficiency together in a Power Amplifier (PA) system is challenging. To solve this problem, out-phasing has become one of the most popular efficiency enhancement techniques. CORDIC (Coordinate Rotation Digital Computer) is a hardware-efficient iterative method which uses rotations to calculate a wide range of elementary functions. At the algorithm level, CORDIC shows advantages in both throughput and number of logic gates. FPGA implementation evaluates its EVM (Error Vector Magnitude), PSD (Power Spectral Density), and ACPR (Adjacent Channel Power Ratio) for millimeter-wave application.

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The tradeoff between linearity and efficiency in power amplifier (PA) designs has been one of the most troublesome difficulties for a long time, especially at the millimeter-wave frequency. The output power, power-added efficiency (PAE), and input signal's probability density function (PDF) curves of a typical millimeter-wave PA. When transmitting both

amplitude and phase-modulated signals (e.g., 256 QAM), the transmitter regularly suffers from a 6–10-dB back off from 1-dB compression point (P1dB) to ensure good linearity, leading to poor average power (PAVG) and poor average PAE (PAEAVG).

To solve this problem, out phasing has become one of the most popular efficiency enhancement techniques. The out-phasing technique makes PAs maintain peak efficiency without sacrificing linearity. For instance, out phasing can increase the PAE of a 60-GHz PA by 11%. Out phasing transmitters split S (t) into two constant-envelope signals S1 (t) and S2 (t) by an Out Phasing modulator (OPM).

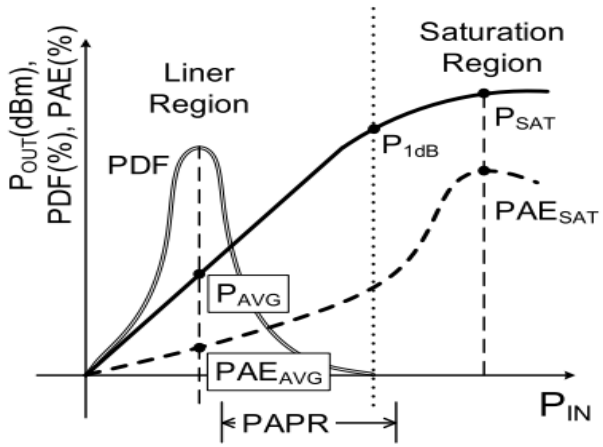

Fig-1: Characteristics of a typical Power Amplifier (curves of PDF, output power, and PAE).

An OPM based on unrolled and pipelined radix-2 Coordinate Rotation Digital Computer (CORDIC) is proposed in this article with algorithm analysis, FPGA measurements, and application-specific integrated circuits (ASIC) evaluation. By comparison with normal rolled CORDIC, the throughput is increased. The out-phasing angle is innovatively calculated by a mixture of single-CORDIC and double-CORDIC algorithms, which significantly reduces the critical path delay. Block diagrams of two out phasing transmitter architecture based on (a) IQ modulation and (b) phase modulation saves considerable hardware consumption. A comparison with several commonly used algorithms reveals that the unrolled and pipelined CORDIC has an advantage in through put power and area and evaluated using the radix-2 version.

1.2 OBJECTIVE

The purpose of this proposal is to basically achieve the following for millimeter-wave transmitter applications.

- higher throughput,
- lower the power consumption and
- Minimizing the area consumption.

2. RELATED WORK

[1] A. Helmy, H. Abdelmohsen, H. Mostafa,A. Elnabawy, M. Moustafa and M. Elbediwy,"A low power CORDIC-based hardware implementation of Izhikevich neuron model",2018. The CORDIC based hardware implementation of the Izhikevich neuron model is introduced. The CORDIC algorithm is used to approximate the square term in Izhikevich equations that describes the neuron response.

[2] N. Bharanidharan, S. Rajaram and M. Chinnathambi, FPGA implementation of fast and area efficient CORDIC algorithm", 2014.The multiplexer based CORDIC reduces both area and speed of operation while pipelining increases both area and speed of operation.

[3] Pramod K. Meher, Leena Vachhani, K.Sridharan, Efficient CORDIC algorithms and architectures for low area and high throughput implementation", 2009.It presents two area efficient algorithms and their architectures based on CORDIC. The FPG implementations consume approximately 8% LUTs of a Xilinx Spartan XC2S200E device and have a slice-delay product of about 3.

3. EXISTING SYSTEM

Existing architecture can be applied to out phasing transmitters dependent on both IQ and phase modulation. CORDIC-based OPM is not applied as part of the low-power millimeter-wave out phasing transmitter. FPGA execution assesses its EVM, PSD, and ACPR for millimeter-wave application.

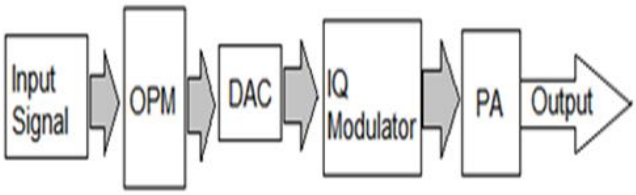

Fig-2: Block Diagram for Existing Architecture

It is communication system architecture. The Out phasing architectures use phase-shift control of multiple saturated or switched-mode branch power amplifiers (PAs) to create a modulated RF output. By modulating with in-phase (I) and quadrature (Q) input, any arbitrary output amplitude and phase can be selected.

4. PROPOSED SYSTEM

The CORDIC-based OPM will be applied as a feature of the low-power millimeter-wave out phasing transmitter. Here the altered model of Clocked Radix-2 CORDIC configuration is assessed. It accomplishes high throughput and low power and area reduced architecture. After processing the input, we get output in few nanoseconds.

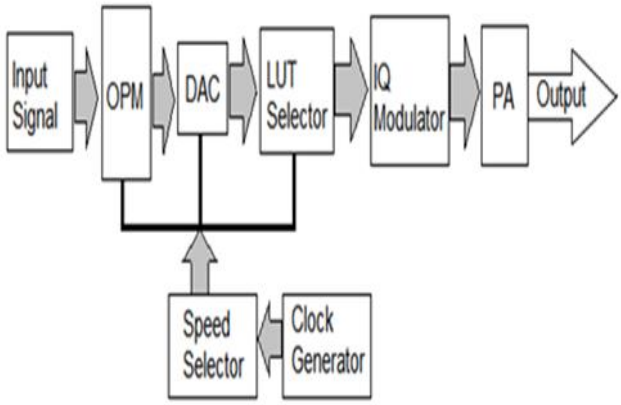

Fig-3: Block Diagram for Proposed Architecture

Before an input signal is being transmitted, it is modulated. Since OPM, LUT and DAC are all associated with Speed selector and Clock Generator the proposed modulator acts as a reconfigurable modulator and their operating frequencies can be varied. Speed variations are possible through Clock generator and the outcome from it is given to Speed Selector.

5. EXPERIMENTAL RESULTS

The universal modulator has been implemented on the Spartan 3E FPGA using three different architectures of CORDIC. From the results it is found that Universal modulator based on multiplexer based two level pipelined architecture is 5\% area and 4\% speed efficient in comparison with the universal modulator based on unrolled CORDIC.

CORDIC WAVEFORMS

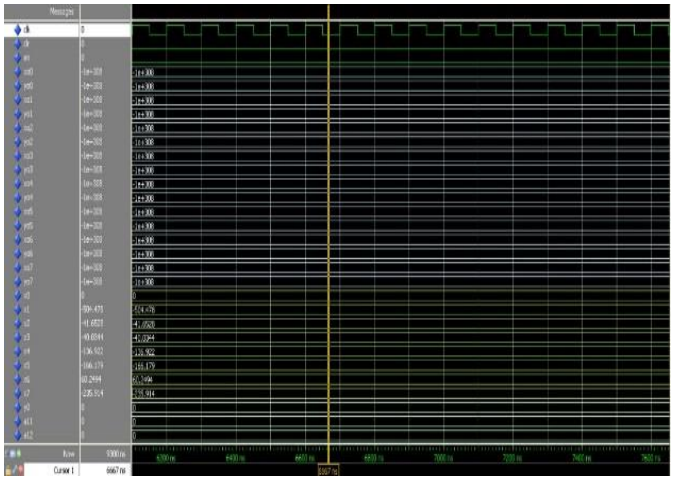

Fig-4: BEFORE ALGORITHM EXECUTION

Fig-5: AFTER ALGORITHM EXECUTION

It acts as a combinational circuit. The CORDIC based OPM is applied to the low-power millimeter-wave out phasing transmitter. The process is performed by using Low power technique. From the results it is found that Universal modulator based on multiplexer based two level pipelined architecture is 5\% area and 4\% speed efficient.

6. CONCLUSION

The universal modulator has been implemented on the Spartan 3E FPGA using three different architectures of CORDIC. From the results it is found that Universal modulator based on multiplexer based two level pipelined architecture is 5\% area and 4\% speed efficient in comparison with the universal modulator based on unrolled CORDIC.

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BIOGRAPHY:

Dr. N. Nagaraju,
Associate Professor,
Electronics And Communication Engineering Department,
Adhiyamaan College of Engineering,
Anna University.