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Design and Comparative analysis of processors based on Harvard and von Neumann architectures

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Abstract - *Computers became a part of our life. The brain behind these computers is a processor. Harvard and von Neumann architectures are the mostly used architectures for designing processors. In this paper simple processors using Harvard and von Neumann architectures are designed and are briefly compared. These processors are Reduced Instruction Set Computers (RISC), meaning the ISA (Instruction Set Architecture) is simple and optimized.*

Key Words: CPU, Verilog, architecture, RISC, modelsim.

1. INTRODUCTION

We cannot imagine performing daily tasks without involving computers. In this era of IT, computers became a crucial part as many manually tasks are now automated. Importance of computers increased because of their ability to accomplish complex tasks accurately. Actual computation required to perform these tasks are done by the Central Processing Unit (CPU) of the computer. CPU is the unit that executes instructions of a program. Generally, all processors follow fetch, decode and execute steps. If one instruction is executed then the whole process is repeated for the following instruction. It is no wonder CPU is considered as the brain of the computer. There are two main architectures used for designing the processors:

i. Von Neumann architecture
ii. Harvard architecture.

In this work we proposed design of two 8-bit Reduced Instruction Set Computer (RISC) processors one using Harvard and another using Von-Neumann architectures. RISC stands for Reduced Instruction Set Computer. In these types of computers, the instruction set is highly optimized. Unlike Complex Instruction Set Computer (CISC), the instruction set of RISCs has only few basic steps, so it makes the hardware simpler to design.

2. HARVARD AND VON-NEUMANN ARCHITECTURES

Basically, there are two types of Computers:

a.) Fixed Program Computers – Their function is very specific and they couldn't be programmed. First computers had fixed programs. Few simple computers still use this design. For example, a calculator is a fixed program computer.

b.) Stored Program Computers – These can be programmed to carry out many different tasks, applications are stored on them, hence the name. They have an instruction set and memory to store instructions, and computation is done according to that stored program.

Both von Neumann and Harvard architectures are for Stored Program Computers.

i. VON NEUMANN ARCHITECTURE:

Von Neumann architecture is first introduced by John von Neumann and others in First Draft of a Report on the EDVAC. It was published in 1945. In that document, Von Neumann described a design of a very high speed automatic digital computing system. The document is further subdivided into: a central arithmetic part, a central control part, memory, input, output, and external memory. Processors based on this architectures store data and instructions in the same memory. Since the bus is common for program data and instructions, data operation and instruction fetch cannot happen simultaneously. This type of storing results in a problem called von Neumann bottleneck. Because of this, the data transfer rate between CPU and memory is limited.

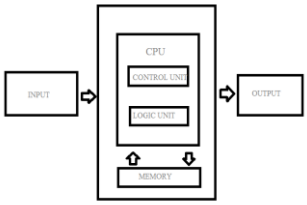

Fig.1 Von Neumann architecture block diagram

ii. HARVARD ARCHITECTURE:

Harvard architecture have separate memories and buses for instructions and program data. So, CPU can read an instruction and read/write data at the same time. Harvard architecture came into picture to eliminate the bottleneck problem in von Neumann architecture. The name Harvard is taken from a relay-based computer Harvard Mark I. For a given circuit complexity, Harvard architecture can be faster than von Neumann since it has separate paths to instructions and data.

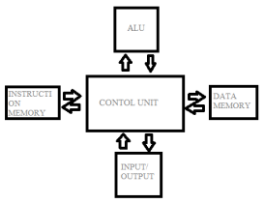

Fig2. Harvard architecture block diagram

3. PROPOSED MODELS

To avoid complexity in comparison of processors, same modules are used in designing both processors. The processors are modeled using Verilog HDL and simulated using the Modelsim tool. The ISA for proposed models is as shown in table1.

Table1. Instruction Set Architecture

Instruction	M-format	ALU src	ALU Control	Branch	Jump	MemtoReg	MemWrite	RegWrite
add	0	0	00	0	0	0	0	1
addi	0	1	00	0	0	0	0	1
sw	0	1	00	0	0	X	1	0
lw	0	1	00	0	0	1	0	1
beq	0	0	01	1	0	X	0	0
slti	0	1	10	0	0	0	0	1
li	1	1	11	0	0	0	0	1
j	X	X	X	X	1	X	0	0

i. PROCESSOR IMPLEMENTED USING HARVARD ARCHITECTURE

The main modules of Harvard design are Control unit, ALU, Register Unit, Program counter unit, Instruction memory and Data memory unit. The top-level schematic is as shown in fig3.

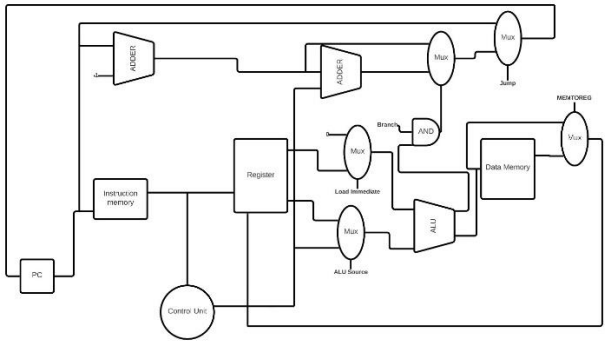

Fig3. Schematic diagram of Harvard processor

A. CONTROL UNIT

Control unit is a part of CPU that directs the operation of the processor. The simulation result of this module is as shown in fig4.

Fig4. Control unit simulation result

B. ARITHMETIC LOGIC UNIT

ALU is a part of CPU that carry out arithmetic and logic operations. The simulation result of this module is as shown in fig5.

Fig5. ALU simulation result

C. REGISTER UNIT

Register unit has registers that can e quickly accessible to CPU. The simulation result of this module is as shown in fig6.

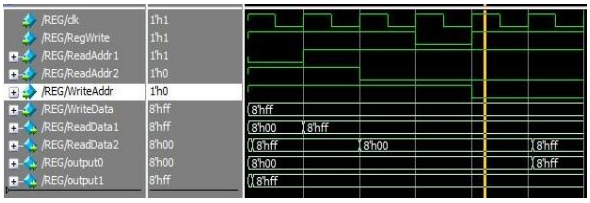

Fig6. Register unit simulation result

D. PROGRAM COUNTER UNIT

Program counter acts as instruction pointer. It holds the address of next instruction to be executed. The simulation result of this module is as shown in fig7.

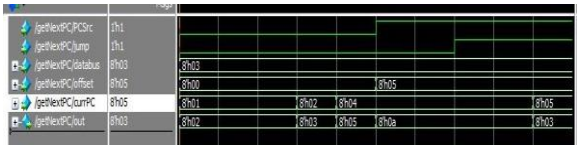

Fig7. Program Counter simulation result

E. INSTRUCTION MEMORY

Instruction memory contains instructions. This memory does not have write signals. It only has read signals. The simulation result of this module is as shown in fig8.

Fig8. Instruction memory simulation result

F. DATA MEMORY

In data memory you can read and write values. The simulation result of this module is as shown in fig9.

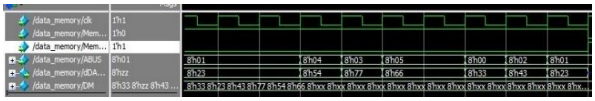

Fig9. Data memory simulation result

G. CPU

The simulation result of overall CPU is as shown in fig10.

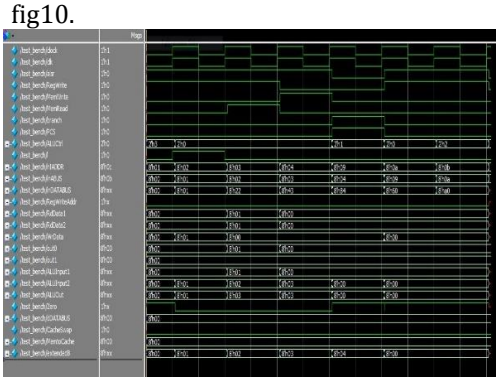

Fig10. CPU simulation result

ii. PROCESSOR IMPLEMENTED USING VON-NEUMANN ARCHITECTURE

The main modules of Von-Neumann design are Control unit, ALU, Register Unit, Program counter unit and Memory unit. The Control unit, ALU, Register Unit and Program counter unit used in this design is same as those modules used in Harvard design. The only difference between modules of these two designs is that the Harvard has two memory modules – one for instruction and other for data, whereas von Neumann design has a single memory module. The top-level schematic diagram of this processor is as shown in fig11.

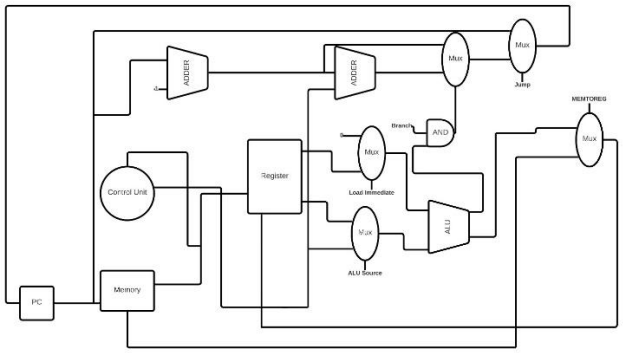

Fig11. Schematic diagram of von Neumann processor

A. MEMORY UNIT

Unlike Harvard architecture, von Neumann has single memory section. This memory is used for bot instructions and data, The simulation result of this memory module is as shown in fig12.

Fig12. Memory unit simulation result

B. CPU

The overall simulation result of this CPU based on von Neumann architecture is as shown in fig13.

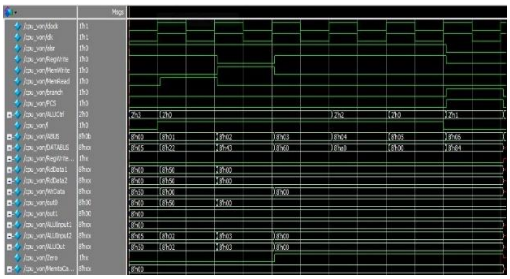

Fig13. Von Neumann CPU simulation result

4. CONCLUSION

This paper presented the design and comparison of two processors, one using Harvard and another using von Neumann architecture. All modules used in this work are verified through exhaustive simulations. Although there is no significant difference in the performance of these proposed 8-bit processors, the difference would be obvious in high performance applications.

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