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Design and Implementation of Trinary Cascade 9-Level H-Bridge Inverter

Single Phase Inverter by Genetic Algorithm

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Abstract - *A multilevel inverter having more number of levels is responsible for reducing the harmonic content in output voltage. Trinary cascaded H-bridge 9-level inverters designed using unequal input DC power sources as well as less number of switches. If DC voltage sources are having the ratio of 1:3, then the inverter is called as trinary asymmetric multilevel inverter. Genetic Algorithm is used to implement proposed topology.*

Key Words: multilevel, Trinary, Genetic Algorithm, Asymmetric, PWM

1. INTRODUCTION

The proposed technique is brought into use to eliminate the traditional logic gate pulse technique [6] [7] [8] which is the well-known conventional method. There is a pulse generator for giving pulses to the switches which is designed by Genetic Algorithm [4]. A multilevel inverter having more number of levels can be very usefull in reducing the harmonic content in voltage at output. Cascaded Trinary H-bridge multilevel inverters are designed with using unequal DC input power sources and less switches. If DC voltage sources are having the ratio of 1:3, then the inverter is called as trinary asymmetric multilevel inverter. Genetic Algorithm is used to implement this topology. Binary asymmetric multilevel inverter producing seven level output requires 8 switching devices.

Trinary asymmetric multilevel inverter is able to produce nine levels with having eight switching devices [2]. Such converters can be used with other techniques as fuzzy logic also. With the use of modulation index as input, rules for the fuzzy logic controller (FLC) can open various possibilities in directly producing the pulses [3]. But this paper explains the GA technique for inverter operation [1]. Main advantage of a trinary asymmetric topology as compaired to binary asymmetric topology is using the same number of switches. However such kind of asymmetric inverter will require input DC voltage sources with having different values.

2. DESIGN OF INVERTER

Design of the proposed single phase trinary 9-level inverter is entirely depends upon the Input DC voltage levels. The value for each input DC source can be obtained using the Equation,

$V_k = 3^{(k-1)} V_{dc}$, k = 1,2,3,.....h (1)

Number of voltage levels 'N_L' are obtained as,

$N_L = 3^h$ (2)

'N_S' Number of switching devices,

$N_S = 4h$ (3)

'V_{0max}' Maximum output voltage,

$V_{0max} = (3^h - 1)\frac{Vdc}{2}$ (4)

Hence for 9 level inverter there must be two different input dc sources and 8 switches. Circuit diagram of the asymmetric inverter is shown in fig 1. It is having two bridges, bridge one is having the input voltage as $Vdc/4$ and the second one is having $3Vdc/4$. The voltage levels are shown in figure 2.

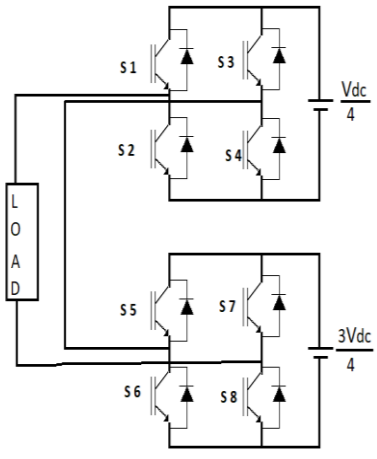

Fig -1: Trinary 9-Level Inverter

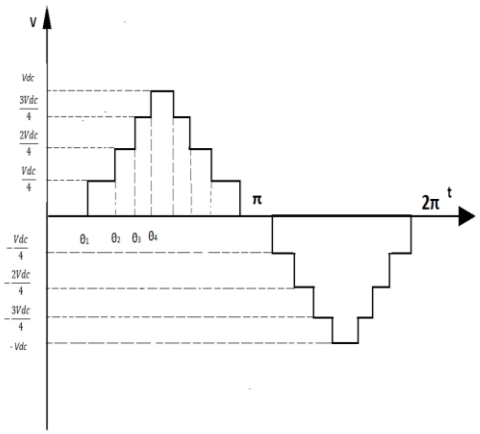

Fig -2: Voltage levels with respect to firing angles

2.1 CALCULATION OF FIRING ANGLES

By manipulating the opening and closing of the switches of bridge-1 correctly, an output voltage V1 can be made equal to $V_{dc}/4$, 0, $V_{dc}/4$ where an output voltage of bridge-2 is can be made $3V_{dc}/4$, 0 or $3V_{dc}/4$ by closing and opening its switches. Therefore at the output end, the voltage of the inverter will have nine values $V_{dc}/4$, $2V_{dc}/4$, $3V_{dc}/4$, V_{dc}, 0, $V_{dc}/4$, $2V_{dc}/4$, $3V_{dc}/4$, and V_{dc}. With the use of genetic algorithm the firing angles for the switches can be easily calculated. For better performance 0.9 is selected as modulation index. The required firing angles can be calculated and they are as shown in the following table. Where $\theta_1 < \theta_2 < \theta_3 < \theta_4 < (\frac{\pi}{2})$.

Table -1: Calculated firing angles for different MI

Switching Angles in Radians				
MI	θ_1	θ_2	θ_3	θ_4
0.75	0.131	0.265	0.623	1.571
0.8	0.172	0.356	0.670	1.055
0.85	0.068	0.368	0.469	0.947
0.9	0.039	0.240	0.396	0.685

The maximum fundamental voltage (V1max= 4Vdc/4) can be perfectly obtained when the switching angles of all switches are zero. The equation for m_a is given as follows.

$$m_a = \frac{\pi V1}{4sVdc} \quad (5)$$

from this, the following equations can be formed as,

$$\cos(\theta 1) + \cos(\theta 2) + \cos(\theta 3) + \cos(\theta 4) = 4ma \quad (6)$$

$$\cos(5\theta 1) + \cos(5\theta 2) + \cos(5\theta 3) + \cos(5\theta 4) = 0 \quad (7)$$

$$\cos(7\theta 1) + \cos(7\theta 2) + \cos(7\theta 3) + \cos(7\theta 4) = 0 \quad (8)$$

$$\cos(9\theta 1) + \cos(9\theta 2) + \cos(9\theta 3) + \cos(9\theta 4) = 0 \quad (9)$$

3. MATLAB SIMULATION STUDY

The trinary 9-level inverter is modelled using MATLAB/SIMULINK software. Two input voltage sources used are 80.25V & 240.75V. All switches here are considered to be ideal. Pulse generator is used to give desired firing angles to all switches. Simulation figure is shown in figure 3,

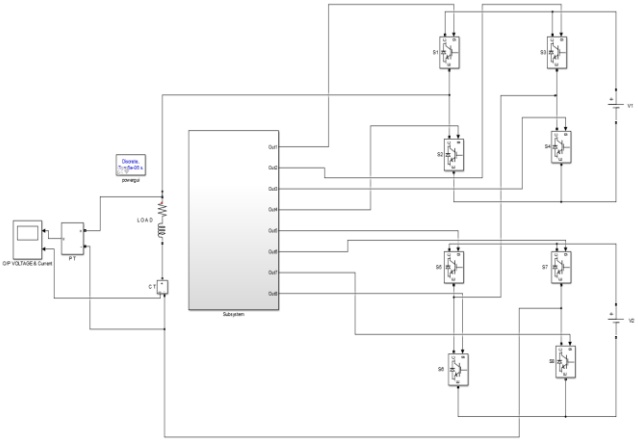

Fig -3: Simulink diagram of trinary 9-level inverter

Switching pulses are given with the use of firing angles calculated are shown in fig 4.

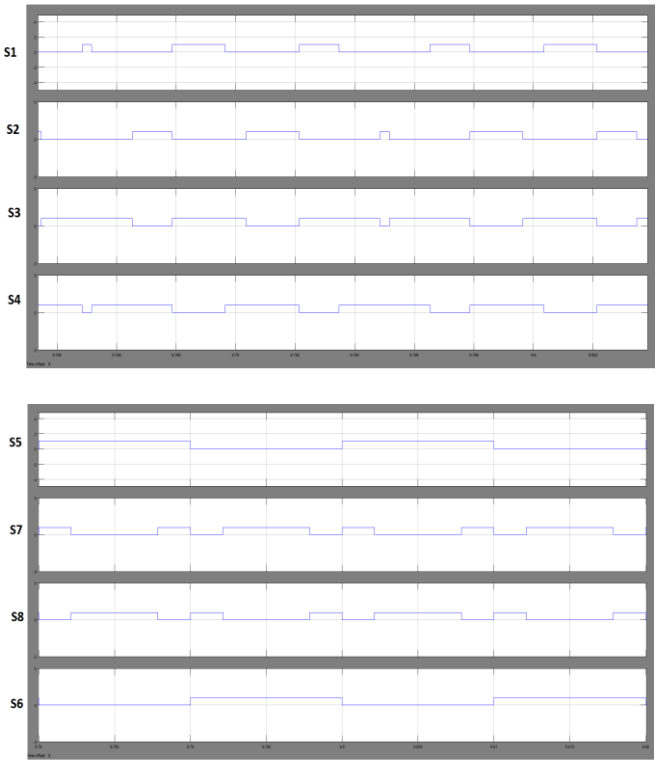

Fig –4: Switching signals for the switches

4. HARDWARE IMPLEMENTATION

Single phase asymmetric trinary cascaded H-bridge nine level inverter is implemented in real time. The block diagram of the overall experimental setup is shown as in Figure 5. The various units involved within the fabrication of hardware are power supply unit, battery unit, ARDUINO UNO controller, gate driver circuit and multilevel inverter. Driver circuits operates at two different voltage levels, thus multi-output power supply unit becomes a vital part of the proposed system. The controller used in the proposed system is ARDUINO UNO controller which operates at +5V DC supply. For implementing the hardware of the proposed inverter, MOSFETs IRF840 are used as switches. For giving gate pulses TLP250 Gate Driver circuit is used.

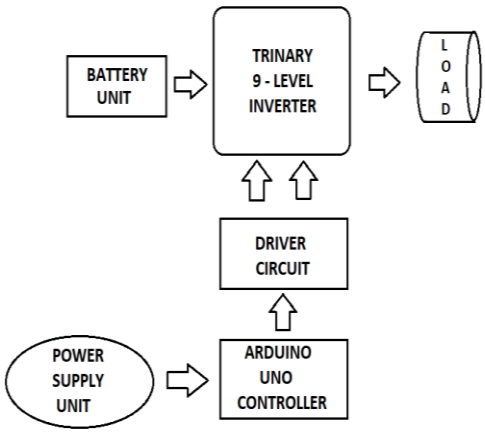

Fig –5: Block diagram of experimental setup

Battery unit consists of two batteries which are used to supply bridge-1 and bridge-2 of the asymmetric cascaded inverter. DC voltages of 80V and 240V are given to the bridge 1 and bridge 2 respectively. The main advantage of this controller is the ability to generate PWM pulses using pre-calculated values. This reduces the overall computational time required in determining the switching times for inverter legs, this makes the system more suitable and reliable real time implementation for larger drives.

5. FINAL RESULTS

Final results are obtained with having 1000 ohm resistance as a load. Output of bridge 1 and bridge 2 are shown in Figure 6. (a) & (b) respectively. Output of inverter is shown in fig. 6 (c). Arduino controller generates the required pulse for the switching devices to produce nine level output voltage. Once the asymmetric multilevel inverter gets the required DC voltage as input and the required PWM signals from the controller, the inverter produces a nine level output voltage.

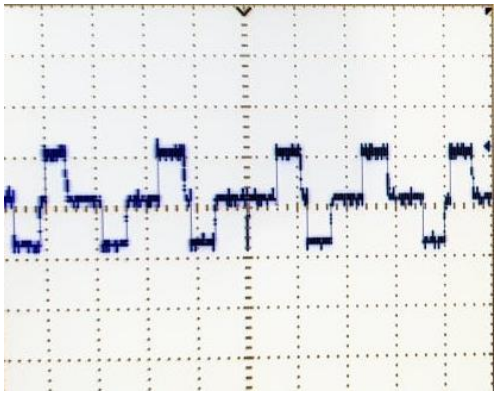

Fig –6(a): V_{01}

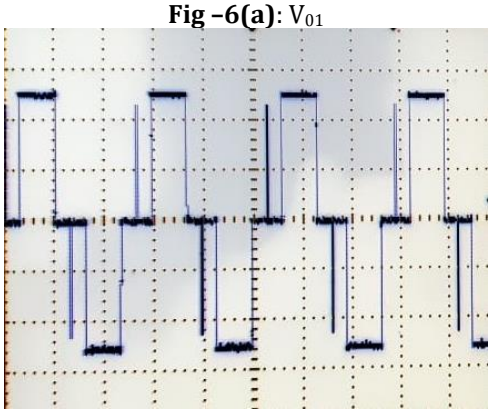

Fig –6(b): V_{02}

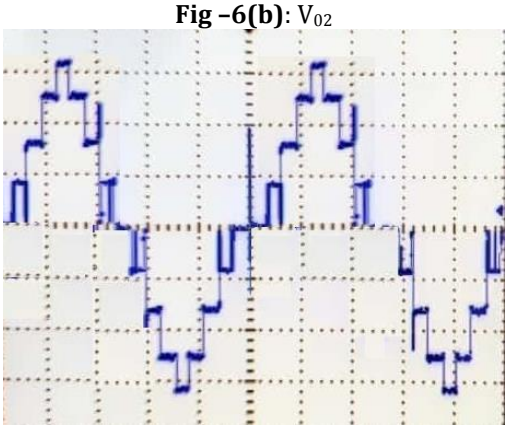

Fig –6 (c): Inverter output

6. CONCLUSIONS

In this paper, a detailed analysis of asymmetric trinary cascaded H-bridge multilevel inverter topology is presented. Genetic Algorithm optimization method is applied to trinary cascaded multilevel inverters. Topology presented in this paper is having less number of switches compared to the conventional symmetric cascaded H-bridge inverter. Comparing the simulation and hardware results, this topology shows better performance and also requires the same number of switches which are used in the binary asymmetric cascaded seven level inverter. Hence trinary asymmetric topology is definitely advantageous over the conventional symmetric topologies.

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