

EFFECT OF MOTH FLAME OPTIMISATION ON TOTAL HARMONIC DISTORTION FOR SELECTIVE HARMONIC ELIMINATION

Jyoti¹

22180703 M.Tech
Electrical Engineering Department
Swami Devi Dayal Institute of Engineering
and Technology

Manish Singh²

Assistant professor (Guide)
Electrical Engineering Department
Swami Devi Dayal Institute of Engineering
and Technology

Abstract: Multilevel Inverter (MLI) has lately emerged as a very significant option in the areas of energy regulation with high-intensity medium voltage. It consists of number of advantages; however, despite of its benefits, its performance is majorly affected due to the presence of harmonics. Numerous approaches have been presented in literature to reduce the harmonic distortion in MLIs. However, it has been analyzed that they did not yield effective results as they consists of certain limitations. Therefore, to overcome the previous limitations and to efficiently reduce the harmonics from MLIs, a novel approach is proposed in this work. In the proposed work, moth flame optimization (MFO) approach is implemented. The main purpose of designing the novel approach is to remove the harmonic distortion and selective harmonic of 5th, 7th and 11th order in MLIs and achieve better results. This proposed approach is implemented in the MATLAB environment to analyze its performance. Also, the comparative analysis is performed between proposed approach and previous approaches in terms of THD. And all the obtained results of simulation demonstrate the efficacy of proposed approach over conventional ones.

Index Terms - Multilevel Inverters (MLIs), Selective Harmonic Elimination (SHE), Total Harmonic Distortion (THD), Moth Flame Optimization (MFO)

I. INTRODUCTION

Multilevel Inverter (MLI) has lately emerged as a very significant option in the areas of energy regulation with high-intensity medium voltage. Staircase waveform can be generated by synthesizing the terminal voltage of the AC output from several DC voltages. MLIs have been a realistic and effective method for eliminating losses from switches. The synthesized output provides new steps on the DC side as the number of voltage levels increases, producing the result that challenges the sinusoidal wave with the smallest number of harmonic distortion. The general function of MLI is to establish a sinusoidal voltage from many voltage rates characteristically derived from condenser voltage sources [1].

MLIs are calculated for a growing range of applications due to their large power efficiency combined with smaller switching losses and harmonics of lower performance. MLIs have been a proficient and realistic approach for

rising strength and reducing harmonics of AC loads [2]. Most desirable characteristics of MLIs are as:

- MLI can generate exceptionally low dv / dt output voltages and distortion.
- MLI, draw feedback current, with very little distortion.
- MLI generates smaller common-mode (CM) voltage, thus reducing the stress of the motor bearings. In addition, CM voltages may be removed using advanced modulation techniques.
- MLI can operate at a lower frequency switching technique.

The stepwise output voltage is the key benefit of MLIs as opposed to conventional two-level voltage source inverters. This results in higher power efficiency, lower switching losses, improved electromagnetic stability, higher voltage ability, and a transformer's pointlessness at the stage of distribution voltage, thereby reducing the expense.

The MLI has been deployed in numerous applications varying from medium to high-power stages, such as power conditioning systems, motor drives, as well as traditional and modern generating capable electricity [3]. The different MLI structures are [4]:

1. Diode-clamped (neutral-clamped)
2. Cascaded H-bridge inverter
3. Capacitor-clamped (flying capacitors).

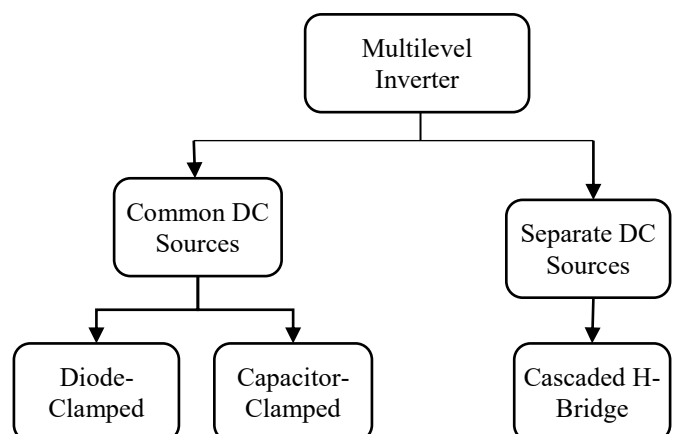


Figure 1: MLI Topologies

MLI topologies are different ways to reduce the harmonic content which keeps the number of switches small. In essence, Harmonics are unwanted higher frequencies that superimposed a distorted wave pattern on the fundamental waveform. They can produce electric waveforms with greater voltage levels, at the cost of higher switching and control algorithm complexity. The harmonic efficiency is further enhanced where the preprogrammed switching schemes defined as the SHE and Selective Harmonic Mitigation (SHM) are used with MLI.

SELECTIVE HARMONIC ELIMINATION (SHE):

SHE is a method for eliminating certain chosen harmonics from the square wave by adding extra square wave switches. Back in 1973, it was Hasmukh and Richard who developed the SHE methodology [5]. In SHE, the output is turned on and off many times over each half cycle of the square wave, and these changes are spread equally over each half cycle with quarter-wave symmetry. The immediate transition of each switching is measured from the y-axis is called the switching angles but every set of switching angles is linked through Fourier who developed the transcendental trigonometric equations mathematically to reflect the harmonic content of a square wave. When implementing the SHE PWM (pulse-width modulation) by properly switching on and off at the preferred moment, some odd harmonics, usually a set of lower order harmonics, can be selectively eliminated from the inverter's output voltage and the magnitude of the fundamental voltage is regulated [6]. The higher-order harmonics can be quickly extracted through limited physical scale passive filters and at a related decreased expense.

There are different solving algorithms and techniques for SHE such as numerical approaches, optimization based approaches and other approaches. Some of the techniques are reviewed in next section:

II. LITERATURE REVIEW

Numerous approaches have been proposed in order to remove the harmonic distortion or selective harmonics in the MLIs. Some of the techniques presented in literature are reviewed which are discussed in this section:

Improvement of harmonics can be viewed as an advanced way of reduction of harmonics. The work [7] applied an innovative version of the process of particle swarm optimization (PSO) to 7-level inverters in this way.

The paper [8] proposed the latest approach for optimizing harmonic stepped waveform by using harmony quest algorithm for MLIs.

The work done in [9] addressed the removal of substantial lower order 5th harmonic in five-stage cascaded inverters using sine cosine algorithm (SCA).

S. Bhalerao, et al., [10] had introduced the design and real-time implementation of the Bipolar SHE-PWM in the Single-Phase 2-level Inverter for Lower Order Harmonic Suppression scheme.

The research [11] described in depth the implementation of the SHE-PWM technique to thirteen-level cascaded sub MLI.

The reduction of unnecessary harmonics in a MLI with equivalent DC sources was described in the paper [12] using bat evolutionary optimization method.

A. Kavousi, et al. [13] introduced the Bee optimization approach in a cascaded MLI for harmonic elimination.

The study [14] explored the critical parameter modeling methodology for single-phase systems on a cascaded H-Bridge (CHB) with SHE/ SHC.

M. T. Yaqoob [15] provided the review on MLIs for SHE that PSO is stronger in terms of time and output than the Genetic Algorithm, Imperialist Competitive Algorithm, Bee Algorithm, and Differential Algorithm.

Application of PSO algorithm to find the optimum solution of the flipping angles in a 3-ph seven-level Cascaded MLI with unequal DC sources for the removal of lower-order harmonics was described in the paper [16].

In the article [17], the author had suggested a procedure for solving the optimization by using SCA algorithm to eliminate the selective harmonics in CHB MLI.

In [18], the optimization based technique had been used to eliminate the 5th, 7th and 11th order harmonics of nine-level inverter. For this, author had presented SCA approach.

However, it has been analyzed that SCA comprised of some problems that affect the system's performance. Therefore, the SHE problem cannot be eliminated completely with the SCA and a novel algorithm should be implemented with better performance.

III. PRESENT WORK

To remove harmonic distortion in MLIs, various optimization algorithms based approaches are designed and some of these are reviewed in above section. One of these approaches proposed is SCA based approach which had been considered as effective approach. However, as mentioned above, it is analysed that SCA comprises of various issues. These issues include slow convergence and falling into local solutions. Considering these demerits of SCA algorithm, there is a requirement of modifications in the existing model.

Thus, a novel approach is designed in which moth flame optimization (MFO) algorithm is implemented in the place of SCA. MFO algorithm is inspired by the navigation methods of the moths. Moths are capable of maintaining the fixed angle with the moon that is helpful in making the right angle for switching pulses of the diodes.

As 9-level inverter is utilized in the existing technique, the main purpose of designing the novel approach is to remove the harmonic distortion and selective harmonic of 5th, 7th and 11th order in MLIs and achieve better results. MFO is responsible for making the best decision about switching the pulses and efficient conversion from DC to AC. MFO seems to be better in terms of convergence due to its navigation method. It is also better than SCA because it does not fall into the local solutions.

Therefore, by proposing MFO based optimization technique, the problem of SHE can be eradicated.

The schematic diagram of the proposed system is shown below:

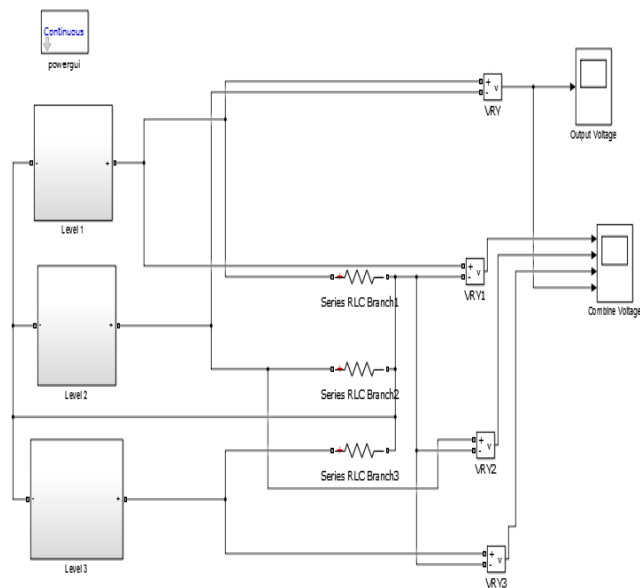


Figure 2: Schematic diagram of proposed system

The figure 2 shows the simulink model of the proposed system. In this, the three different levels i.e. level 1, level 2 and level 3 are designed. These three levels generate the three-phase output and return the voltage. The level here represents the inverter i.e. 9 level cascaded H-bridge (CHB) MLI. The pulses that are given to the inverter are generated by using the MFO optimization algorithm. These pulses are generated on the basis of switching angle. These pulses are then fed to the 9-level CHB MLI which then generates the output voltage. The output voltage of all the three levels are then combined lastly which gives the overall generated output voltage of the system. The

performance of this system is then analyzed further to verify that whether the generated output of the proposed system gives the efficient results in terms of harmonic distortion. The results of the performance analysis obtained are represented in the next section.

IV. RESULTS AND DISCUSSION

As stated in the above section, the new approach i.e., MFO is used in the proposed work to resolve the problem of SHE in MLIs. Now, this proposed approach is implemented in the MATLAB environment and simulation is performed in order to analyze its performance in terms of different parameters. And obtained results of the simulation are discussed in this section.

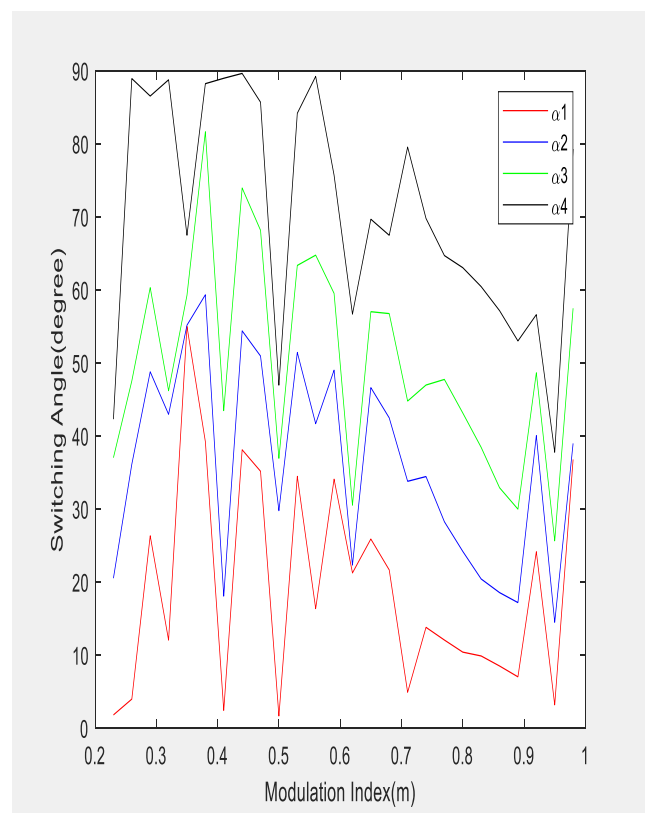


Figure 3: Switching angles in proposed approach with respect to modulation index

The graph shown in figure 3 illustrates the calculated switching angles i.e. α_1 , α_2 , α_3 and α_4 with respect to modulation index (m). The modulation index is defined mathematically as:

$$M = \frac{V_f * s}{V_{dc}} \quad (1)$$

In which, s represents number of dc sources, V_{dc} represents supply voltage and V_f implies fundamental voltage. In the graph, the y-axis calibrates the value of switching angles that ranges from 0 to 90 degree, and x-axis calibrates the values of modulation index ranging from

0.2 to 1. The switching angled are calculated in such a way that they can result in reduction of THD of the system.

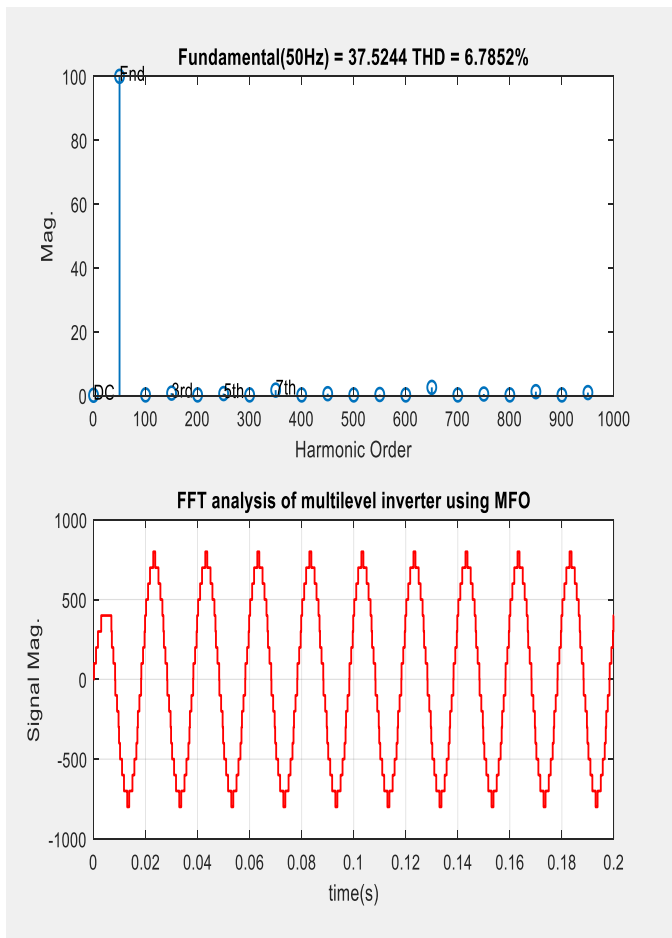


Figure 4: FFT analysis of MLI using proposed MFO

The FFT analysis of the MLI is performed using proposed MFO approach as shown in figure 4. The above graph in the figure shows the magnitude of 3rd, 5th and 7th order harmonics and THD which is 6.7852%. In that graph, the y-axis and x-axis calibrates the values of magnitude and harmonic order, respectively. In this, the range of magnitude varies from 0 to 100 and that of harmonic order varies from 0 to 1000. And the below graph in the figure exemplifies the signal magnitude of FFT analysis of MLI. In this graph, the signal magnitude of the MLI using proposed approach is shown with respect to varying time. The signal magnitude varies between range -1000 and 1000, and the time varies from 0sec to 0.2 sec. The results imply that proposed approach minimizes the targeted harmonics efficiently.

Now, the comparative analysis is performed between proposed MFO approach and conventional approaches i.e. NR and SCA approach, in term of THD and the obtained results are represented below:

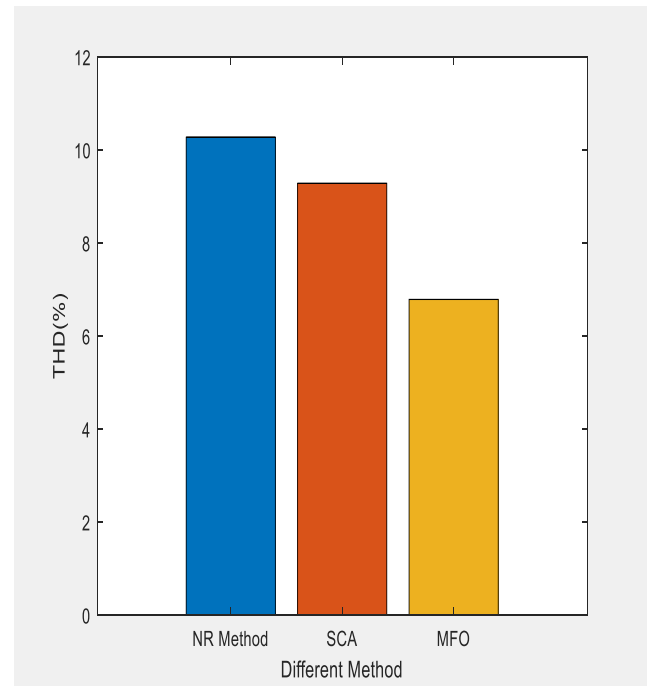


Figure 5: Comparative analysis in terms of THD

The bar graph shown in figure 5 depicts the results of comparative analysis performed between proposed MFO approach and conventional NR and SCA approaches in terms of THD. On analyzing the graph, it is clearly depicted that among these three approaches NR is the most inefficient approach as it has the highest value of THD. Whereas, SCA is quite efficient than NR as its THD values are lower than NR. However, the THD value of proposed MFO approach is even lower than that of SCA, which demonstrates the superiority of the proposed approach over these two conventional approaches i.e. SCA and NR, with regards to THD.

The values of two different parameters i.e. THD and improvement, for proposed and conventional approaches, are recorded in table 1.

Sr. No.	Parameter	NR	SCA	MFO
1	THD (%)	10.27	9.28	6.78
2	Improvement (%)	--	9.63	26.9397

Table 1: THD and improvement values of different approaches

The proposed and conventional approaches are compared in terms of their THD and improvement, and the obtained values are recorded in above table. It is clearly demonstrated from the shown values that NR has the maximum value of THD i.e. 10.27%, followed by SCA i.e. 9.28%, whereas proposed MFO approach has the minimum

value of THD i.e. 6.78., and thus it is the most efficient technique than other two previous approaches. Also, the NR does not shows any improvement, whereas, the value of improvement of SCA is 9.63% and that of proposed MFO is 26.9397%, which is highest than other approaches. Thus, this demonstrates the efficacy of the proposed approach.

V. CONCLUSION AND FUTURE SCOPE

The novel approach is designed in the proposed work to remove the harmonic distortion and selective harmonic of 5th, 7th and 11th order in MLIs. In this proposed approach, the MFO is used to resolve the problem of SHE. The simulation of this proposed approach is then carried out in the MATLAB environment to analyze its performance. For simulation, different parameters are taken into consideration such as switching angle, THD and FFT analysis. Also, the comparative analysis is performed between proposed approach i.e. MFO-based approach and conventional approaches i.e. NR and SCA in terms of THD. And obtained results revealed that proposed approach is more efficient than the previous approaches in terms of THD as it has lowest THD i.e. 6.78 than the other approaches. Also, the proposed approach has the highest improvement value i.e. 26.9397 than the previous two approaches. Therefore, from all the results, it has been demonstrated that proposed approach has high efficacy with regards to all the considered parameters.

For future work, the fitness function of the system can be updated and system performance can be then analyzed. And also, the hybrid optimization technique can be used in it for elimination of harmonic distortions from the MLIs.

REFERENCES

- [1] Rajaram, M "Certain investigations on metaheuristic algorithms based selective harmonic elimination in multilevel inverters", <http://hdl.handle.net/10603/182142>, 2016.
- [2] Lai, J. S. and Peng, F. Z. "Multilevel converters - A new breed of power converters," IEEE Transactions on Industrial Applications, Vol. 32, No.3, pp. 509-517, 1996.
- [3] Rodriguez J., Franquelo L.G., Kouro S., Leon, J.I., Portillo R.C., Prats M.A.M., Perez M.A. "Multilevel Converters: An Enabling Technology for High-Power Applications", Proceedings of the IEEE , vol.97, no.11, pp.1786-1817, Nov. 2009.
- [4] Anjali Krishna R, Dr L Padma Suresh, "A Brief Review on Multi Level Inverter Topologies", 2016, International Conference on Circuit, Power and Computing Technologies (ICCPCT)
- [5] Hasmukh S Patel and Richard G Hoft, "Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part I-harmonic elimination", IEEE Transaction on Industry Applications, vol, I A-9, no.3, pp. 310-317, 1973
- [6] M. Mythili and N. Kayalvizhi, "Harmonic minimization in multilevel inverters using selective harmonic elimination PWM technique," 2013 International Conference on Renewable Energy and Sustainable Energy (ICRESE), Coimbatore, 2013, pp. 70-74, doi: 10.1109/ICRESE.2013.6927790.
- [7] K. Kaviani, S. H. Fathi, N. Farokhnia and A. J. Ardakani, "PSO, an effective tool for harmonics elimination and optimization in multi-level inverters," 2009 4th IEEE Conference on Industrial Electronics and Applications, Xi'an, 2009, pp. 2902-2907, doi: 10.1109/ICIEA.2009.5138740.
- [8] B. Majidi, H. R. Baghaee, G. B. Gharehpetian, J. Milimonfared and M. Mirsalim, "Harmonic optimization in multi-level inverters using harmony search algorithm," 2008 IEEE 2nd International Power and Energy Conference, Johor Bahru, 2008, pp. 646-650, doi: 10.1109/PECON.2008.4762555.
- [9] N. Sahu and N. D. Londhe, "Selective harmonic elimination in five level inverter using sine cosine algorithm," 2017 IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI), Chennai, 2017, pp. 385-388, doi: 10.1109/ICPCSI.2017.8392322
- [10] S. Bhalerao, S. Pawar and N. Patwardhan, "Design and Implementation of Bipolar SHE-PWM Single Phase Inverter for Lower Order Harmonic Suppression," 2018 3rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT), Bangalore, India, 2018, pp. 1066-1071, doi: 10.1109/RTEICT42901.2018.9012349
- [11] P. Mamatha and C. Venkatesh, "Performance Improved Multilevel Inverter with Selective Harmonic Elimination," 2017 International Conference on Recent Trends in Electrical, Electronics and Computing Technologies (ICRTEECT), Warangal, 2017, pp. 133-138, doi: 10.1109/ICRTEECT.2017.24.
- [12] K.Ganesan, K.Barathi, P.Chandrasekar, D.Balaji "Selective Harmonic Elimination of Cascaded Multilevel Inverter Using BAT Algorithm" Volume 21, 2015
- [13] A. Kavousi, B. Vahidi, R. Salehi, M. K. Bakhshizadeh, N. Farokhnia and S. H. Fathi, "Application of the Bee Algorithm for Selective Harmonic Elimination Strategy in Multilevel Inverters," in IEEE Transactions on Power Electronics, vol. 27, no. 4, pp. 1689-1696, April 2012, doi: 10.1109/TPEL.2011.2166124.
- [14] H. Zhao, S. Wang and A. Moeini, "Critical Parameter Design for a Cascaded H-Bridge With Selective Harmonic Elimination/Compensation Based on Harmonic Envelope Analysis for Single-Phase Systems," in IEEE Transactions on Industrial

Electronics, vol. 66, no. 4, pp. 2914-2925, April 2019, doi: 10.1109/TIE.2018.2842759.

- [15] M. T. Yaqoob, "Selective Harmonic Elimination in Cascaded H-Bridge Multilevel Inverters using Particle Swarm Optimization: A review," 2019 13th International Conference on Mathematics, Actuarial Science, Computer Science and Statistics (MACS), Karachi, Pakistan, 2019, pp. 1-5, doi: 10.1109/MACS48846.2019.9024783
- [16] S. D. Patil and S. G. Kadwane, "Application of optimization technique in SHE controlled multilevel inverter," 2017 International Conference on Energy, Communication, Data Analytics and Soft Computing (ICECDS), Chennai, 2017, pp. 26-30, doi: 10.1109/ICECDS.2017.8390050
- [17] P. Mishra and A. Mahesh, "Sine cosine algorithm based staircase modulation for cascaded H-bridge inverter," 2019 3rd International conference on Electronics, Communication and Aerospace Technology (ICECA), Coimbatore, India, 2019, pp. 914-919, doi: 10.1109/ICECA.2019.8822115.
- [18] Sahu, N., & Londhe, N. D"Optimization based selective harmonic elimination in multi-level inverters", 2017 National Power Electronics Conference (NPEC).