Low Power and Highly Reliable 125-MHz Relaxation Oscillator Using 45nm CMOS Technology

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Abstract - *To realize an on-chip reference clock with phase noise and temperature stability are important performance indexes. This relaxation oscillator was fabricated in the 45nm CMOS Technology under the supply of 0.6-V. The whole oscillator consumes 86.07 µW. The measured average of oscillation frequency with and without compensation are 125MHz obtained. The approach was done by using Switched-Capacitor.*

Key Words: Temperature stability, digital compensation, phase noise, relaxation oscillator, temperature coefficient (TC), Switched-Capacitor.

1. INTRODUCTION

In this gadgets of application the supply of clock generation may be a main priority one in nowadays technology, like wireless sensing nodes, Implantable Biomedical devices and Wearable Health observance systems. To understand an on-chip reference clock with phase noise and temperature stability are two important performance indexes [1].

A swing-boosted differential topology is adopted to scale back the noise of the comparator by increasing the signal slew rate at the comparator inputs [2]. A construction topology [3] suppresses the comparator noise by increasing the transition slope at the comparator output flipping time. During this transient, a digital compensation loop is given to scale back the temperature coefficient (TC) of the relaxation oscillator [4]. Additionally, the on-chip voltage references are completed. To scale back the power consumption, a voltage reference [6] is modified to get the reference voltages Vref,OSC and Vref,cal for the comparator and the digital compensation loop, severally. To scale back the noise and also the temperature variation, a two-transistor voltage reference [7] is employed to bias the current source I1.

For example, by employing a temperature-independent current source in [5], the simulated phase noise at 1-kHz offset frequency is degraded by 31.16 dBc/Hz. Thus, the noise contribution of voltage reference VREF ought to be low to avoid the deterioration of the phase noise. Furthermore, its oscillation frequency is depends on the gate–source voltage VGS of the transistor M1, that is sensitive to the temperature variations.

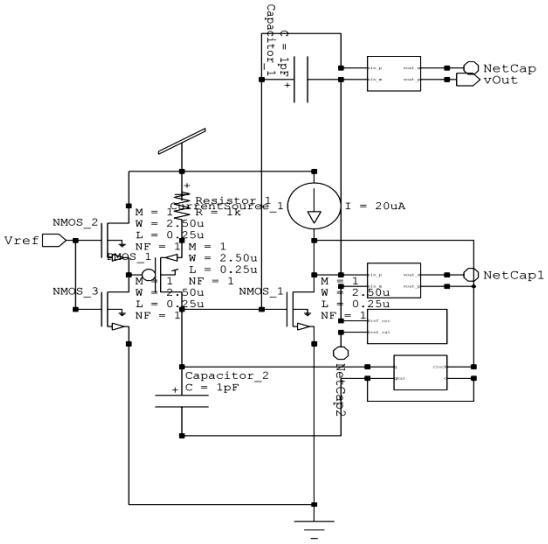

Fig -1: Relaxation Oscillator

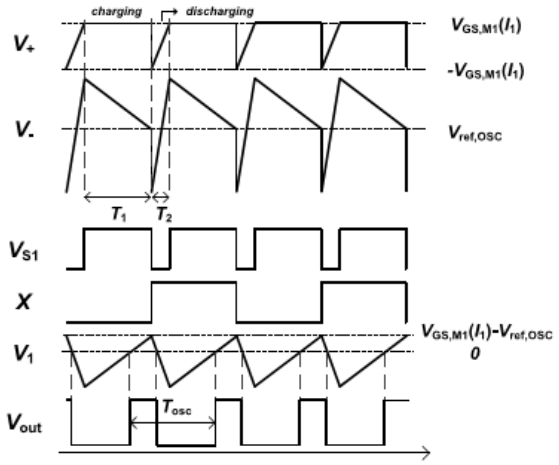

Fig -2: Waveforms of Relaxation Oscillator

2. CIRCUIT REPRESENTATION

The switch S1 shown in Fig. 1 is completed by a PMOS transistor. The waveforms of the relaxation oscillator are shown in Fig. 2. The operation of this relaxation oscillator is split into a charging phase and a discharging one, severally. The corresponding charging time and discharging time are T1 and T2, severally. Within the charging phase, the switch S1 is open and also the current I1 charges capacitance C1. A hard and fast gate-to-source voltage VGS,M1(I1) is established since I1

flows through the transistor M1. During this phase, voltage V+ is equal to VGS,M1(I1) and voltage V− decreases with regard to time. When V− becomes lower than Vref,OSC, the output of the comparator CMPOSC toggles and also the voltage on capacitance C2 is reversed. This oscillator then works within the discharging phase and also the switch S1 is closed. The current I2 flows through capacitance C1 to cut back V1 and increase V−. Capacitor C2 is charged by the currents I1 and I2 toward voltage VGS,M1(I1). Once V− becomes higher than Vref,OSC, the output of the comparator CMPOSC toggles. The switch S1 is open, and also the oscillator goes back to the charging phase. Both the comparators CMPOSC and CMPOUT are realized by the differential amplifiers. The charge Qsub subtracted from capacitance C1within the discharging phase is given as

$$Qsub = \frac{2VGS,M1(I1)C2}{I1+I2} I2 \qquad (1)$$

To keep the oscillator within the steady state, the charge obtained within the charging should be capable that subtracted within the discharging phase. For capacitance C1, the charging current and also the discharging ones are I1 and I2, severally. The charging time T1 and discharging time T2 are given as

$$T1 = \frac{\frac{2VGS,M1(I1)C2}{I1+I2} I2}{I1} \text{ and } T2 = \frac{\frac{2VGS,M1(I1)C2}{I1+I2} I2}{I2} \qquad (2)$$

Then, the oscillation period TOSC is expressed as

$$TOSC = \frac{2VGS,M1(I1)C2}{I1} \qquad (3)$$

Assume that C2 is completed by a metal–insulator–metal (MIM) capacitor, and its TC is extremely low. In line with (3), the TC of the oscillation frequency depends upon those of VGS,M1(I1) and I1. During this temporary, a digital compensation loop is employed to stabilize VGS,M1(I1) and a temperature-compensated current source I1 is adopted.

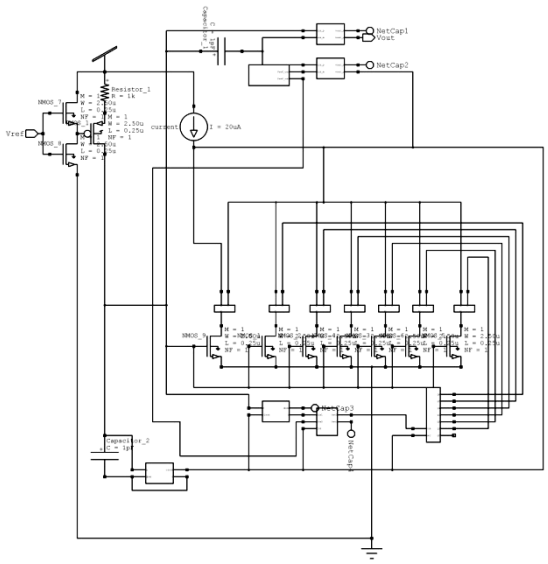

Fig -3: Relaxation oscillator using a digital compensation loop

2.1 Relaxation Oscillator with Temperature Compensation:

Fig. 3 shows the relaxation oscillator with the digital compensation loop. For an NMOS transistor biased within the sub threshold region with a hard and fast drain current, its gate–source voltage VGS[8] is given as

$$VGS(T)=\eta VT \ln(\frac{ID}{K\ I0})+VTH(T) \qquad (4)$$

Where I0 = μCOX(η − 1)V2 T , η is the sub threshold slope factor, VT is the thermal voltage, ID is the drain current, K (= W/L) is the aspect ratio of the transistor, μ is the carrier mobility, and COX is the gate–oxide capacitance. The threshold voltage VTH(T) is modeled as

$$VTH(T)=VTH(T0)+KT(T/T0-1) \qquad (5)$$

Where KT is the negative. Normally, VGS(T) may be a complementary to- absolute-temperature (CTAT) voltage since KT is dominant. To cut back the TC of VGS,M1(I1), the effective ratio of M1 is adjusted by using the digital compensation loop.

2.2 Robust ARM latch comparator:

Fig. 4 Strong ARM latch comparator may be a well-known topology. It has some vital options that creates it distinctive, like 1) It doesn't consume static power, 2)It produces rail-to-rail output, 3) It has small input referred offset and 4) It has high input impedance. These favorable options made up the means for the latch to be widely used as a way of sense amplifier, a comparator or a strong latch[2]. As a consequence, it is common to seek out the robust ARM latch in analog-to-digital converters (ADCs)[3] and Flip-Flops circuits[4]. With the increasing interest in wearable electronics, Internet-of-Things (IoT) and low power applications, the requirement for little,

quick and power-efficient electronics is usually present.

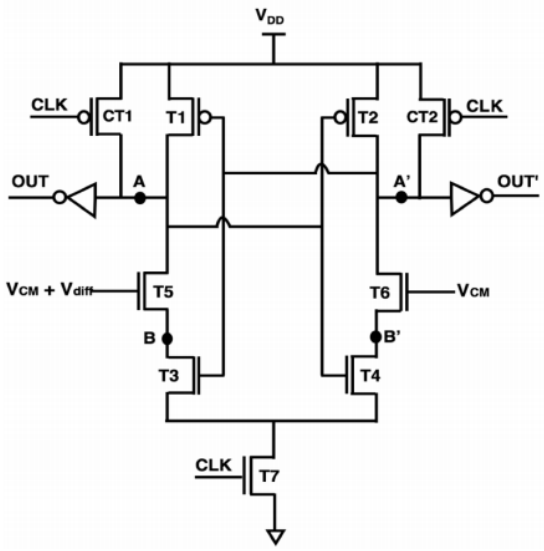

Fig -4: Robust ARM latch comparator design

The operation of the latch consists of 3 phases: Reset, Amplification, and Regeneration as illustrated in Fig 2. Reset phase starts once the CLK goes Low, and consequently the internal capacitors at the nodes A, A', B and B' to VDD through the CTs. Amplification phase starts once the CLK goes High, turning all CTs OFF and permitting the capacitors to discharge through T7. T5 and T6 are biased by a relentless common mode voltage (VCM), hence, these transistors are continuously ON. Once a little differential voltage (Vdiff) is present between the gates of T5 and T6, it causes a small difference between the current flowing through these 2 transistors. Consequently, the capacitors at nodes B and B' are discharged at slightly different speeds, therefore, the voltages at these nodes drop at different rates. T3 and T4 turn ON(active) once the voltages at nodes B and B' reach (VDD - Vthn). After that, the voltages at nodes A and A' begin to drop at different rates. Regeneration phase starts once the voltage at either A or A' drops to (VDD - Vthp) turning either T1 or T2 ON, and also the different transistor remains OFF due to the cross coupled configuration. As a result, the final voltages reach VDD in either node (A or A') and zero volts for the opposite node, depending on the polarity of Vdiff. The output is taken from nodes A and A', and fed into inverters.

2.3 Low Power Voltage References:

There are many approaches to coming up with voltage references in CMOS technology. The foremost common technique may be a band gap voltage reference using parasitic BJTs (bipolar junction transistors). To come up with a temperature insensitive output voltage, band gap references linearly mix 2 voltages with opposing temperature characteristics: a complementary-to-absolute-temperature (CTAT) voltage and a proportional-to-absolute-temperature (PTAT) voltage. Another technique combines PTAT and CTAT currents, instead of voltages, to come up with a temperature-independent output voltage. Voltage references also can be designed by employing 2 devices of various threshold voltages, which may be enforced by distinct gate doping or selective channel implantation. As an alternative, one can do a stable output voltage supported the finding that the weighted difference between gate-source voltages of 2 complementary metal-oxide silicon (CMOS) transistors is temperature insensitive. Another approach uses sub threshold-biased transistors to lower minimum partial supply voltage and power consumption. Finally, storing and refreshing a voltage at a floating node may be used to supply a reference voltage.

Fig. 5 The transistor M1 is biased within the sub-threshold region. The sub-threshold gate–source voltage VGS is nearly independent of the drain–source voltage VDS if the drain–source voltage VDS is larger than 4VT , where VT is the thermal voltage. Therefore, the reference voltage Vref,OSC ought to be on top of 4VT to form voltage VGS,M1(I1) independent of the signal V−. Voltage Vref,OSC also needs to be lower than voltage VGS,M1(I1) to confirm the comparator CMPOUT toggles. As long as the reference voltage Vref,OSC is higher than 4VT and lower than voltage VGS,M1(I1), it has negligible impact on the oscillation period.

The reference voltage Vref,cal can be expressed as

$$Vref,cal=\alpha 1 VGS,M5+\beta 1 VT \quad (6)$$

where VGS,M5 is the gate–source voltage of M5, α1 = (1 + (R4 + R5/R3))(R2/R1)(K8/K7) − (R4 + R5/R1)(K9/K7), β1 = (1+(R4 + R5/R3))ln((K11/K10)(K8/K9)), VT is the thermal voltage, and K is the aspect ratio. By properly selecting the coefficients α1 and β1, the TC of Vref,cal may be nulled out. The reference voltage Vref,cal is designed to be lower than the threshold voltage of the NMOS transistor to make sure that the transistor M1 and also the compensation circuit are biased within the sub-threshold region. The simulated Vref,cal is 444.5 mV, and its TC is 74.99 ppm/ ◦ C. The reference voltage Vref,OSC can be expressed as

$$Vref,OSC=\alpha 2 VGS,M5+\beta 2 VT \quad (7)$$

Where
α2=(1+(R4/R3))(R2/R1)(K8/K7)−(R4/R1)(K9/K7) and β2= (1 + (R4/R3))ln((K11/K10)(K8/K9)). Note that the TCs of those 2 reference voltages cannot be zero at the same time. The reference voltage Vref,OSC should be larger than 4VT to confirm VGS,M1(I1) independent of the drain–source voltage V−. Additionally, Vref,OSC needs to be lower than VGS,M1(I1) for the comparator CMPOUT to toggle. As long as VGS,M1(I1) > Vref,OSC > 4VT , it has a negligible impact on the oscillation period. The simulated Vref,OSC is 289.3 mV, and its TC is 152.66 ppm/ ◦ C.

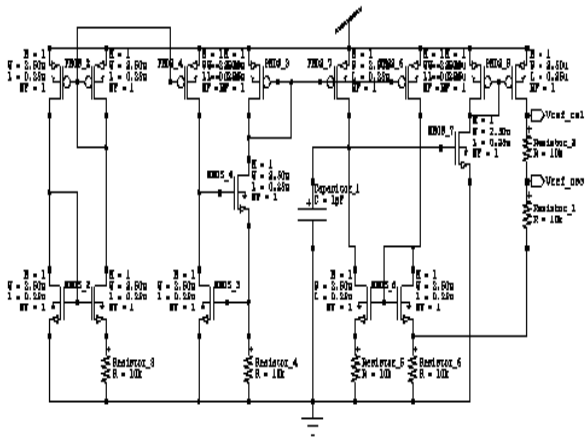

Fig -5: Low-power voltage reference

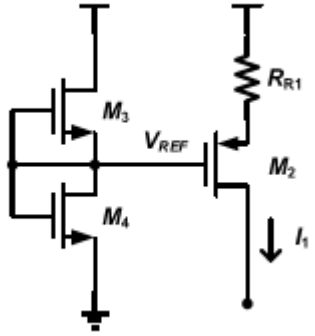

Fig -6: Current source

2.4 Current Source I1:

Fig. 6 shows the current source I1 of the oscillator. The current I1 can be derived as

$$I1=\frac{VDD-VREF-\left(\sqrt{\frac{2I1}{\mu pCox\left(\frac{W}{L}\right)2}}+|VTH2|\right)}{RR1} \quad (8)$$

Since the threshold voltage VTH of a MOSFET is CTAT[8], a PTAT voltage VREF[7], [10] is adopted. If VREF is a fixed voltage, the CTAT nature of M2's VTH would build I1 PTAT. The simulation results show that a rather PTAT resistance RR1[11] is needed to compensate the TC of the third term of the numerator in (8). Thus, the TC of the current I1 is decreased. The transistors M3 and M4 are biased within the sub threshold region. Voltage VREF can be expressed as

$$VREF=b.\ VT.\ \ln\left(\frac{\mu 3Cox3W3L4}{\mu 4Cox4W4L3}\right) \quad (9)$$

where b is a process-dependent quantity. The simulation results show that this current source consumes 32.4 μW at 25 ° C. The simulated phase noise at 1-kHz offset frequency is merely degraded by 0.11 dBc/Hz comparing with that using an ideal VREF. Thus, a two-transistor PTAT voltage reference[7], [10] is used. The current source I2 is realized similarly.

3. EXPERIMENTAL RESULT

The proposed relaxation oscillator is fabricated in a 45nm CMOS technology. When the supply is 0.6V, this oscillator consumes 86.07μW with the digital compensation loop which was shown in Fig. 7. Fig. 8 shows the oscillation frequency of the proposed oscillator which represents VOut and VRef. The measured average of oscillation frequency with and without compensation are 125 MHz obtained were shown in Fig. 9.

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Power Results
VVDD from time 0 to 1.5e-007
Average power consumed -> 8.607788e-005 watts
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Fig -7: Power results of Oscillator

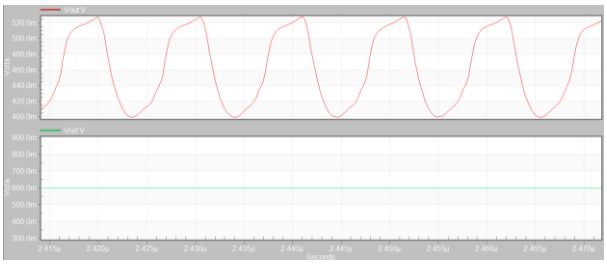

Fig -8: Oscillation frequencies of VOut and VRef

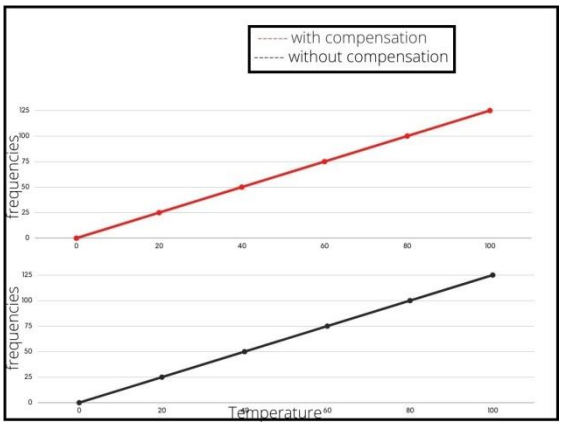

Fig -9: Measured oscillation frequencies for with and without compensation

Table: Comparisions

	Existing Work	**Proposed Work**
Technology (nm)	180	45
Area	0.117	0.022
Power (uW)	157.8	86.07
Supply (V)	1.2	0.6
Approach	Switched-Capacitor	Switched-Capacitor

The comparisions of existing and proposed works are shown in above table.

4. CONCLUSION

A low power and highly reliable 125-MHz relaxation oscillator using 45nm CMOS technology is presented. The proposed relaxation oscillator is used to decrease the area and power which are compared to existing work. The comparisions are done with existing work which are represented in table.

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