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Design of Low Noise CMOS Differential Amplifier using 180nm Technology

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Abstract – *This article presents the Low Noise CMOS Differential Amplifier design using 180nm technology. The analog circuit design includes favorable sets of restraints at the same time determining the effective design parameters value which in turn develops the performance of a circuit. The circuit with noise presence can affect its working by not providing exact information at the receiver end, therefore proper analysis is needed in achieving a sophisticated or well-functioning circuit. This Low Noise CMOS Differential Amplifier is used because of its properties like low noise figure, high gain and good reverse isolation as well as good stability. This paper presents a design of low noise CMOS differential amplifier with suitable compensatory circuit, along with this MOS transistor length and width is designed, by considering numerous specifications which is necessary for the circuit design. The design of LNA is simulated using Cadence virtuoso tool in 180nm technology and the results are shown by using Spectre simulator. The pre-simulation and post-simulation waveforms are obtained for Transient Analysis, AC Analysis and DC Analysis.*

Key Words: **Low Noise Differential Amplifier, Noise Figure, Cadence, virtuoso, Spectre, Gain.**

1. INTRODUCTION

The differential amplifier is one of the most effectively and efficiently used circuit in analog and mixed signal circuits. A Low Noise Differential Amplifier is the fundamental element in the Communication system as well as in Data Conversions circuits in terms of design, cost using 180nm Technology. Our project includes different techniques to explore the applications and implement of a low noise amplifier. The multiple properties like high gain, low noise, good matching of input and output and limitless stability are essentially important and that does not depend on each other's favor. Our project mainly focused to suppress the noise [1].

In a developed CMOS technique, the demanding part of design and advancement of the LNA are circuit linearity, decreasing supply voltage, low noise figure and high gain. The simple way to design a Low Noise Amplifier with cascode-stage is to amplify weak and noisy signals. The cascode is a two-stage amplifier that consists of a common-source stage feeding into a common gate stage. It is used to improve the performance of an analog circuit. [7].

Differential amplifier circuit receives only two input signals and amplifies the difference between those two input signals. The circuit mainly consists of NMOS and PMOS transistors where NMOS is used to form differential pair and PMOS is used as a current mirror active load (Compensatory circuit). Application are it amplifies a very low power signal without much reducing its signal to noise ratio and it also improves frequency responses and also helps to increase CMRR which further helps to avoid unwanted signal [3].

2. LITERATURE SURVEY

As mentioned in the Literature Survey Paper [1], has proposed a paper which explains the designing of LNA for front end frequency of radio. The design aims for low noise factor and high gain, which is performed in 180NM technology. The result is being simulated by using Spectre RF simulator. For targeted design of low noise amplifier, they have used, three stages which are input and output matching set-up and core amplifier. Input matching necessities are completed using inductor at gate of MOSFET. The designed Low noise amplifier gives a reliable voltage gain of about 28dB, good reverse isolation of -70dB, maintains a good stability and noise figure of 0.7dB.

As mentioned in the Literature Survey Paper [3], has proposed a paper that involves the designing of LNA with compensatory circuit using automated design methodology for minimum circuit area. The paper uses HPSO nature inspired heuristic optimization algorithm that gives acceptable approximate solution within the time. They have used Matlab and Cadence tool where both are connected to bring about the design using 180micrometer technology. The proposed design has better efficiency and takes less time as compared to other HPSO based design method.

As mentioned in the Literature Survey Paper [5], has proposed a paper that deals with the designing of an amplifier array with neural recording which has ultra-power and low noise which is best suited for large scale integration. The design consists of supply sensitive single ended first stage and differential second stage. The design takes up 2.85 microampere per channel from 1v supply. The proposed design is accomplished using 90nm CMOS technology. The design has low input noise of 3.04microvolts.

As mentioned in the Literature Survey Paper [7], presents a paper that analyses low noise amplifier with 45NM technology that focuses on less power consumption and high

gain. The design consists of common gate amplifier in the input stage, common drain amplifier at the output stage and an active inductor. It uses 12 transistors for reducing parasitic effect and reduced power consumption, the output gain is of 13.63dB and bandwidth of 10.71 KHz.

As mentioned in the Literature Survey Paper [10], proposed a paper that focuses on balanced differential amplifier which is Complementary metal oxide semiconductor based with MOS loads. In the paper they have used active loads with are diode connected and current source for balanced differential amplifier. The proposed paper uses 0.25micrometer CMOS technology. The CMRR for differential amplifier with diode connected load is found to be 40.56dB, with current source load it is found to be 34.87dB and with the combination of both it is found to be 51.67dB.

3. WORKING

A Low Noise Differential Amplifier (LNA) is one of the most used part in designing of receiver and it plays a vital role in millimeter wave application such as Remote Sensing, Radio Astronomy, trans-receivers and in satellite communication.

A LNA provides trade-off between gain and noise figure. A good signal to noise ratio (low noise figure) and high gain is the main requirement for the better working of LNA. The efficiency determination of LAN is necessary to analyze parameter such as linearity, high gain, noise figure and stability and matching of input and output in the circuit.

4. BLOCK DIAGRAM

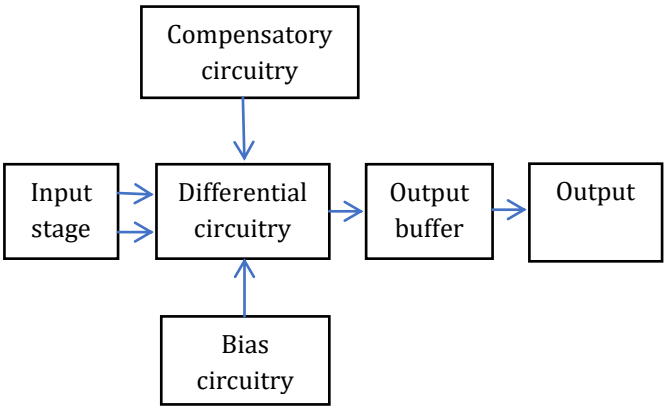

Fig -1: Block Diagram of Differential Amplifier

A Differential Low Noise Amplifier amplifies the difference between the two inputs, it provides common-mode rejection as it eliminates noise which is common to both input signals.

Designing of an analog circuit involves selection of enhanced dimension of transistor which gives an outcome of good performance in desired circuit specifications. To obtain the improved working of a circuit, the parameters used in the design are calculated under different set of conditions. In this project, we are going to design a Low Noise CMOS Differential Amplifier with current mirror load acts as compensatory circuit. Current mirrors are current source that uses the principle that if the gate-source potentials of two uniform CMOS transistors are equal, then the currents in the channel should be equal.

The Differential Low Noise Amplifier has a pair of MOSFET which forms differential circuitry which receives two signals as input and amplifies the difference of the signal by gain Av. Another pair of MOSFET is used to form current mirror active load and a single MOSFET is used for biasing.

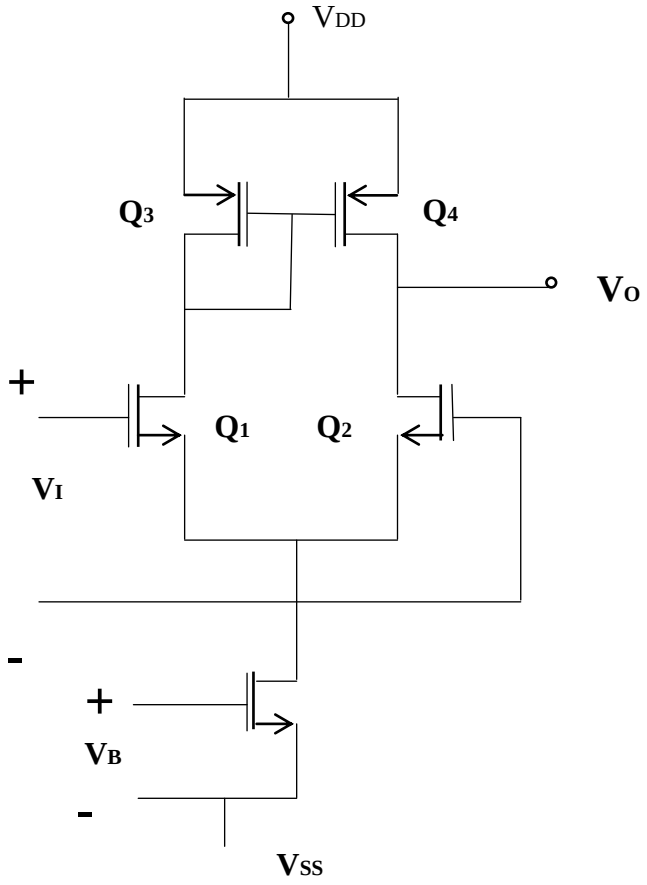

Fig -2: Differential Amplifier with current mirror load

5. FLOW CHART

The flow chart shows sequence of steps in which our project is going to be executed. We will initiate the project by collecting the specification data required for the design of LNA such as small signal gain, ICMR, Slew rate and so on.

Then we start making a schematic of LNA, which is in our project is a current mirror load LNA then we start determining the (W/L) ratio of CMOS transistors to achieve the given set of constraints, hence optimizing the length and width of MOS transistors.

Then the schematic capture with optimized length and width is simulated using cadence tool using 180nm technology. If simulation yields expected results, we move on to next step that is layout formation of LNA, else we iterate again from implementation step until we get expected result. If anything goes wrong in layout we iterate the steps from schematic capture, else the layout is given for fabrication to get LNA of desired specification.

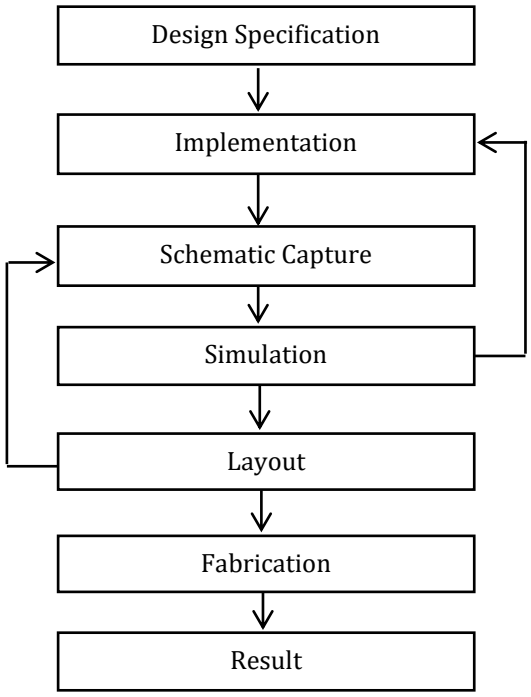

Fig -3: VLSI Design Flow Chart

6. DESIGNING PROCEDURE

In the design of CMOS circuit, it is significant to identify the suitable relation that connects the design specification to its parameters. The design includes two types of details. The first type is designing of different parameters namely power supply, technology, and the temperature. The other type of information is specifications.

The design specifications for the differential amplifier consists of small-signal gain (Av), frequency response of load capacitance (w-3db), input common-mode range (ICMR) or maximum input common-mode voltage [VIC(max)], minimum input common-mode voltage [VIC(min)], slew rate (SR) and power dissipation (Pdiss).

- Small signal voltage gain

  AV = gm. Rout (1)

  Where gm can be calculated by,

  $gm = \sqrt{2\mu nCox\left(\frac{W}{L}\right)Ibias}$ (2)

  $Cox = \frac{\epsilon ox}{tox}$ (3)

- Slew rate (SR), Calculation of I5

  SR = I5/CL (4)

- Frequency response (ω-3dB), Calculation of Rout

  ω-3dB = 1/Rout.CL (5)

- Upper ICMR (VIC(max), Calculation of (W/L)3

  VIC(max) = VDD - VSG3 + VTN1 (6)

  (W/L)3 = 2I5/K'P (VSG3 + VTP) (7)

- Lower ICMR (VIC(min), Calculation of (W/L)5

  VIC(min) = VSS - VDS5(sat) + VGS1 (8)

  (W/L)5 = 2I5/K'N V^2DS5(sat) (9)

- Power dissipation (Pdiss)

  Pdiss = (VDD + |VSS|). (I5) (10)

- The design procedure involves the assumption of small signal voltage gain Av, the -3dB frequency (ω-3dB), lower common mode voltage [VIC(min)], upper common mode voltage [VIC(max)], Slew Rate (SR), power dissipation (Pdiss) are given.

- Select I5 that satisfy the slew rate with the known values of CL or Pdiss.

- Frequency response can be calculated using Rout, if it is not satisfied then check for I5 or modify the topology.

- Select (W/L)3 and (W/L)4 ratio which satisfies upper ICMR.

- Select (W/L)1 and (W/L)2 ratito which satisfies small signal voltage gain Av.

- Select (W/L)5 ratio to satisfy lower ICMR.

- Repeat the step anywhere that is essential to meet requirement.

7. SIMULATION AND ANALYSIS

There are three types of analysis done basically to know the performance of the circuit. They are:

- Transient Analysis
- DC Analysis

- AC Analysis

This analysis is the most fundamentals of device and circuit analysis. While designing of an analog circuit, checking bias condition that is DC analysis is important. This tells what would happen when circuit is turned on and no signal is applied to it. AC analysis is done basically to figure out the circuit frequency response. It helps to analyze the circuit when AC signal is applied to its input. Then transient analysis is used to identify the circuit behavior under non-well-behaved signals.

8. APPLICATIONS

- Used in RF Receiver.
- Wireless Communication System.
- Biomedical Applications.
- Used in automatic gain-controlled circuit.

9. ADVANTAGES

- Improves frequency responses.
- It amplifies a very low power signal without much reducing its SNR.
- Helps to increase CMRR which further helps to avoid unwanted signal.

10. CONCLUSIONS

Low Noise Differential Amplifier has been developed for the required Signal to Noise ratio with desired Noise Figure, and high Gain with a low power consumption of about 1.8-2.8V is applied. The design of LNA is analyzed and simulated using Cadence 180nm CMOS Technology successfully with the desired specifications. It can be used for different applications to obtain low noise at their output.

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