Design of Single Phase Half- Height Neutral Point Clamped Multilevel Inverter with Reduced Number of Components and Optimum THD Performance

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Abstract - *This paper presents, a design of single phase Half-height neutral point clamped (NPC) multilevel inverter with optimum total harmonic distortion (THD). The offered inverter topology is explained with the help of a single phase eleven-level inverter. Compared to traditional topologies such as a cascaded H-bridge converter, Diode Clamped converter, Flying Capacitor converter and NPC converter, the proposed inverter consists of a single dc voltage source, a single phase full bridge cell, switching devices and power diodes half in number. Due to the less number in switching devices the conduction losses will decreases, there by efficiency improves, and also the size and weight of the multilevel inverter are decreases. The switching signals were generated using Equal Phase (EP), Half Equal Phase (HEP), Feed Forward (FF) and Half Height (HH) methods. The proposed single phase inverter has been simulated through MATLAB/Simulink.*

Key Words: Multilevel inverter1, Half-height NPC inverter2, total harmonic distortion (THD)3, EP4, HEP5, FF6 and HH7

1. INTRODUCTION

A multilevel inverter is a device which consists of multiple components such as switching elements and voltage sources, which provides high voltages with low THD [1]. The conventional two-level inverter provides high switching losses, EMI and high dv/dt stress, high level of THD in high power and medium voltage applications [2]. Due to these difficulties the multilevel inverter was proposed in 1975 [3]. In the case of multilevel inverters, an interesting aspect is that renewable energy sources can be conveniently interconnected; electric cars, batteries and capacitors can be plugged in [4].The concept of multilevel converters introduces utilization of a higher number of semiconductor switches to perform the power conversion in small voltage steps resulting primary advantage of high power quality, better electromagnetic compatibility, lower harmonic components, and lower switching losses [5].

In the last few years, multilevel inverters have become more popular because they offer more advantages than the traditional two level inverters. In the last three decades, there are different topologies which were proposed, aiming to produce a sinusoidal waveform. The multilevel inverter was started with the 3- level and now it has been promoted to N number of levels. Normally, there are four different kinds of multilevel inverter topologies. They are (a) Cascaded H-bridges converter (CHB) (b) Diode clamped (DC) converter (c) Flying capacitors (FC) converter and (d) Neutral point clamped (NPC) converter [6]. The disadvantage of CHB topology is that, it requires more number of separate voltage sources to supply each cell. This problem in CHB was chased by the DC converter that uses a bank of series capacitors [7]. This topology has several attractive and indifferent characteristics comparing to the DC inverter. The additional clamping diodes are not required for FC converter. Moreover, the flying capacitor inverter has switching luxuriance within the phase that can be used to balance the flying capacitors and to require only one dc source [8]. It does not require additional clamping diodes and provides redundant switch states that can be used to control the capacitor charge even under loads with the dc level [9]. However, larger structures require a relatively high number of capacitors, and additional circuits are also required to initialize the capacitor charge.

However, the multilevel concept has mainly been proposed to generate an AC voltage using small DC voltage levels with better THD performances and lower losses. THD mainly depends on the degree of the level of the inverter and controlling scheme of the switching devices. But for existing topologies, the inverter turns into massive shape and complex structure [10]. The conventional topologies require a huge number of switching devices, power diodes, dc voltage sources and auxiliary capacitors to increase the level of the output voltage. As a result the size and weight of the inverter, conduction losses increase. In recent years, several topologies with reduced number of switches and sources have been proposed in [11], [12].

In this paper, a new topology of multilevel inverter has been proposed with reduced number of components, which make the inverter smaller in size, light in weight. It also reduces the losses and increases the efficiency. The proposed inverter involves half of the number of components as compared to the NPC topology to generate equal number of voltage levels. Hence it can be named as half-height NPC inverter.

In this paper, the Switching angles which are given to the IGBTs are calculated by using the following methods [13].

1. Equal Phase (EP) Method.

2. Half Equal Phase (HEP) Method.
3. Half Height (HH) Method.
4. Feed Forward (FF) Method.

2. PROPOSED INVERTER TOPOLOGY

The proposed inverter topology is introduced in this section. The working principle of the inverter is explained with the help of a single-phase 11-level inverter.

2.1 Generalized Configuration of Inverter

The generalized circuit of the single-phase proposed topology is shown in Fig. 1. This inverter requires only one DC voltage source as shown in Fig. 1. This dc voltage is divided into *m* numbers of small dc voltage levels using dc bus capacitors, where *m* represents the number of output voltage level. A full bridge cell with the load is also part of the generalized topology.

Hence, the number of dc bus capacitors required for *m*-level inverter is,

$$N_C = (m-1)/2 \quad \ldots\ldots(1)$$

The number of switches needed for *m*-level inverter is,

N_S m 7)/2……(2)
The number of power diodes needed for *m*-level inverter is,

$$N_D \approx (m-3)/2 \quad \ldots\ldots(3)$$

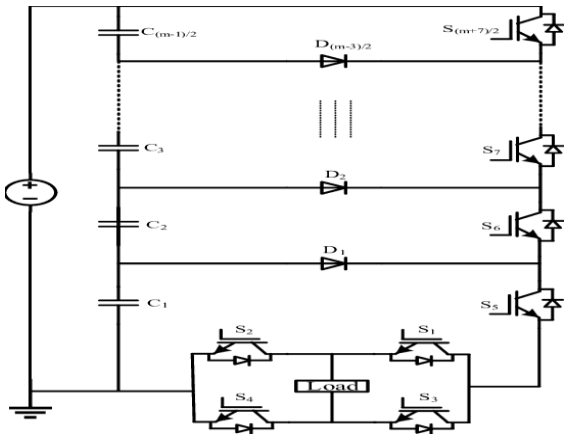


Fig -1: Generalized circuit of the single-phase proposed topology

2.2 Methods for Generation of Switching Signals

Several methods have been proposed to calculate the switching angles which are given to IGBTs. In this paper four methods were considered to generate the switching angles. The Switching angle is the angle at which the voltage level changes at the output. The m-level waveform is as shown in Fig. 2. It has 2(m-1) switching angles namely, α_1, α_2, α_3..., α_{m-2}, α_{m-1}. Since the sine wave is a symmetrical waveform, the negative half cycle is symmetrical to its positive half cycle. And the waveform of the second quarter period is mirror image to the waveform of its first quarter period. So we call the switching angles in the first quadrant period as main switching angles.

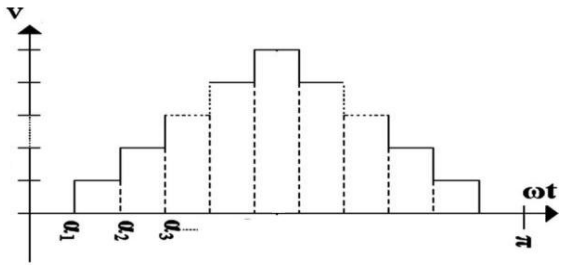


Fig -2: m-level output waveform

Main Switching Angles in the first quarter of the sine wave (i.e., 0^0 to 90^0) are:

$$\alpha_1, \alpha_2, \alpha_3 \ldots \alpha_{(m-1)/2} \quad \ldots\ldots(4)$$

The switching angles in the second quarter of the sine wave (i.e., 90^0 to 180^0) are given by,

$$\alpha_{(m+1)/2} = \Pi - \alpha_{(m-1)/2}, \Pi - \alpha_{(m-2)/2}, \ldots\ldots \Pi - \alpha_1 \ldots\ldots(5)$$

The switching angles in third quadrant of the sine wave (i.e., 180^0 to 270^0) are given by,

$$\alpha_m = \Pi + \alpha_1, \ldots\ldots, \Pi + \alpha_{(m-1)/2} \ldots\ldots(6)$$

The switching angles in the fourth quadrant (i.e., 270^0 to 360^0) are given by,

$$\alpha_{(3m-1)/2} = 2\Pi - \alpha_{(m-1)/2}, \ldots\ldots, 2\Pi - \alpha_1 \ldots\ldots(7)$$

It was found from the above equations that we only need to evaluate the main switching angles (i.e. from 0^0 to 90^0), other switching angles (i.e. from 90^0 to 360^0) can be derived from the main switching angles in the first quadrant. In section III, the output voltage waveforms and current waveforms with the frequency spectrums of 11-level, 21-level, 29- level and 37-level inverter have been presented to know the best method out of four methods that provides the optimum THD.

The main switching angles are determined from the following methods.

2.2.1 Equal Phase Method

In this method the switching angles are distributed averagely in the range 0-Π. The main switching angles are determined by the equation *(8)*,

$$\alpha_i = i * 180^0/m; \text{ where } i=1, 2, \ldots, (m-1)/2 \ldots\ldots (8)$$

2.2.2 Half Equal Phase Method

The waveform obtained from the EP method looks like a triangle waveform, so to get some better output waveform, another method called [13] HEP is established. The main switching angles are in the range 0^0-90^0, which are obtained by the equation *(9)*,

$\alpha_i = i * 180^0/(m+1)$; where i=1, 2,..., (m-1)/2.....(9)

2.2.3 Half Height Method

In the above two methods the waveforms obtained were not a sine wave shape. According to the sine function a new method called [13] HH was established to determine new switching angles. The main switching angles are obtained by the equation *(10)*,

$$\alpha_i = \sin^{-1}\frac{(2i-1)}{m-1} \quad ; \quad \text{where i=1, 2....,(m-1)/2.....(10)}$$

2.2.4 Feed Forward Method

In the above three methods, we can observe that there are wider gaps between the positive and negative half-cycles. In order to reduce those gaps, another approach called the [13] FF was established to find the main switching angles. The main switching angles are determined by,

$$\alpha_i = \frac{1}{2}\sin^{-1}\frac{(2i-1)}{(m-1)} \text{ ; where i=1, 2,..., (m-1)/2.....(11)}$$

2.3 Operating principle of the proposed topology

The operating principle of the proposed inverter is described here with the help of 11-level inverter. By connecting the dc bus capacitors with the dc voltage source in series, the input dc voltage is divided into five small dc voltage levels. The generalized formula for the determination of each output voltage level of the inverter is,

$$Vk = (2kVDC)/(m-1).....(12)$$

Where, *VDC* is the DC source voltage and $k = 0, \pm1, \pm2,...\pm(m-1)/2$. The individual output voltage level with corresponding switching state is summarized in Table I. Table 1 shows the operation of 11-level proposed inverter.

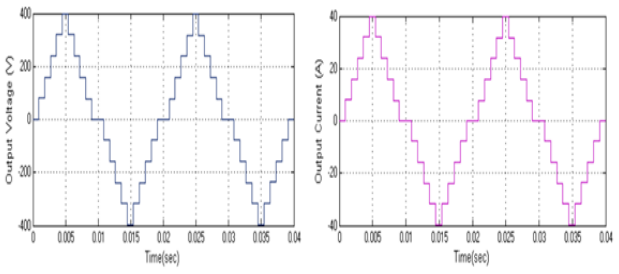
TABLE –1: Switching states with corresponding voltage levels

Output Voltage	Switching states								
	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9
$V_5=V_{DC}$	ON	OFF	OFF	ON	ON	ON	ON	ON	ON
$V_4=4V_{DC}/5$	ON	OFF	OFF	ON	ON	ON	ON	ON	OFF
$V_3=3V_{DC}/5$	ON	OFF	OFF	ON	ON	ON	ON	OFF	OFF
$V_2=2V_{DC}/5$	ON	OFF	OFF	ON	ON	ON	OFF	OFF	OFF
$V_1=V_{DC}/5$	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
$V_0=0$	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
$V_{-1}=-V_{DC}/5$	OFF	ON	ON	OFF	ON	OFF	OFF	OFF	OFF
$V_{-2}=-2V_{DC}/5$	OFF	ON	ON	OFF	ON	ON	OFF	OFF	OFF
$V_{-3}=-3V_{DC}/5$	OFF	ON	ON	OFF	ON	ON	ON	OFF	OFF
$V_{-4}=-4V_{DC}/5$	OFF	ON	ON	OFF	ON	ON	ON	ON	OFF
$V_{-5}=-V_{DC}$	OFF	ON	ON	OFF	ON	ON	ON	ON	ON

During the positive half cycle, *S1* and *S4* switches are always ON state; and, *S2* and *S3* switches are OFF state. Hence, output voltage is taken into account as positive. During the negative half cycle, *S2* and *S3* switches are always ON state; and *S1* and *S4* are OFF state. So, the output voltage is negative. By applying gate triggering signals to the remaining switches, small dc voltage levels are generated.

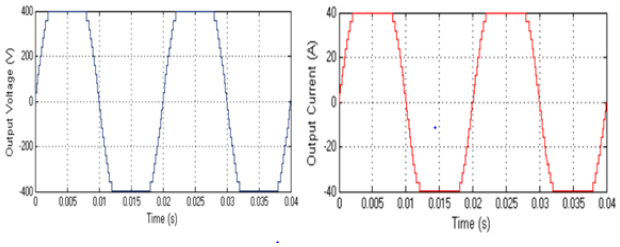
3. PERFORMANCE ANALYSIS OF THE PROPOSED INVERTER

In order to analyze the performance of the proposed inverter, four different levels including 11-level, 21-level, 29-level and 37-level inverters have been simulated with MATLAB/Simulink software. The value of the dc voltage source is considered as 400V. The value of the switching frequency fs is used as 10 kHz. In Fig. 3, Fig. 4, Fig. 5 and Fig. 6 the simulated waveforms of output voltage and current for 11, 21, 29 and 37 level inverters are presented. From the Fig. 3, Fig. 4, Fig. 5 and Fig. 6 we can observe that with the increase of the output voltage level, the output voltage waveform progresses to pure sine wave. That is the 37-level inverter shows the best output waveforms among those four particular level inverters.



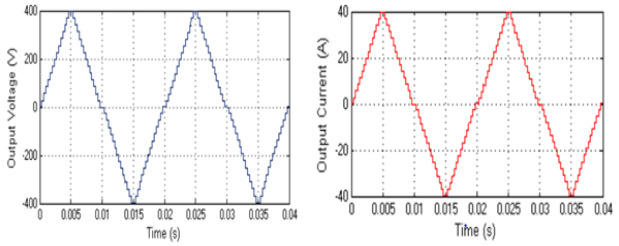
(a) (b)

Fig -3: The output waveforms of 11-level inverter by EP method (a) Output voltage, (b) Output current



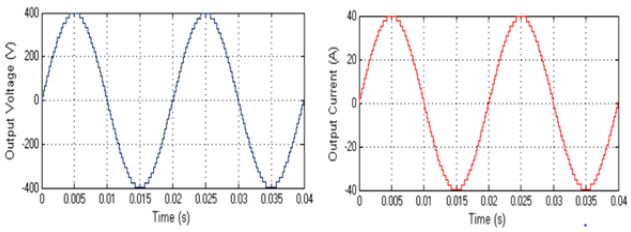
(a) (b)

Fig -4: The output waveforms of 21-level inverter by FF method (a) Output voltage, (b) Output current



(a) (b)

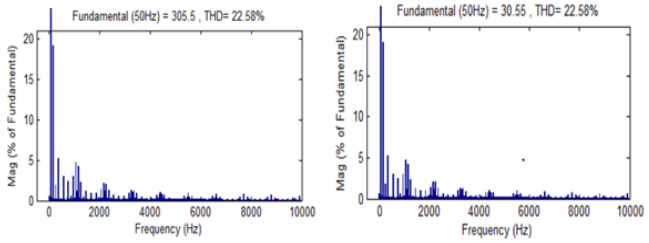
Fig -5: The output waveforms of 29-level inverter by HEP method (a) Output voltage, (b) Output current



(a) (b)

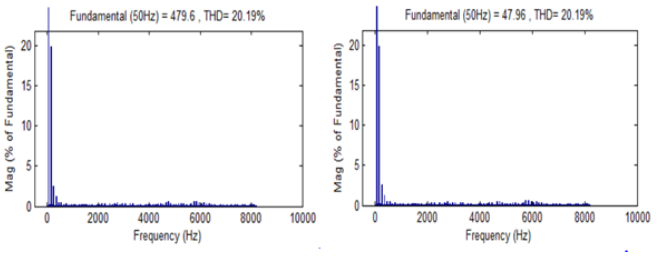
Fig -6: The output waveforms of 37-level inverter by HH method (a) Output voltage, (b) Output current

The harmonic spectrums of the output voltage and current waveforms of 11, 21, 29 and 37-level inverters are shown in Fig. 7, Fig. 8, Fig. 9 and Fig. 10. From these figures, it is observed that the value of the THD decreases as the level of the output voltage increases. Furthermore, the offered inverter topology provides better THD performance than the existing topologies for same number of level. In 21-level inverter, the CHB, DC, FC, NPC and proposed inverters provide 7.70%, 7.58%, 7.28%, 7.07% and 4% THD respectively and in 29-level inverter THDs are 6.57%, 6.37%, 6.14%, 5.95% and 2.92% respectively. Finally, in 37-level inverter 5.05%, 4.89%, 4.72%, 4.47% and 2.32% THDs are provided by CHB, DC, FC, NPC and proposed inverters respectively. Hence the presented scheme leads to lower losses and higher efficiency.



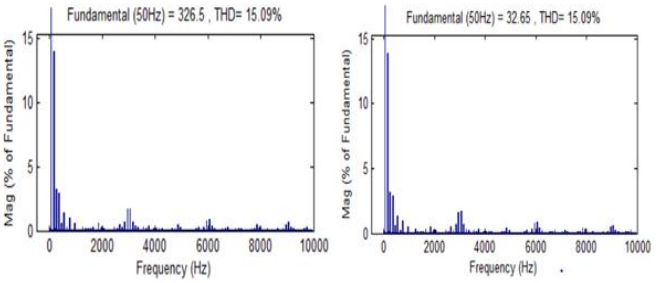
(a) (b)

Fig -7: Harmonic spectrums of 11-level inverter by EP method (a) Output voltage, (b) output current



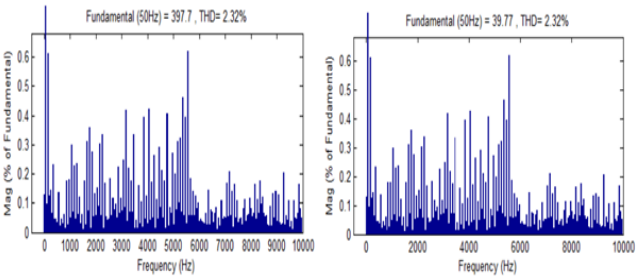
(a) (b)

Fig. 8 Harmonic spectrums of 21-level inverter by FF method (a) output voltage, (b) output current



(a) (b)

Fig. 9 Harmonic spectrums of 29-level inverter by HEP method (a) output voltage, (b) output current



(a) (b)

Fig. 10 Harmonic spectrums of 37-level inverter by HH method (a) output voltage, (b) output current

4. COMPARISON WITH EXISTING TOPOLOGIES

TABLE -2: Comparison between the proposed topology by HH method and existing topologies

Level	Parameters	CHB	DC	FC	NPC	**Proposed**
21	No. of Sources	10	1	1	1	**1**
	No. of Switches	40	40	40	40	**14**
	No. of power diodes	-	380	-	38	**9**
	No. of capacitors	-	20	380	20	**10**
	THD (%)	7.70	7.58	7.28	7.07	**3.93**
29	No. of Sources	14	1	1	1	**1**
	No. of Switches	56	56	56	56	**18**
	No. of power diodes	-	756	-	54	**13**
	No. of capacitors	-	28	756	28	**14**

	THD (%)	6.57	6.37	6.14	5.95	**2.87**
37	No. of Sources	18	1	1	1	**1**
	No. of Switches	72	72	72	72	**22**
	No. of power diodes	-	1260	-	70	**17**
	No. of capacitors	-	36	1260	36	**18**
	THD (%)	5.05	4.89	4.72	4.47	**2.25**

All the existing topologies require a large number of components including switches, power diodes, dc voltage sources and dc bus capacitors. For example, 18 and 22 switches are needed to design 29-level and 37-level proposed inverter whereas 56 and 72 switches are required for all the existing topologies to design 29-level and 37-level inverters. Again, the number of power diodes required for DC topology in 37- level inverter is 1260 whereas 17 power diodes are needed in proposed 37-level inverter. For a 37-level FC inverter, 1260 auxiliary capacitors are required, but only 18 dc bus capacitors are needed in the proposed 37-level inverter. Due to this reason, the sizes of the existing inverter topologies become bigger and the weight of the inverter increases. Because of the large number of switches, the switching losses and the conduction losses increase, as a consequence efficiency decreases.

Hence, considering all of the issues, the proposed inverter is designed with lower number of switches, power diodes, dc bus capacitors and a single DC voltage source. Thus, the size of the proposed inverter becomes smaller and the weight becomes lighter. As a consequence, losses are minimized and productivity improves. The proposed inverter also shows optimum THD performance as compared to existing topologies. Table 2 represents the comparison in performance between the proposed topology and existing topologies. It is concluded from Table 2 that the proposed topology shows better performances than the existing topologies.

5. CONCLUSION

In this paper, a multilevel inverter topology is proposed and also EP, HEP, HH and FF methods have been proposed to calculate switching angles for Half-Height Neutral Point Clamped multilevel inverter. By observing Table 3, we concluded that by Half-Height method we can obtain better harmonic spectrum compared to other three methods, because the output waveform obtained by HH method is nearer to the sinusoidal. The presented multilevel inverter has advantages: (i) it requires lower number of switching devices, (ii) the size of the inverter is smaller and is light in weight, (iii) it offers higher efficiency and lower losses, (iv) it shows optimum THD performance. Hence, the proposed inverter is suitable for medium and high voltage applications. In the future, three-phase multilevel inverter can be designed by using the concept of this topology.

TABLE -3: THD CAMPARISION TABLE

Type of Method	THD (%)
Equal Phase method	14.71
Half Equal Phase method	14.49
Feed Forward method	20.14
Half Height method	2.32

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