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Quantum-Dot Cellular Automata based Design of Flip-Flops and Shift Register

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Abstract – *As the component measurements diminishing in the present-day technology the basic CMOS technology faces severe problems due to the physical limitations of the day to day situations. Such as effects of short channel, more power dissipation, current leakage and the effects of short channel at the region of nano scale. Quantum-dot Cellular Automata (QCA) is a substitute for the challenging experience that gives a completely alternative measuring process to design the digital circuits by means of quantum dot technology. This process will productively process and transmits the data at the nano scale region as a better competitor for the standard CMOS technology. This paper illustrates the implementation of the flip-flop circuits such as SR flip-flop, JK flip-flop, T flip-flop and D flip-flop. The parallel input parallel output shift register is also demonstrated by using the D flip-flop.*

Key Words*:* Quantum-dot Cellular Automata, Majority gate, CMOS logic, Flip-Flop circuit, Polarization inputs

1. INTRODUCTION

In relation to Moore's rule, the size of the chip will diminish as the year [1]. The observation of Moore's law becomes right in VLSI circuit design based on CMOS. Yet now, in wide nano-meter technology, CMOS based VLSI technology has a scaling restriction. To bypass the VLSI circuit design's physical limitation based on MOSFET, such as tunneling currents, quantum effects, sub-threshold leakage, manufacturing expense, interconnect latency, a new technology was found by researchers that uses both the cellular automata and the quantum mechanics. A QCA (Quantum-dot Cellular Automata) is the perfect alternative for the CMOS based VLSI technology. It was a new form of criterion of computation that work at the level of quantum.

In 1993, Lent et al introduced physical automation by using the cells of Quantum-dot QCA Cell was first developed in 1997 [2]. The QCA has a tiny cell of two free electrons, holding four quantum dots. The quantum dots are linked through tunneling barriers and also the electrons were able to travel between the quantum dots through the barrier. The cell size can be within a range of nanometers [3]. Hence, the area which the circuit of QCA occupies will become exceptionally small. And the cell's switching speed is extremely fast. Hence the QCA device speed is nearly small. There the binary values which are stored in the cell's state of polarization, which is the cell's charging configuration, not with the current switches[4]. That means the QCA device's power consumption is comparatively low. Digital electronic circuits which are divided into two major categories. They are sequential and combinational circuits. The circuits are both implemented in the QCA technology. The combinational circuits which are realized precisely in the QCA with the similar functions of Boolean logic functions are used in traditional CMOS circuits [5].

The digital electronics production environment has remodeled over the last few years because of the rapid growth of technology. Co-founder of Intel company Gordon Moore estimated in 1960 that in every eighteen months, the single chip transistors would double. The traditional CMOS logic-based devices have been progressed from micron to submicron range, submicron to deep submicron range, and nano-meter scheme in the last five decades, according to his estimate[6]. But again, the scaling of nano scale CMOS devices affects the efficiency of several variables, such as leakage currents and heat dissipation.

The created heat will no longer dissipate and leads to chip damage but as most of the devices are loaded into same area. So, there are many creative technologies and resources to replace traditional VLSI technology that is based on transistors have been deeply developed and researched at nano scale [7]. QCA is a creative favorable transistor with less quantity paradigm which performs processing data and routing data in the nano- meter range domain, among many other alternatives. QCA 's special attribute is that one cell reflects logic states. A cell is a device of a nano-meter range scale which is capable of transmitting data across two combinations of state electrons. QCA 's advantages over traditional CMOS technology comprise less delay, ow power consumption and high-density structures allowing us to conduct quantum computing mostly in coming years.

2. QCA REVIEW AND MAJORITY GATE BASICS

Quantum Dot Cellular Automata are theoretical quantum computing models. Von Neumann introduced the cellular automata. The standard design of QCA solid state cells considers the spacing among the quantum dots have to been about 20 nm and is of a distance about 60 nm between cells. Like some CA, QCA is built on the basic rules of interrelationship between the cells arranged on the grid. A square patterned QCA cell is fabricated using four no. of quantum dots. Such quantum dots were electrons that can occupy sites by tunneling to them [8]. The design of effective sequential and combinational circuits at nanoscale is a new

technology. Compared to the CMOS technology, this technology has many beneficial features viz. reduced power consumption, slighter region of occupation and low latency. Such characteristics make it ideal for flip flop design and also for the counter design [9].

Clocking function is used in conventional VLSI technology is to restrict the timing of the sequential digital circuits. In QCA based technology, both sequential and combinational designs ultimately involve a pipeline-based clock system. This mechanism also regulates the flow of data but also provides the cells with power. Four clocks are added for the clocking function, i.e. clock signal 0, clock signal 1, clock signal 2, and clock signal 3. Those clocks are as evident in Fig. as 90 ° out of phase. Right now [10]. Each QCA clock consists of four various stages in the clock: switch, hold, release and relax as seen in the Fig.1 In the operation of switch mode, polarized cells initiate, and inter-base dot barriers get raised, and QCA based cell observes several of the no. of polarization states based on the driving cell 's condition. Real computation arises during this process. Cells have a fixed polarization mostly during hold process to drive the successor stage. In the release mode process, cells begin unpolarized cell and inter-dot barriers remain low as during final stage and the cell has no constant polarizations.

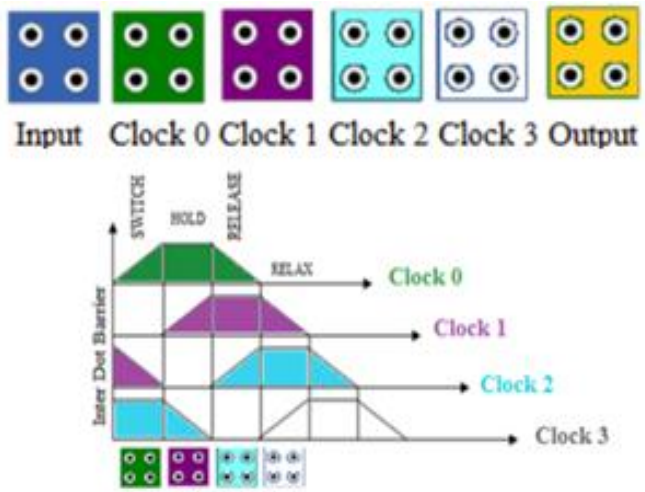

Fig -1: Four phases of QCA clocking

Majority gate:

The basic majority gate design contains a minimum of 5 QCA cells to reflect it. 4 of them are in four separate directions allowing them at the 90 ° angle by the nearby adjacent cells of the substrate material and one cell is shown in the Fig. 2 in the center of them. The logical Boolean expression that is to explain the function of majority gate is –

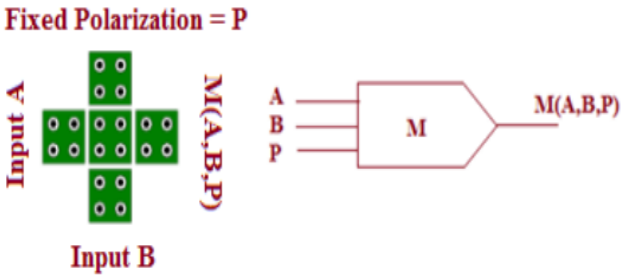

Fig -2: QCA Majority Gate

3. IMPLEMENTATION OF THE PROPOSED DESIGNS

A simple NAND gate-based SR flip-flop circuit gives feedback through to its opposite inputs from each of its outputs and is typically seen in storage circuits to save a single bit data information. Therefore, SR flip-flop circuit basically has 3 i/p's, set input, Reset input and its current output signal Q relevant to the current state or history thereof. The best thing to make a simple SR flip-flop with single bit set-reset input is to attach a set of 2-input NAND gates that are cross coupled, to build a Set-Reset based Bi-stable often described as an active LOW signal SR NAND Gate based Latch. The proposed majority gate structure of the SR flip-flop is shown in the Fig. 3. The characteristic table of the flip-flop circuit is shown in the table.1. The proposed structure layout which was shown in Fig.4 has 38 cells that forms a SR flip-flop. The proposed design includes clock input, S input, R input, two fixed positive polarization inputs and two fixed negative polarization inputs. And two output cells Q and Qb.

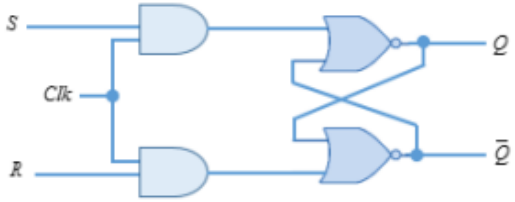

Fig -3: Proposed style of SR flip-flop majority gate structure

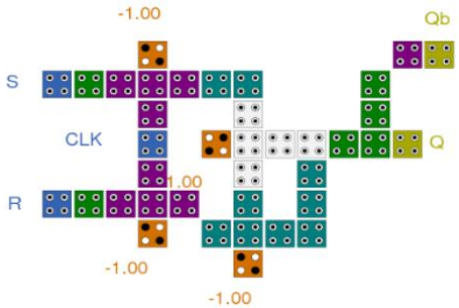

Fig -4: Proposed layout design of the SR flip-flop

Table -1: Characteristic Table of SR flip-flop

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	X

A JK flip-flop circuit is a flip-flop variant of SR. The main difference would be that the middle stage is more structured and reliable than the SR flip-flop circuit. Input signal J and input signal K behave in the same way as same as the SR flip-flop input signals S and R [11][12]. The letter J stands for SET, and the letter K stands for CLEAR. The JK flip-flop block diagram is shown in Fig, using SR flip-flop circuit. The proposed majority gate structure of the JK flip-flop is shown in the Fig. 5. The characteristic table of the flip-flop circuit is shown in the table.2. The proposed JK flip flop circuit layout is a simplified version for the existing JK flip-flop which is presented in the Fig.6. It contains 55 cells which are designed as a JK flip-flop. This design has the rotated and the translated cell.

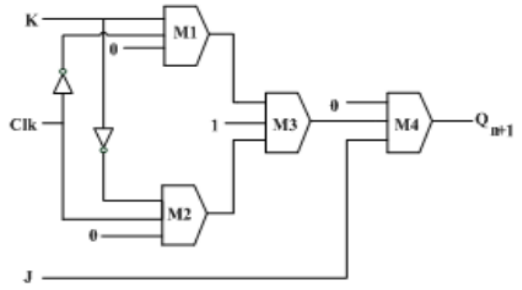

Fig -5: Proposed style of JK flip-flop majority gate structure

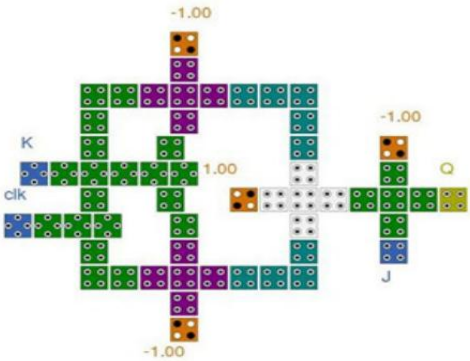

Fig -6: Proposed layout design of the JK flip-flop

Table -2: Characteristic Table of JK flip-flop

J	K	Qn+1
0	0	0
0	1	0
1	0	1
1	1	Toggle

When the pulse of the clocking is provided to the flip-flop circuit, the output signal starts toggle that is half the frequency of the input T. Construction of frequency dividers, binary counters and for simple binary addition is useful. The proposed T flip-flop circuit is a simplified method of the all the previous designs. The proposed majority gate structure of the T flip-flop is shown in the Fig. 7. The characteristic table of the flip-flop circuit is shown in the table.3. The proposed T flip-flop layout schematic that is seen in Fig. 8 has one T input, one clock input, four negative fixed polarizations, and one positive fixed polarization.

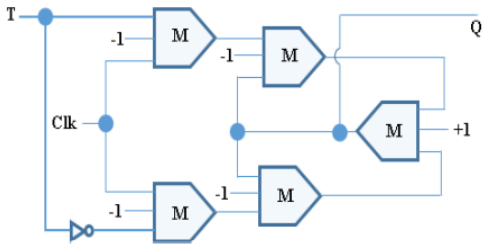

Fig -7: Proposed style of T flip-flop majority gate structure

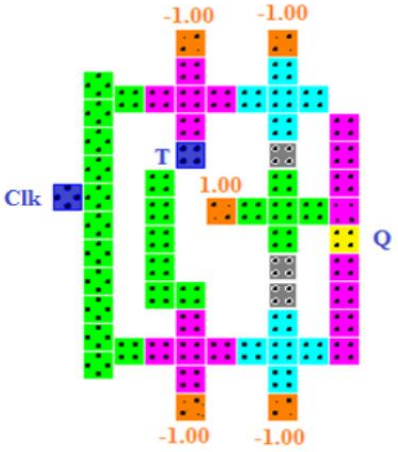

Fig -8: Proposed layout design of the T flip-flop circuit

Table.3 Characteristic Table of T flip-flop

Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

The very most important of the clock input flip-flop circuit is the D Flip Flop, since it implies how inputs S and R aren't ever similar to the one signal at the exact time. The D flip flop circuit is built from a gated SR flip-flop circuit with just an inverter inserted among the input S and input R to permit for a single binary input D (Data). This is the very easy and simple version among all the existing D flip-flop. The proposed majority gate structure of the T flip-flop is shown in the Fig. 9. The characteristic table of the flip-flop circuit is shown in the table.4. The proposed design layout that is

presented in Fig.10 has D input, clock input, one fixed positive polarization, and two fixed negative polarizations and the Q output.

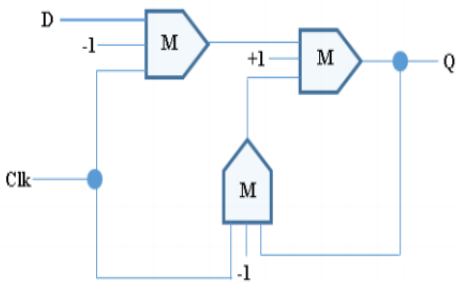

Fig. 9: Proposed style of D flip-flop majority gate structure

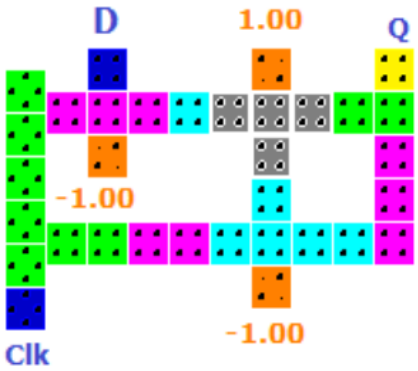

Fig.10: Proposed layout design of the D flip-flop circuit

Table.4 Characteristic Table of D flip-flop

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

The parallel input parallel output shift register is designed by using the D flip-flop circuit is shown in the below fig. it has a series combination of four series connection of the above proposed D flip flop. It has four parallel data inputs from D1 to D4 and the four parallel output lines from Q1 to Q4. When we gave the four inputs simultaneously, we will get the outputs also simultaneously. For this we gave the clock input to all the D flip flops simultaneously.

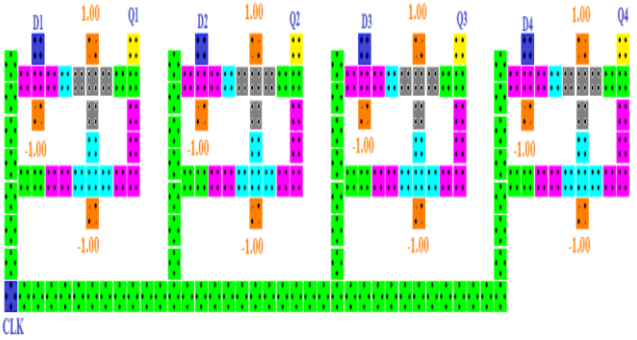

Fig. 11: Proposed layout design of the PIPO shift register

4. SIMULATED RESULTS

The simulated results of the various flip-flop circuits are designed and simulated by using the QCADesigner tool.

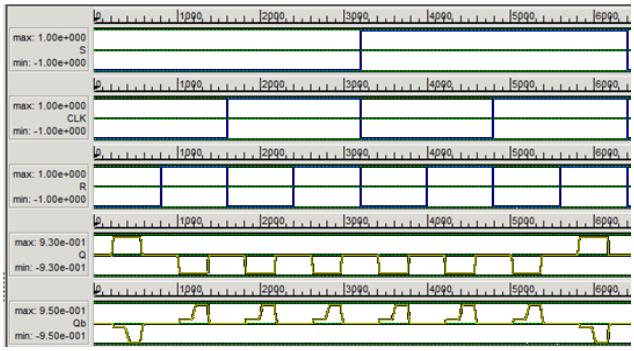

Fig.12: SR flip-flop circuit simulated results

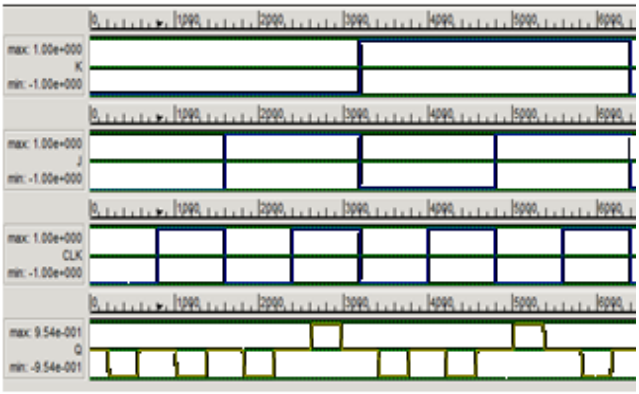

Fig.13: SR flip-flop circuit simulated results

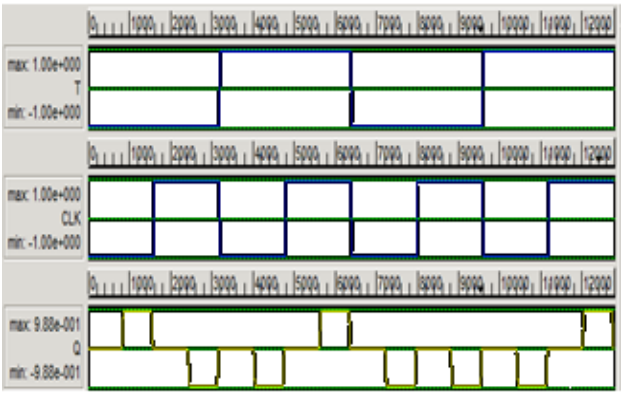

Fig.14: T flip-flop circuit simulated results

Fig.15: D flip-flop circuit simulated results

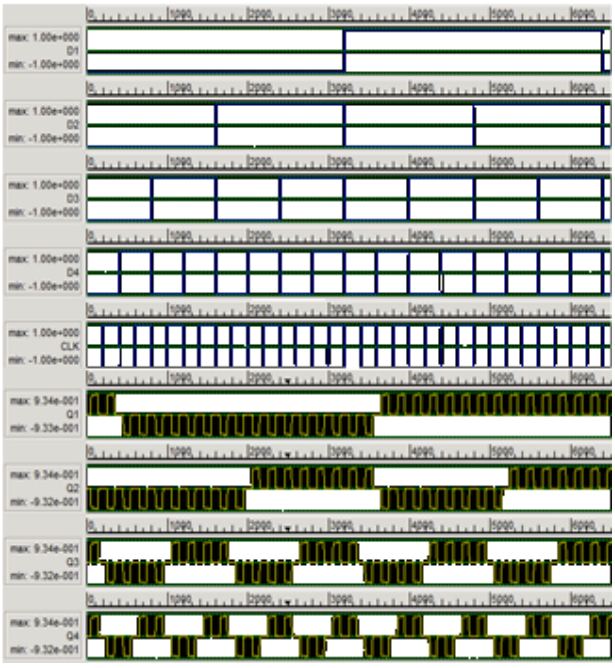

Fig.16: PIPO shift register simulation results

5. CONCLUSIONS

In this work, we have developed and simulate the flip- flop circuits like SR flip-flop, JK flip-flop, D flip-flop and T flip-flops are subsequently designed and simulated by using the QCA design tool. This is the latest method of designing the flip-flop circuits with much less hardware difficulties in the nano-technology region. Any of the storing device can be designed by using the proposed flip-flop layouts. The layout of the circuit is created, and outcomes are simulated by using the QCADesigner tool. In this paper also designed the parallel input parallel output shift register (PIPO) by using the D flip-flop layout. In the coming future there is possibility of designing the other sequential logic circuits like registers, memory blocks by using the proposed designs

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