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FULL ADDER DESIGN IMPLEMENTATION BY USING TRANSISTOR AND XNOR GATE

Vinothkumar K[1], Kavitha B[2], Keerthana A[3], Kowsalya Devi V[4]

[1]Professor, Department of ECE, Muthayammal Engineering College, Tamilnadu, India
[2,3&4] UG Students, Departments of ECE, Muthayammal Engineering College, Tamilnadu, India

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ABSTRACT

In the technologically developing to reduce a time, space and increasing speed. This is 3 transistor xnor gate is proposed. The proposed XNOR gate is designed using Tanner tool and simulated using the Tanner S-edit technology. The proposed results are compared with the previous existing designs in terms of power and delay. It is also observed that the delay is reduced by 31.82% for three transistors XNOR gate and 28.76% for eight transistors full adder.

Keywords: CMOS, full adder, exclusive-NOR (XNOR), low power, delay, transistors, VLSI, High-Level synthesis.

I. INTRODUCTION

In present days, out of speed, area, time, power is the main issue in electronic design systems. Extra power consuming results in components overheating and makes the system failure so we need to design an IC's which consumes less power became the main criterion in the various devices like mobile phones and laptops, High speed work stations etc. Day by day, power management has become the major issue and challenging task for improving battery life time and to reduce the charging time in the electronic handheld devices. The achievement fidelity applications. The characterization and raise of such low power multipliers will cooperation in comparison and choice of multiplier modules in system design. With drastic improvement of the electronic goods, lot of transformation is done and lot of technology is developed in the area of VLSI. More number of gates are integrating on the Chip changed the era of VLSI. So low power is the main area to be concentrated to reduce heat on chip and to extend the battery life and also chip life. The system specification is the processor.

II. METHODOLOGY

This methodology for four bit ripple carry adder, eight transistors full adder and also discussed the low power analysis. This present four bit Ripple carry adder is mapped into Tanner tool and power and delay are decreased. The results is viewed using tanner s-edit tool. Basically it is also known as sequential adder and basic adder and it is also known as basic adder and sequential adder. The full adder comprises of two half adders and it can be realized using the gate delays. The Soc design consists of total power as static power and dynamic power. Dynamic power is the dissipated power when the device is in active mode. Static power is the power consumed when the device is in active mode but the signal values are unchanged.

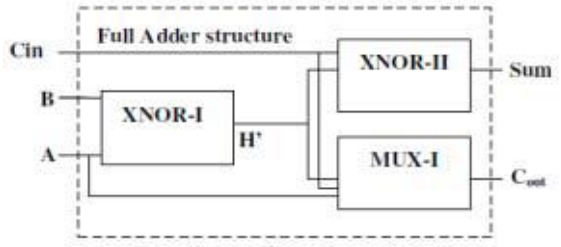

Figure 1: Proposed diagram.

Working principle

The four bit ripple carry adder is mapped into Tanner tool. The results of mapping are viewed using tanner s-edit tool in Tanner tool technology. We proposed mapping style into Tanner tool using xnor gate in the full adder design. The full adder is performed a two half adder and it reduced a power and perform a high speed in the giving power. We proposed mapping style into tanner tool using four bit ripple carry adder by observing the four bit ripple carry adder powers dissipation. The Simulations of xnor gate using three transistors, full adder using six transistors and eight transistors are carried out using Tanner tool technology. The six transistors xnor logic with the input of A, B and output of Vout. For all input combinations frequency of 100MHz signal is applied and verified. During verification of logic, power and delay are measured.

III. MODELING AND ANALYSIS

Materials used in the projects are Tanner EDA tool, Tanner S-edit tool, full adder and exclusive-NOR (XNOR).

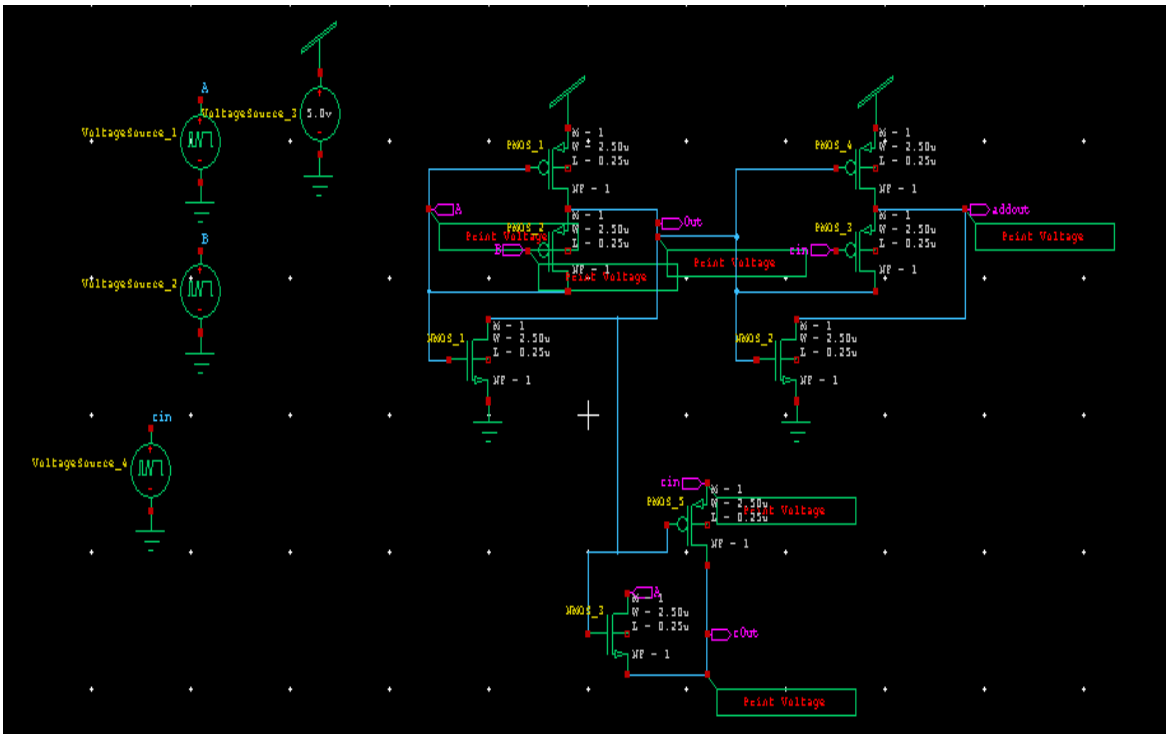

Figure 2: Full adder design implementation by using transistor and xnor gate

Tanner Tool

Tanner tool is a suite of tools for the design of integrated circuits. These tools allow you to enter schematics, perform SPICE simulations, do physical design and perform design rule checks and layout versus schematic checks. Tanner tool is a complete circuit design and analysis system that includes schematic editor. Electronic design automation is a category of software tools for designing electronic system such as integrated circuits and printed circuits board. SPICE is a general purpose, open source analog electronic circuit simulated. It is a program used in integrated circuit and board level design to check the integrity of circuit designs and to predict circuit behavior.

Tanner S-edit

Tanner s edit is an easy to use design environment for schematic capture and design entry. It gives you the power you need to handle your most complex mixed signal IC design capture. S edit is tightly integrated with tanner T-spice simulation, the tanner L edit IC layout tool and the tanner verify DRC and LVS tool. We proposed mapping style into tanner tool using four bit ripple carry adder by observing the ripple carry adder powers dissipation. The Simulations of xnor gate using three transistors and full adders using six transistors and eight transistors are carried out using tanner technology.

Full adder

A full adder contains three inputs and two outputs. And it is also known as basic adder and sequential adder. The full adder comprises of two half adders. And it can be realized using the gate delays. The full adder is sequential adder is the inputs are given in a sequential order and these adders are faster than the other adders for a few bit numbers and becomes bit slower when comes to the higher bits.

XNOR gate

The XNOR gate is a digital logic gate whose function is the logical complement of the exclusive OR gate. The xnor gate is performs the inversion process of the OR gate performance.

IV. RESULTS AND DISCUSSION

This present's four bit ripple carry adder is mapped into tanner compiler. It observing the four bit ripple carry adder output waveform. It is reduced the power and delay. The results is viewed by tanner s edit tool. The output represents the power delay and time delay and improved the speed. The Simulations of XNOR gate using three transistors, full adder using six transistors and eight transistors are carried out using Tanner tool technology.

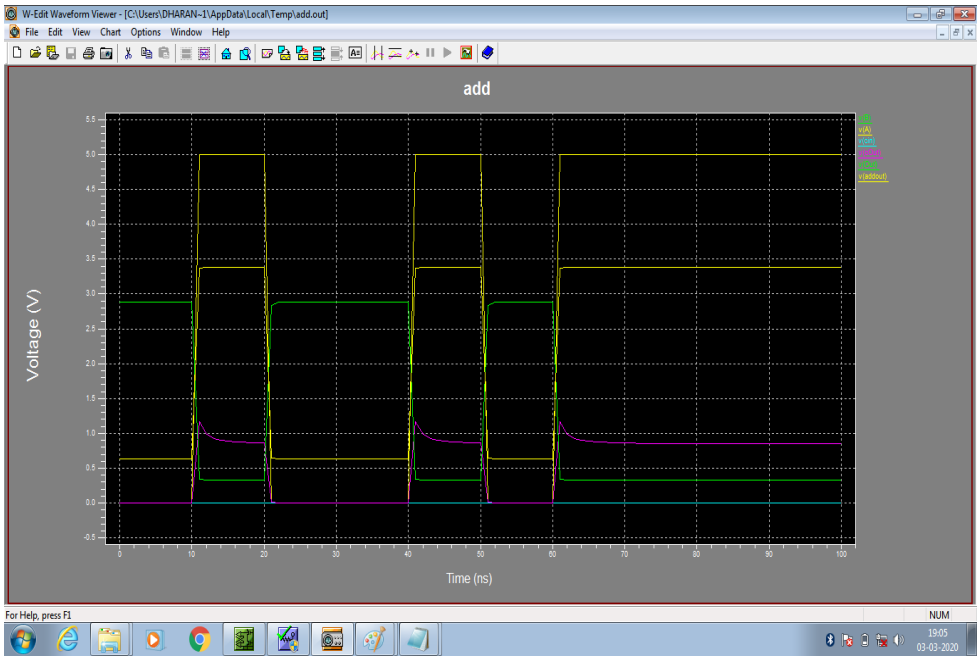

Figure 3: Full adder design implementation by using transistor and xnor gate output.

V. CONCLUSION

The full adder design implementation by using transistor and xnor gate we proposed an xnor gate using three transistors and eight transistors using Tanner tool technology. From the results and graph, it is concluded that the design proposed for xnor gate using 3 transistors, full adder using eight transistors has better performance than in terms of delay and power. And also we proposed four bit ripple carry adder is mapped into Tanner tool. By efficiently mapping into tanner tool, power decreased. The results of mapping are viewed using RTL synthesis tool in tanner s-edit technology.

VI. REFERENCES

[1] N.Prathima, K.Harikishore, "Design of a low power and High performance digital multiplier using a novel 8T adder", International Journal of Engineering Research and Applications,Vol. 3, Issue 1, January -February 2013, pp.18321837 Smith, B. S. and Carter, C. (1969). A method of analysis for infilled frames, Proceedings of the Institution of Civil Engineers, Vol.7218, 31-48.

[2] A. M. Shams and M. Bayoumi, "A novel high-performance CMOS1-bit full adder cell," IEEE Transaction on Circuits Systems II, Analog Digital Signal Process, vol. 47, no. 5, pp. 478–481, May 2000.

[3] Ronn B. Brashear, Noel Menezes, Chanhee Oh, Lawrence T. Pillage, and M. Ray Mercer., Predicting Circuit Performance Using Circuit- level Statistical Timing Analysis., Department of Electrical and Computer Engineering The University of Texas at Austin.

[4] Vaibhav Gupta, Debabrata Mohapatra, Anand Raghu Nathan., and Kaushik Roy, Fellow, IEEE., Low-Power Digital Signal Processing Using Approximate Adders., 0278-0070/$31.00 c_ 2012 IEEE.

[5] Yaseer A. Durrani a, Teresa Riesgo b., Power estimation technique for DSP architectures Digital Signal Processing 19 (2009) 213–219., Contents lists available at Science Direct., www.elsevier.com/locate/dsp, 1051-2004/$ – see front matter 2008 Elsevier Inc.