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Realization of Mathematical Function by Stochastic Logic Using FPGA

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Abstract -*Stochastic computing (SC) is a complete combination of analog and digital concept. Basically, stochastic logic computes on analog which is operated and converted using digital bitstream. This computing aspect exploits the advantages such as low power consumption, less delays, reduce hardware platform, throughput, high efficiency. This paper described stochastic logic operation with application in digital signal processing field for finite impulse response filter. Here paper makes two contributions. Firstly it is shown that operation of FIR filter using stochastic logic computation. Second, compares the output result of conventional and stochastic FIR filter. So this comparison verified the efficient computing method along with various parameters which are most vital in any designing in VLSI field. The whole stochastic logic design is coded through VHDL (Hardware Descriptive Language). The output results for both filters were simulated, compiled and synthesized by using ModelSim-Altera 10.3C and Quartus 2 9.1sp2 software.*

Key Words: **Stochastic logic, digital signal processing, FIR filter, arithmetic and logical function, VHDL**.

1. INTRODUCTION

In VLSI system main motto for any general application-large number of elements are converted on small platform. So this is the basic need of modern technology. From ancient time uptill now there is continuous scaling of MOS transistor which we called as nm scale technology. So due to the advancement in vlsi field size of transistors goes on reducing and increasing its numbers that causes vast amount of power consumption, leakage current, unreliability of circuits as well. To address this problem, here I introduce stochastic computing and realization of various functions on FPGA with its application of Digital Signal Processing (DSP).

1.1 Stochastic Computing

Some potentially beneficial applications of computer technology cannot be realized because they have extreme requirement of small size, high speed or ultra low power, for such requirement solution has accelerated towards a wide variety of alternative computing methods. Stochastic computing uses digital logic approach to perform on continuous random bit stream, where signal value is encoded as the probabilities of 0's and 1's in a stream. This technique is a completely blending of analog and digital logic. Deterministic computation such as FSM required lots of iterations so that time and power dissipation increases. Owning to drawback, where probabilistic results are acceptable for specific applications at that platform stochastic computing is best technique because it saves our time, power dissipation along with less delay. Strength of stochastic logic is complex arithmetic function can be implemented with very simple digital logic gates with minimal number. It is so called stochastic because it computes with analog probabilities but represented them by digital bit stream and processes them with logic circuits. When probabilistic laws are applied to digital clock, it results in stochastic computing. Complex function can be computed by simple bit wise operations on collective bit stream. Basic operation for stochastic computing is addition, multiplication and delay element.

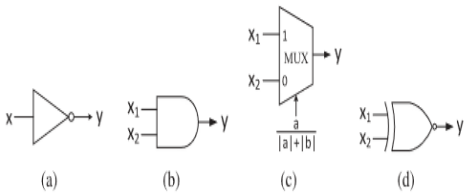


Figure-1: Fundamental operation for stochastic logic

1.2 Digital signal Processing Application: FIR Filter

In DSP stochastic logic is used as application. Finite impulse response filters are one of the most commonly used in DSP field and FPGA is a device platform used to implement it.FIR means impulse response becomes zero after finite number of sample. Main function of FIR for DSP-noise removal from input signal to get desired one. Aim of DSP blocks are used to enhance performance of these arithmetic operations and because of multiple DSP block connection it builds efficient FIR system.

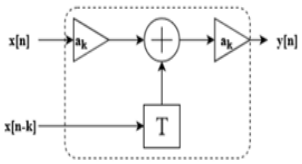


Figure-2: Example of signal flow graph for FIR filter

Mathematically, filter is given by difference equation:

$$y[n]=x[n].h[n]$$

$$y[n] =\sum ak \, . \, x(n-k)$$

Where, ak-FIR filter coeffient

x(n-k)-delayed version of input signal

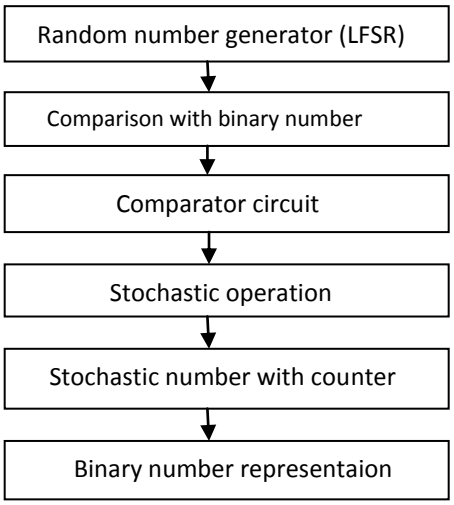
2. LITURATURE SURVEY

S. T. Ribeiro, et al [1], this paper states technique of random-pulse computation and its potential implication. Problems of realization, application examples, and alternate coding schemes are discussed. Speed, accuracy, and uncertainty dispersion are estimated. A brief comparison is made between random-pulse processors and biological neurons. This paper presents and discusses three interlacing ideas: 1) performing algebraic operations with logical gates output pulses by using random pulse reprentation; 2) creation of a class of random-pulse machines; and 3) the construction of highly parallel processors consisting of large iterative arrays of simple arithmetic units. X. Jiang, et al [2], paper introduces structure characteristics and the basic principles of the finite impulse response (FIR) digital filter, and gives an efficient FIR filter design based on FPGA. First got 16-order FIR filter coefficient and then analyze filter design for performance finally implement by using VHDL language. A.S. Chauhan, et al [3], describes the development of FIR filters on Field programmable gate array (FPGAs) using IP cores. FIR filter has been designed and realized by FPGA for filtering the digital signal. To check the accuracy of result, observed output is compared with calculated result so that output designed is fully complies with requirement. A. Alaghi, et al [4], described the design of SC-based circuits and evaluate their advantages and disadvantages and gave examples of the potential applications of SC and discuss some practical problems that are yet to be solved. This article surveys SC from a modern perspective where the small size, error resilience, and probabilistic features of SC may compete successfully with conventional methodologies in certain applications. C.J. Chou, et al [5]s, described an approach to the implementation of digital filter algorithms based on field programmable gate arrays (FPGAs). General purpose DSP implementations often lack the performance necessary for moderate sampling rates, and ASIC approaches are limited in flexibility and may not be cost effective for many applications. The given examples of FIR and IIR filter implementations illustrate that the FPGA approach is both flexible and provides performance comparable or superior to traditional approaches. Because of the programmability of this technology, the examples in this paper can be extended to provide a variety of other high performance FIR and IIR filter realizations. A. Singh, et al [6], described hardware implementation of digital signal processing filters on FPGA. It also suggests the given design is very effectively work as compared to traditional one. It developed 8 order band pass, high pass, low pass filters which is implemented by Spartan3 FPGA Kit. This approach also gives the best performance as compared to simpler filters in terms of cost, power consumption and speed. A. Alaghi, et al [7], this paper gives the brief introduction about challenges, applications and correlation among stochastic operation. It highlights the potential methods overcoming them. Stochastic computing involved the applications such as image processing, decoding and error correcting code and artificial neural network. At a same future challenges regarding stochastic computation also discussed for examples accuracy management, design optimization, biomedical devices and energy harvesting. S. Kumar, et al [8], illustrates the application of FIR filter for denoising. The filter output showed distortationless waveform. The paper concentrate on basically parameters such as lessening area, decrease of noise, less power utilization and low delay which is most important parameters for stochastic computing according to vlsi approach. V.T. Lee, et al [9], this paper outlines a new set of correlation manipulating circuits a synchronizer, desynchronizer, and decorrelator - for managing correlation between SNs and show how using correlation manipulating circuits can improve the accuracy of SC computations and are more energy efficient than using existing correlation manipulation techniques in the context of an image processing pipeline. K.K. Parhi, et al [10], most basic paper for stochastic operation computing for various applications in various fields. This paper demonstrated various complex arithmetic function implemented by Stochastic logic which uses various mathematical series expansion methods to reduce the complexity of function (arithmetic or any mathematical).Also compared the proposed system with conventional methods for excellent performance.

3. METHODOLOGY and PROPOSED WORK

Propose work concentrates on stochastic computing method by using FPGA. This work address to introduce a computing method by stochastic logic for complex arithmetic and logical function and used in digital signal processing application for FIR filter and various parameters are used to analyze and compare performance of the system. The proposed methodology described as follows by flow chart-

Firstly, random number source generator linear feedback shift register (LFSR) is used. For input conversion of binary number into its corresponding stochastic number and vice versa, is a compulsory process. LFSR is designed for cryptographically secure computation base method.



Flow chart: Stochastic logic computation

These bit streams described at each micro cycle, here random numbers are produced and contrast with binary number which is arranged in registers. After that third stage is very important generated sequences are sending to comparator units where they are compared with input probability to produce stochastic stream.

All input are converted to binary sequence of 0 and 1's and then ready for stochastic operation. It operates on continuous bitstream at a time. Realization of complex arithmetic function or any application of SC all basic operations are performed here they are- For complementary function simple not gate is used, for multiplication AND gate, addition multiplexers, subtraction XOR gate, division two and gate and two XNOR gate and square AND gate with delay is used. This stochastic output attached to counter which counts the number of 1's in bit stream at each clock cycle. Finally 0, 1 binary sequence represents the respective value output. These value of ALU are simulated by Altera Quartus2 by VHDL programming, simulated by Modelsim Sf 9.1c.Altera DE2 board is used for hardware interfacing. Proposed work is used for realization any complex arithmetic operation to get simpler one.

Application of stochastic logic in DSP field for FIR filter play very important role to analyze the system based on stochastic computing.

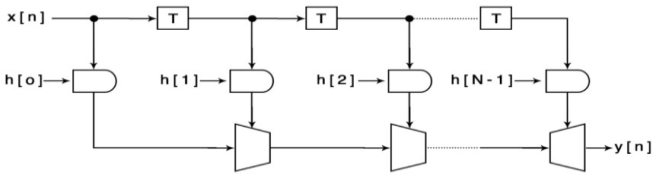


Figure 3: Stochastic implementation of FIR filter

Here, input x(n) samples are delayed by using delayed elements which is in the form of binary number. Input and delayed element are multiplied by using AND gate operation in terms of stochastic logic.

$$y(n)=x(n)*h(n)$$

In conventional method it uses simple general multiplication. After that all coeffient get added used multiplexers so that it reduces area utilization.

4. RESULTS

This result section analyzed and compared the conventional and stochastic logic computation for FIR filter design. For this computation FPGA Device: Cyclone II – EP2C35F672C6, Altera DE2 FPGA Board is used.

Conventional FIR Filter

1. Device Utilization Summary (Area Resources)

Flow Status	Successful - Tue Jun 09 16:34:43 2020
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	fir_4tap
Top-level Entity Name	fir_4tap
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	260 / 33,216 (< 1 %)
Total combinational functions	258 / 33,216 (< 1 %)
Dedicated logic registers	50 / 33,216 (< 1 %)
Total registers	50
Total pins	25 / 475 (5 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

2. Power Utilization

PowerPlay Power Analyzer Status	Successful - Tue Jun 09 16:34:43 2020
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	fir_4tap
Top-level Entity Name	fir_4tap
Family	Cyclone II
Device	EP2C35F672C6
Power Models	Final
Total Thermal Power Dissipation	112.87 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	79.93 mW
I/O Thermal Power Dissipation	32.94 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

3. Minimum Propagation Delay

It is the length of time taken for a signal ssto reach its output.

Tco (Time clock to output) = 8.542 ns

4. Maximum Frequency

It is the rate at which clock input of a system can drive, while maintaining proper operation. High frequency gains fast computation i. e. it increases speed and because of high speed, system dissipates very less power which is main requirement of dissertation.

Max Freq = 1 / Tco = 117.068 MHz

5. Throughput

It is used to measure performance of system. Higher the throughput, more productive system. Productivity measures how efficiently you developed them.

Throughput = No of bits * Max Freq / No of Clk Cycles = (8 * 117.068 / 1) = 936.544 Mbps

Stochastic FIR Filter

1. Device Utilization Summary (Area Resources)

Flow Status	Successful - Tue Jun 09 17:30:02 2020
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	fir_4tap
Top-level Entity Name	fir_4tap
Family	Cyclone II
Device	EP2C35F672C6
Timing Models	Final
Met timing requirements	Yes
Total logic elements	7 / 33,216 (< 1 %)
Total combinational functions	0 / 33,216 (0 %)
Dedicated logic registers	7 / 33,216 (< 1 %)
Total registers	7
Total pins	25 / 475 (5 %)
Total virtual pins	0
Total memory bits	0 / 483,840 (0 %)
Embedded Multiplier 9-bit elements	0 / 70 (0 %)
Total PLLs	0 / 4 (0 %)

2. Power Utilization

PowerPlay Power Analyzer Status	Successful - Tue Jun 09 17:30:02 2020
Quartus II Version	9.1 Build 350 03/24/2010 SP 2 SJ Web Edition
Revision Name	fir_4tap
Top-level Entity Name	fir_4tap
Family	Cyclone II
Device	EP2C35F672C6
Power Models	Final
Total Thermal Power Dissipation	112.80 mW
Core Dynamic Thermal Power Dissipation	0.00 mW
Core Static Thermal Power Dissipation	79.93 mW
I/O Thermal Power Dissipation	32.86 mW
Power Estimation Confidence	Low: user provided insufficient toggle rate data

3. Minimum Propagation Delay

Tco (Time clock to output) = 8.150 ns

4. Maximum Frequency

Max Freq = 1 / Tco = 122.699 MHz

5. Throughput

Throughput = No of bits * Max Freq / No of Clk Cycles = (8 * 122.669 / 1) = 981.352 Mbps

Table-1: Comparative Analysis of Performance Parameters

Sr. No.	Specifications	Conventional FIR filter	Stochastic FIR filter
1	Total registers	50	7
2.	Total logic elements	260	7
3.	Total s power dissipation	112.87mw	112.80mw
4.	Minimum propagation delay	8.542ns	8.150ns
5.	Maximum frequency	117.068mHz	122.699mHz
6.	Throughput	936.544mbps	981.352mbps

6. CONCLUSIONS

Many mathematical complex functions are converted into simpler ALU operation with the help of stochastic logic. Realization of various ALU operations such as scaled addition, subtraction, multiplication are carried out with the help of stochastic computing. Application of SC for FIR filter is very effective because it saves area, time as well as power of the system.FIR filters are most commonly used in digital signal processing. Stochastic computing also increases frequency and throughput of the system so that we got required results for FIR filter. Proposed work not only computes the results but also compared with conventional methods to analyze the performance of proposed work.

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