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MODIFIED ASSYMETRICAL MULTILTVEL INVERTER FOR RENEWABLE POWER APPLICATIONS

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Abstract - *: Now a day's the most drawbacks in power electronic circuit are switching loss, harmonic and voltage stress within the switch. To eliminate the losses, we have to include some different methods like multilevel inverter. To overcome the harmonic drawback the multilevel inverter provides an acceptable solution for medium and high-power systems to synthesize an output voltage that permits a discount of harmonic content in voltage and current waveform. The design of the control circuit for a solar fed cascaded multilevel inverter to reduce the number of semiconductor switches presented in this study. The design include modified multilevel connection. Modern Multilevel Converter-based topologies suitable for varying input sources from the solar photovoltaic (PV). In binary mode, 2(Ns +1) – 1 output voltage levels are obtained where Ns is that the number of individual inverters. This is achieved by digital logic functions which includes counters, flip-flops and logic gates. In trinary mode, 3Ns levels are achieved by corresponding look-up table. MMC intends design in both control and power circuits to supply corresponding output voltage levels by appropriate switching sequences. Hence to get a 15-level inverter, the traditional method requires 28 switches and in binary mode 12 switches are needed but in MMC only 7 switches are employed to achieve 15 levels. The advantage of those three designs is within the reduction of total harmonic distortion by increasing the amount.*

Key Words: **Multilevel Inverter (MLI), Total Harmonic Distorsion (THD), Sinusoidal Pulse Width Modulation (SPWM), Neutral Point Clamped (NPC), Transistor Clamped H Bridge (TCHB), Cascaded H Bridge (CHB), Flying Capacitor Multilevel Inverter (FCMLI), Modified Multilevel Connection (MMC)**

1. INTRODUCTION

Due to improved fuel efficiency, reliability, maneuverability and reduced emissions, all-electric ships (AES) have attracted increasing interests from marine industry in recent years. With an increasing need for electricity in AES, as a result of more electrical loads with different power requirements such as electric propulsion load, pulsed load and distribution load, more power electronic converters are adopted in shipboard power system (SPS). However, the introduction of power electronic based systems will lead to harmonic pollutions in SPS and degrade the power quality of the system. In order to improve the power quality of SPS, these harmonics should to be eliminated.

Several methods have been developed to deal with this issue. Passive power filters can be utilized to mitigate these harmonics. Though they are simple and easy to control, these equipments are bulky, inflexible and have low compensation ratings and high risk of resonance problems which limit their applications for compensation. Active power filter is an alternative promising way to mitigate the harmonic distortions. Many topologies of active power filter have been developed in recent years. A hybrid active power filter is proposed, which is a combination of a parallel passive filter in series with an active power filter (APF). This topology can provide a cost-effective solution for harmonic compensation. Another configuration of shunt hybrid active power filter is that the passive filter is in parallel with an active power filter. Two-level APFs are implemented to compensate harmonics in these hybrid active power filters.

However, two-level APFs aren't suitable for medium or high voltage applications that required large compensation capacity. Active power filter supported multilevel converters has also been studied in many papers. at the present , there are four multilevel converter circuits for active power filter, i.e.Cascaded H-bridge converter, neutral point clamped, flying capacitor converter and modular multilevel converter. Among these active power filter topologies, the APF supported MMC has its advantages of low output current total harmonic distortion (THD), high modularity, low power device stress, etc. Multilevel inverter provides a suitable solution for medium and high power systems to synthesis an output voltage which allows a reduction of harmonic content in voltage and current waveforms. Multilevel inverter refers to the multiple connections of individual inverters defined as 'stages' to provide the output voltage with required levels. Increasing the number of levels will result in the reduction of harmonic distortion. The 3 topologies such as flying capacitor, neutral point clamped and cascaded multilevel inverters are highly opted regarding various applications depending upon its design and modulation algorithms. Among the three topologies, cascaded multilevel inverters are very highly preferred for the interconnection of

renewable energy systems because of the various advantages such as absence of voltage unbalance problem, elimination of DC–DC boost converter, adaptive at low switching frequency and absence of clamping capacitors and diodes.

2. PROPOSED ASYMMETRICALLY MULTI-LEVEL INVERTER FOR RENEWABLE ENERGY APPLICATIONS

2.1 BLOCK DIAGRAM

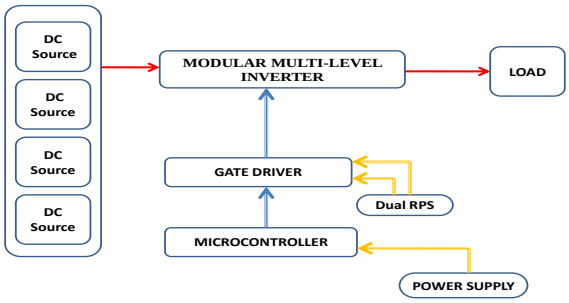


Fig-1 **Block diagram of proposed model**

In binary mode 16 switches are needed but in MMC only 8 switches are employed to achieve 31 levels. The advantage of these three designs is in the reduction of total harmonic distortion by increasing to eliminate the losses, we have to include some different methods like multilevel inverter. To overcome the harmonic drawback the multilevel inverter provides an acceptable solution for medium and high-power systems to synthesize an output voltage that permits a discount of harmonic content in voltage and current waveform. The design of control circuit for cascaded multilevel inverter to reduce the number of semiconductor switches is presented in this study. Among 'binary', 'trinary' and 'modified multilevel connection', (MMC)-based topology is suitable for varying input sources. In binary mode, 2(Ns +1) – 1 output voltage levels are obtained, Ns is the number of individual inverters. This is achieved by digital logic functions which includes counters, flip-flops and logic gates. In trinary mode, 3(Ns) levels will be achieved. MMC provides design in both control and power circuits to provide desired output voltage levels by appropriate switching sequences. Hence to obtain a 31-level inverter, the conventional method requires 32 switches the levels.

2.2 CIRCUIT DIAGRAM

Modular multilevel inverter (MMI) has extremly high switching frequency – which provides direct implication on important parameters like converter loss and reliability – mainly because of increased number of switching components. However, conventional switching techniques, where submodule sorting is just based on capacitor voltage balancing, are not able to achieve switching frequency reduction objective. Carrier-based sinusoidal pulse-width modulation (PWM) techniques, such as phase disposed PWM(PD-PWM) and phase shifted PWM (PS-PWM), are widely applied to control the modular multilevel inverters.

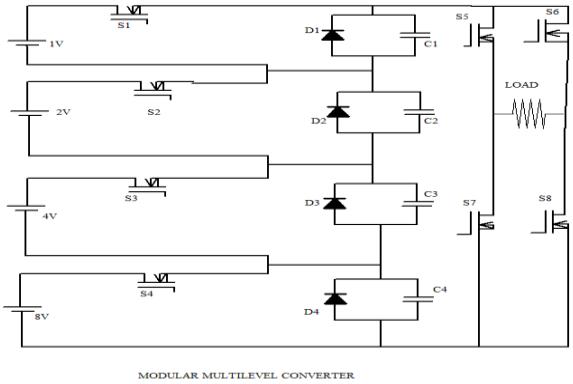


Fig-2 Circuit diagram of MMLI for 31 level output

In this approach, the modification is made in both control circuit and predominately in power circuit to obtain 31levels with only eight switches. The addition of diode and capacitor is to normalize the output within the given interval. In this method, the embedded-based controller is used for providing the gating signals based on the switching sequence according to the addition of input voltages. In developing PWM-based technique, unipolar switching with single carrier is used with switching frequency of 1 kHz.

2.3 MODES OF OPERATION

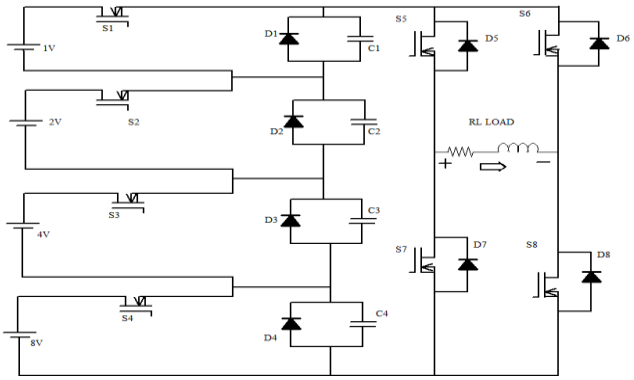


Fig-3 Mode 0

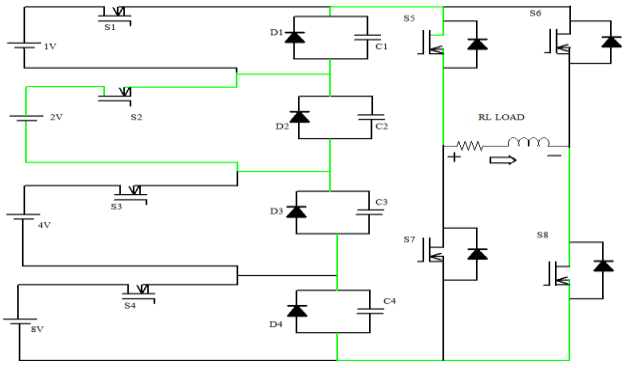


Fig-4 Mode 1

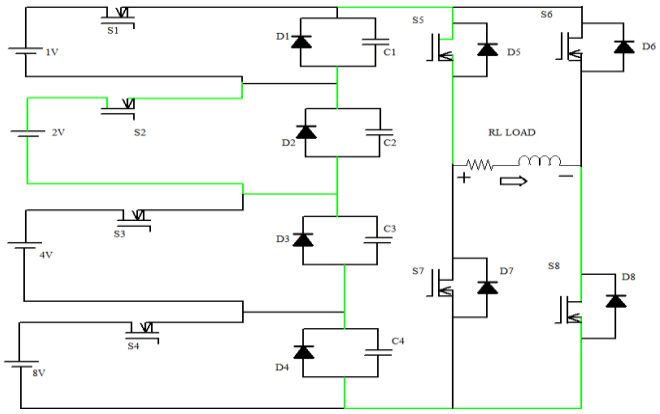


Fig-5 Mode 2

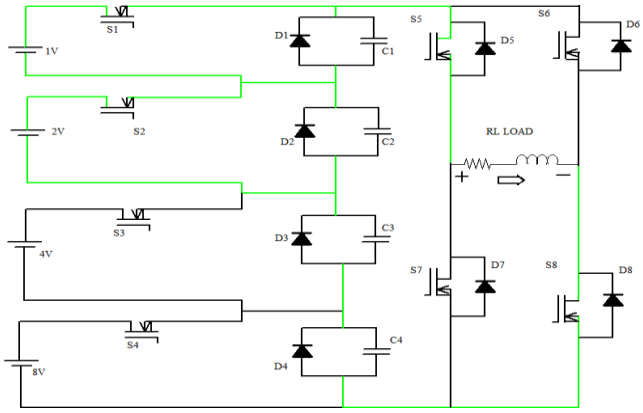


Fig-6 Mode 3

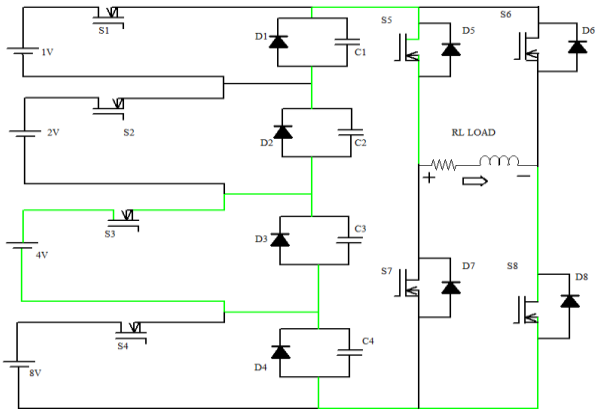


Fig-7 Mode 4

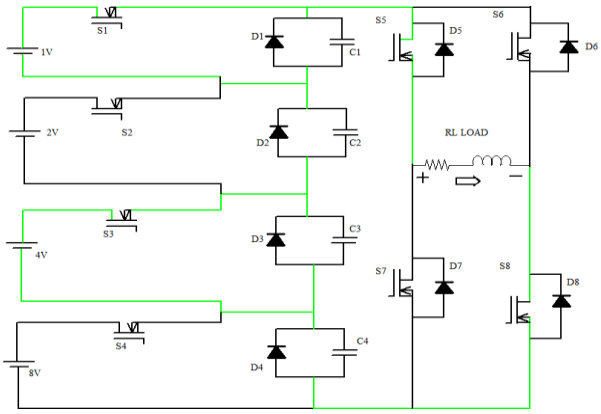


Fig-8 Mode 5

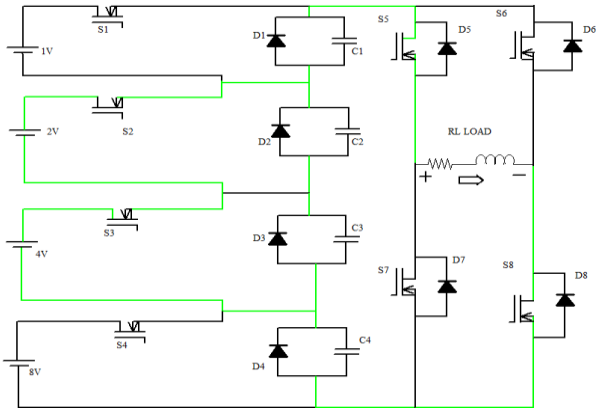


Fig-9 Mode 6

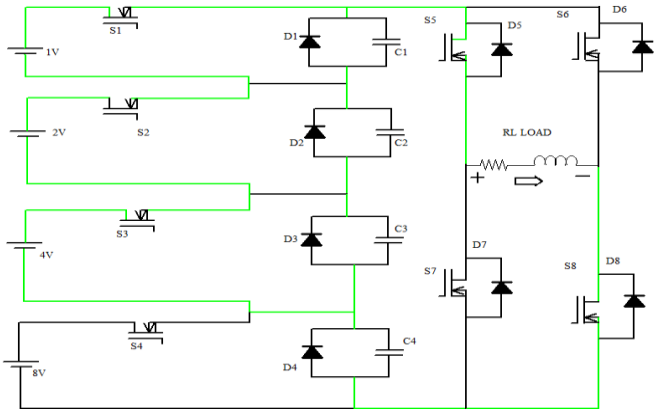


Fig-10 Mode 7

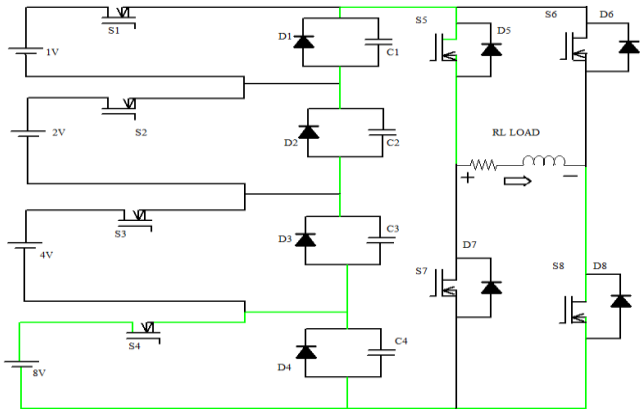


Fig-11 Mode 8

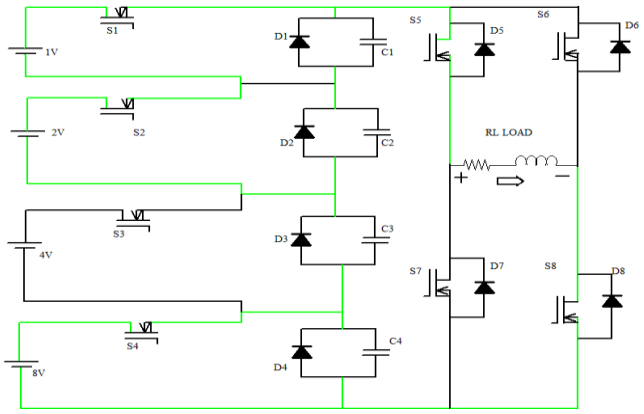
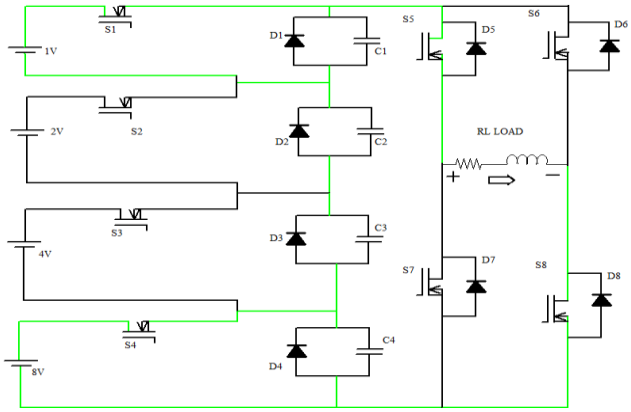


Fig-14 Mode 11



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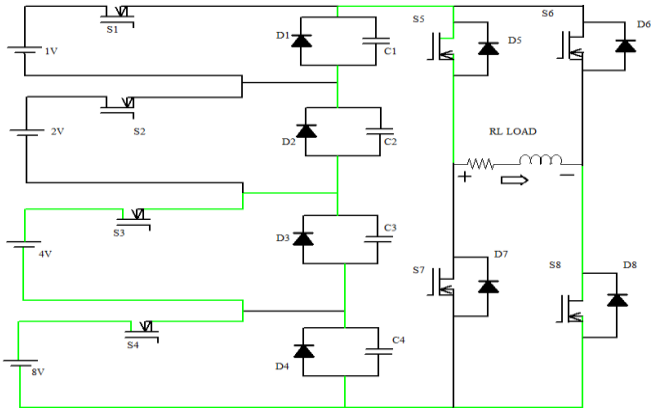

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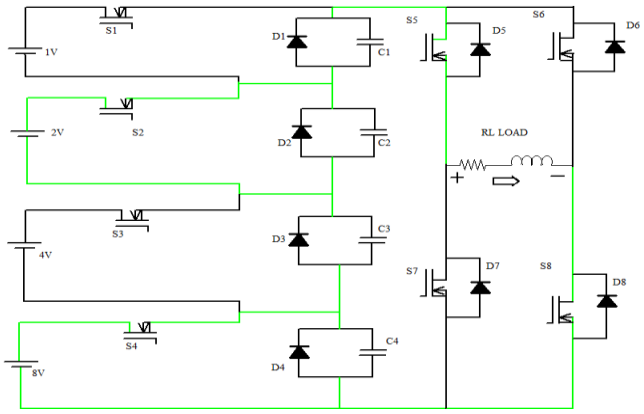

Fig-13 Mode 10

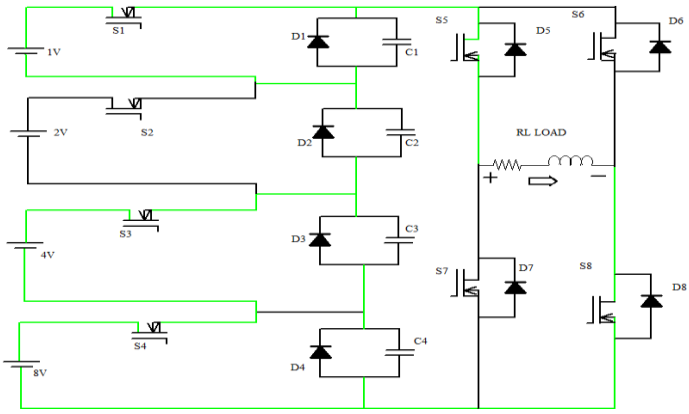

Fig-16 Mode 13

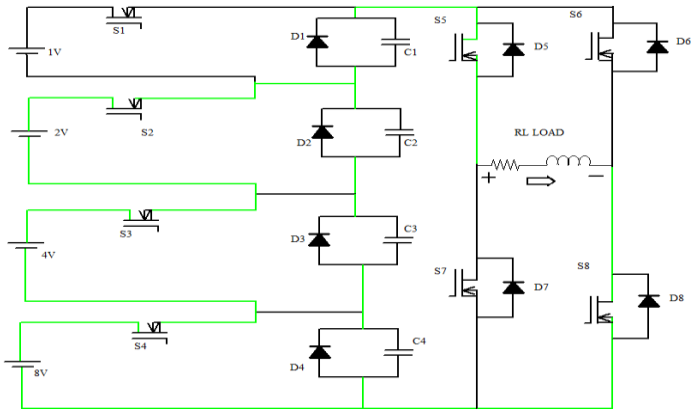

Fig-17 Mode 14

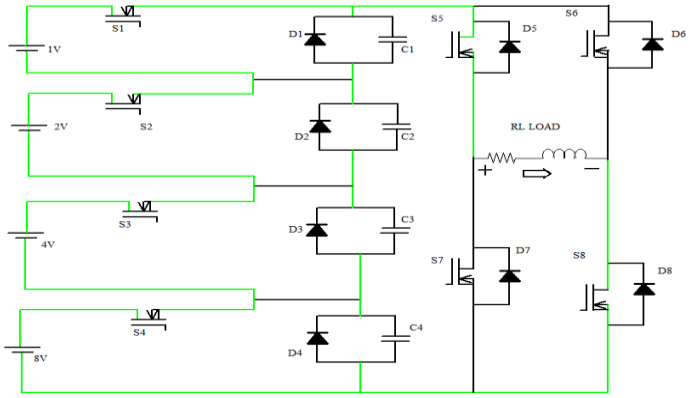

Fig-18 Mode 15

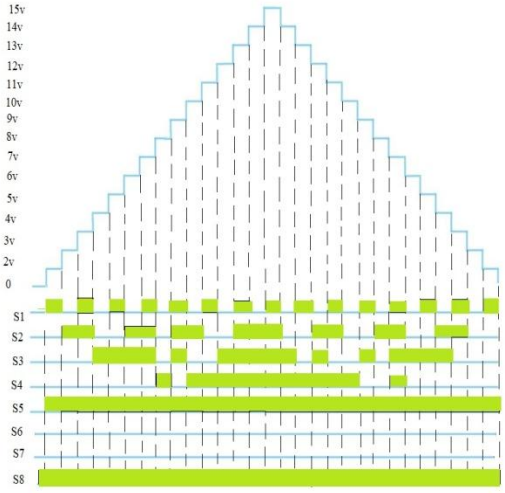

Fig-19 Positive half cycle of 31 level MMLI

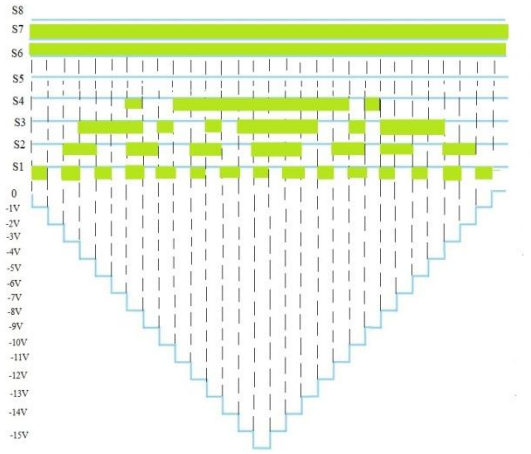

Fig-20 Negative half cycle of 31 level MMLI

2.4 SIMULATION CIRCUIT

The proposed modular multilevel converter which is designed to provide 225 Vrms , 50Hz AC supply as much of the domestic loads operates in this system. The power circuit of 31 level CMLI consist of 8 number of switches.

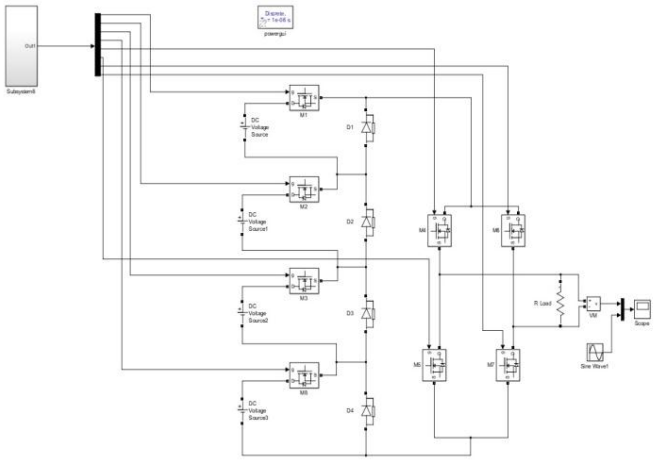

Fig-21 Simulation diagram

2.5 SIMULATION RESULTS

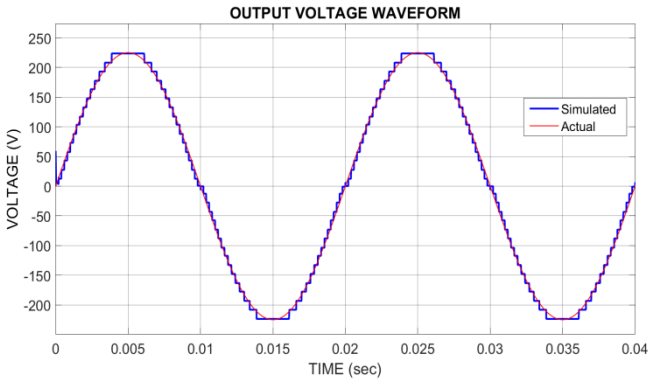

Chart-1 Output waveform of MMLI(31level)

The value of Total harmonic distortion must always be less than or equal to 5% according to the IEEE standards for efficient functioning of the system. This proposed modular multilevel inverter achieves 31 levels with the total harmonic distortion of 3.5%.Similarly, the output voltage waveform of 15 level modular multilevel inverter gives a total harmonic distortion of 2.90%

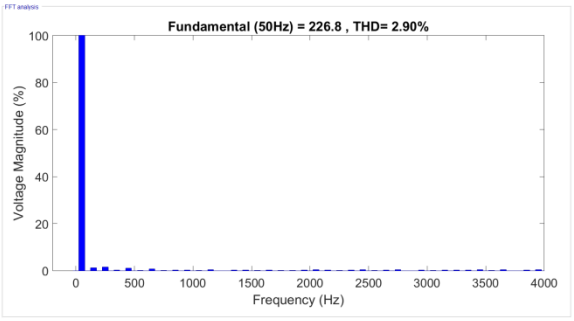

Chart-2 THD throuhg FFT analysis

3. HARDWARE SPECIFICATIONS

Table-1 Hardware components

S.NO	PARAMETERS	VALUES
1	DC input voltage	15V
2	Diode	o.oo1 ohms Vf=o.8
3	Switches	IRF840
4	Load	100 ohms
5	Fundamental frequency	50Hz
6	Maximum frequency	100Hz
7	Voltage regulator	LM8075, LM7912

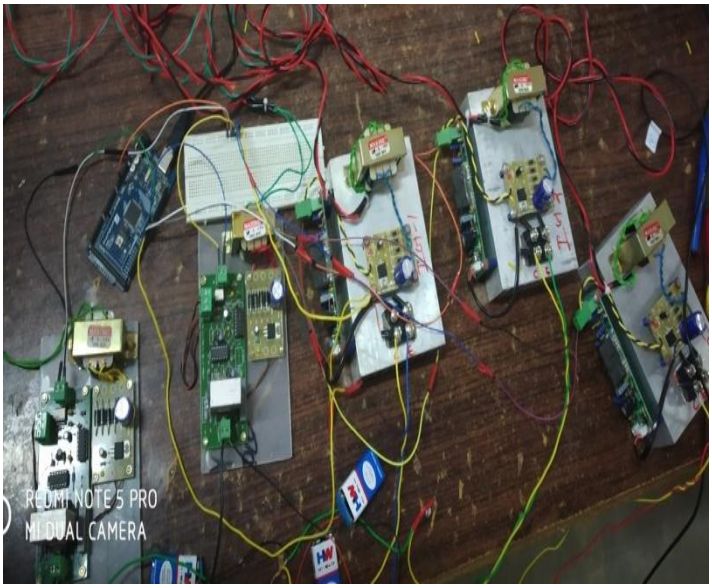

Fig-22 Hardware implementation

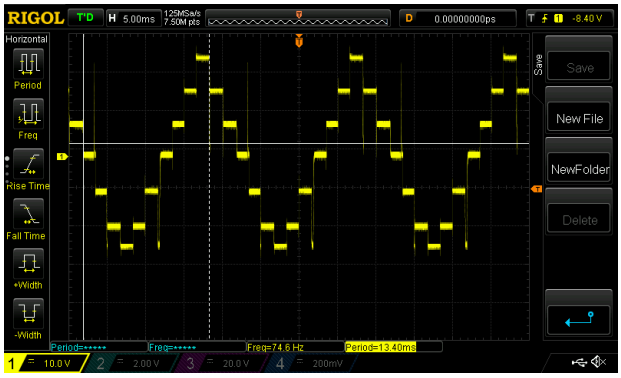

Fig-23 Output waveform during normal switching

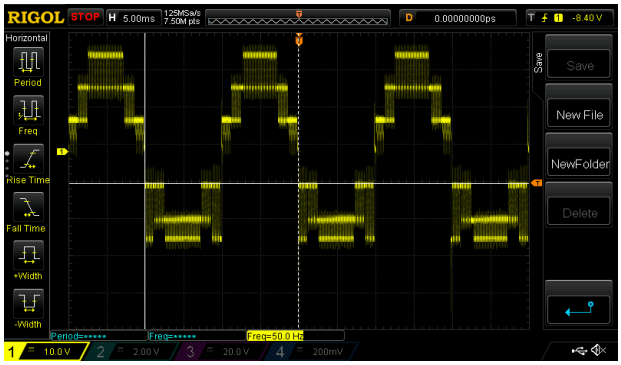

Fig-24 Output during PWM switching

4. CONCLUSIONS

Based on the results it is found that by adopting these topologies increased level Cascaded Multilevel Inverter can be obtained with reduced number of semiconductor switches. In addition, the harmonic distortion is simultaneously reduced. The power quality improvement for a DC source CMLI with reduced number of semiconductor switches is investigated in this paper. The required 31-level output is achieved with only 8 switches in MMC mode. The DC source is considered as the input to the inverter stages. An explained simulation study is carried out for various levels and comparison has been made. In CMLI, the MMC harmonics analysis was compared. Based on these observations, the proposed method provides the multiple advantages which includes reduced THD, less cost, subtle design, less computational complexity and the absence of transformers, boost converters, detailed look-up table and filter circuit. These methods are extremely suitable for standalone/solo/grid interacted PV systems to improve power quality.

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[4] G.Murali Krishna (2012) presented a THD Analysis of Symmetrical and Asymmetrical Cascaded H-Bridge Multilevel Inverters with PV Arrays. Multilevel cascaded H-bridge inverters from five levels to seventeen levels have been simulated using Matlab/Simulink

[5] Anup Kumar Panda, Yellasiri Suresh (2012) proposed a Cascaded Multilevel Inverter (CMI) which employed a single DC source and three phase transformers. Proposed CMI has the attractive features of low 16 switching frequency, increased utilization rate which allowed to achieve high quality output voltages and input currents

[6] Krishna Kumar Gupta, Shailendra Jain (2013) proposed a new multilevel inverter topology which produces additive and subtractive combinations of input DC levels at the output voltage waveform, the actual number of levels depended on the DC source arrangement.