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IMPLEMENTATION OF PARALLEL ADDER USING 180nm AND 45nm TECHNOLOGY IN CADENCE TOOL

Dr Savita Sonoli[1], G Sirisha[2], H M Chandana[3], P G Ambika[4], Shravani S[5]

[1]Vice Principal and HOD, [2] [3] [4] [5]UG Students
Department of ECE, Rao Bahadur Y Mahabaleswarappa Engineering College

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Abstract - *Adders area unit main element used in Digital Signal process (DSP), they are typically used in digital integrated circuits, and vital half in any processor/controller style. Parallel adder may even be a quite common example of combinative circuits and is employed wide in Application Specific Integrated Circuits. Performance of adder circuits extremely affects the general capability of the system. throughout this paper we've a analytic and comparative description of assorted 4-bit parallel adder circuits, considering numerous constraints like power consumption, speed of operation (delay) and space. The circuits area unit designed at intervals the virtuoso platform, exploitation cadence with the GPDK-180nm and 45nm tool. The 4-bit Parallel adder circuits with the twenty eight semiconductor, sixteen and ten transistor in each 180nm and 45nm area unit with success designed, simulated and compared for numerous parameters like power consumption, speed of operation (delay) and space (transistor count).*

***KeyWords*- Cadence, Virtuoso, GPDK-180nm and 45nm, Area (Transistor Count), Power Consumption, Speed of operation (Delay), Parallel Adder.**

1. INTRODUCTION

Addition (Summation) is that the basic arithmetic operations and employed in VLSI systems as a full adder extensively. Full adder is that the adder that adds three inputs and produces two outputs. The first 2 inputs square measure A and B and third input is carry as Cin. The output carry is meant as do and traditional output is selected as S that is add. The full adder circuit performance hooked in to the approach for coming up. The speed of operation of a circuit is indirectly found with the help of delay time calculation that directly depends on the junction transistor count, the logic depth and different criteria. The four bit parallel adder circuits square measure designed, within which junction transistor count varies from twenty eight to a minimum of ten transistor(i.e., 28t, 14t, 10t).The designed 4bit parallel adder circuits have their own benefits and downsides. Hence the most objective of this project is to scale back power, delay and will increase the steadiness issue of a parallel adder by using varied 1-bit full adder styles and techniques and eventually tabulate an equivalent to conclude the most effective style that suites the designers Specifications. The adders square measure designed and enforced within the virtuoso platform exploitation Cadence 180nm and 45nm tool.

DESIGN METHODOLOGY

A parallel adder is associate degree arithmetic combinatory logic circuit that's wont to add over one little bit of knowledge at the same time.A full adder adds 2 1-bits associate degreed a carry to convey an output. However, to feature over one little bit of knowledge long, a parallel adder is employed.

A parallel adder adds corresponding bits at the same time victimization full adders.at the same time, it keeps generating a carry and pushing it towards subsequent most vital bit to be more. associate degree n-bit parallel adder uses n full adders connected in cascade with every full adder adding the 2 corresponding bits of each the numbers.

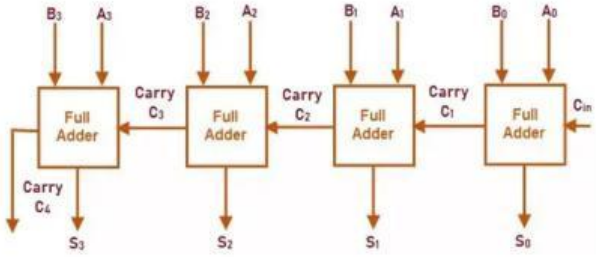


Fig: Diagram of 4-bit parallel adder

Full adder

SYMBOL

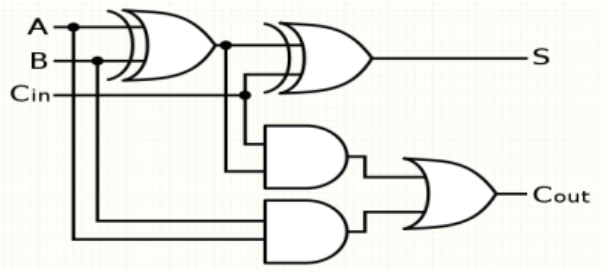
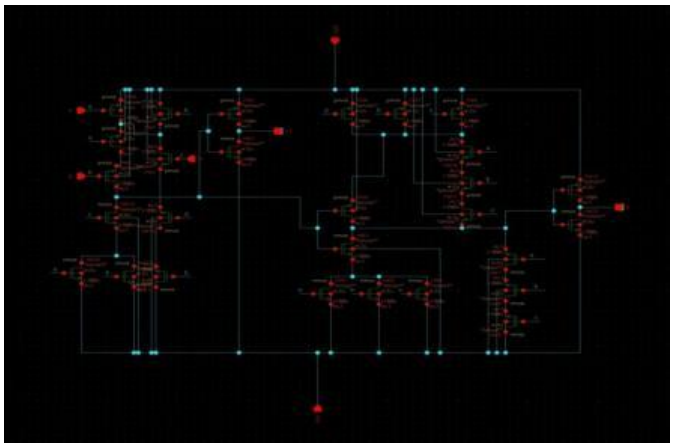


Figure: Logic Symbol of Full Adder

Table: Truth Table of Full Adder

A	B	C	SUM	CARRY OUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Schematic of 1 bit Full Adder using 28 transistors



Full adder is that the adder that adds 3 inputs and produces 2 outputs. the primary 2 inputs are A and B and third input is an carry as Cin .the output carry is meant as perform and traditional output is selected as sum. A full adder logic is meant in such a fashion which will take eight inputs along to form a computer memory unit wider adder and cascade the carry bit from the reality table full adder logic are often enforced, the output S is AN EXOR between the input A and also the 0.5 adder add output with B The perform is high only 2 out of the 3 inputs ar high.

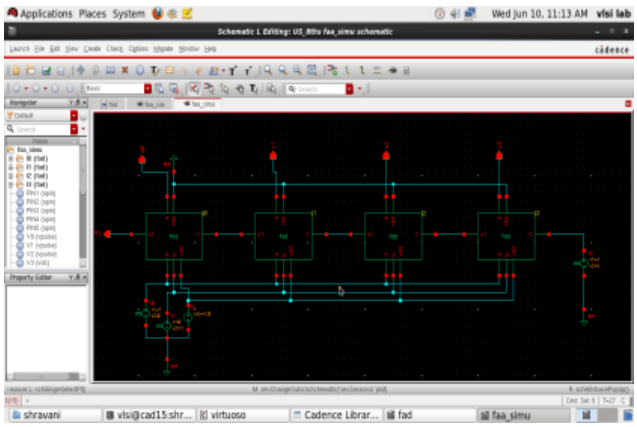
A full adder circuit is enforced with the assistance of 2 [*fr1] adder circuits .the primary [*fr1] adder are accustomed add A and B to provide a partial add.

The adder logic is accustomed add Cin to the add made by the primary half adder to induce the ultimate S output. If any of the [*fr1] adder logic produces a carry, there'll be Associate in Nursing output carry.

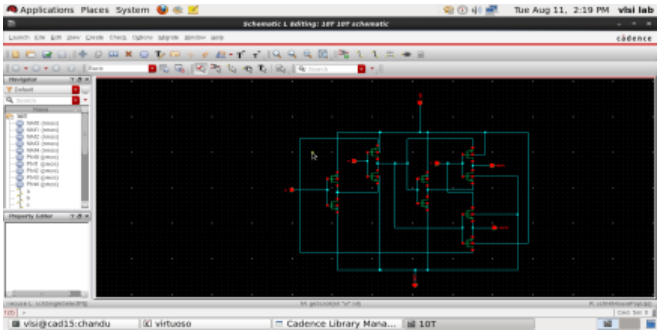
SUM=A XOR B XOR Cin

Carry_ out=AB +BCin + CinA

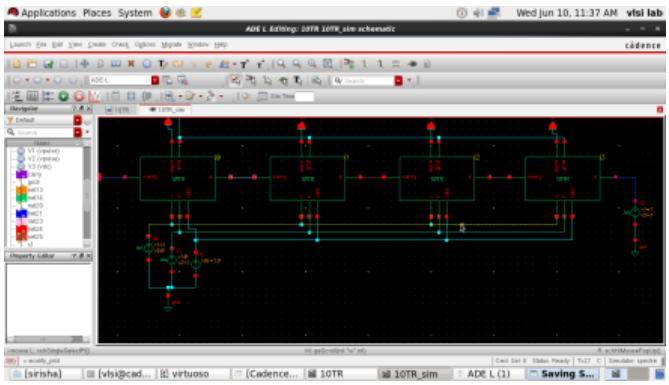
4-bit parallel adder using 28 transistors



Schematic of 1-bit full adder using 10transistor



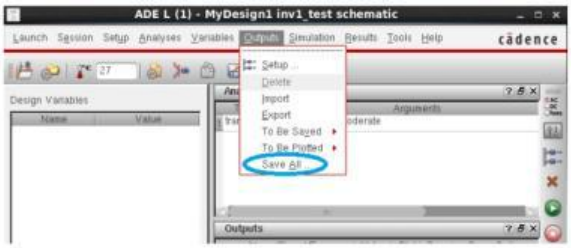
4-bit parallel adder using 10 transistor



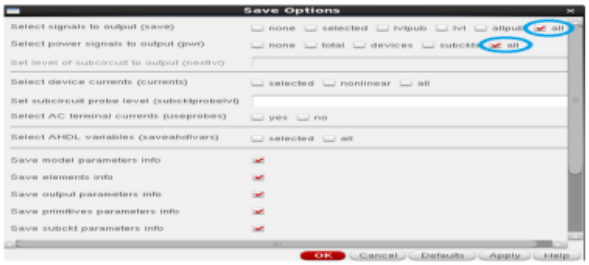
Power Calculation

Steps for power calculation

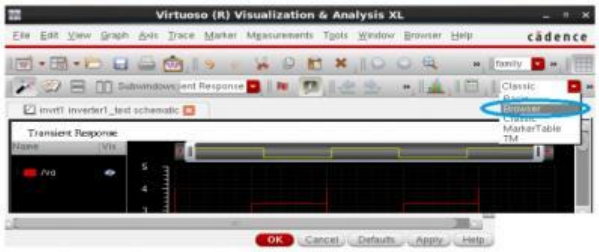
1. From ADE window, Select option Save All under Outputs



2. New window will get, corresponding to Select signals to output (save) and Select power signal to output select option all and give ok



3. In Waveform window change workspace from Classic to Browser



4. In waveform window left side Browser window will come

4. Double click tran option for power signal come as pwr, you can drag and drop it to waveform window so that power graph will get

4. The graph will come in window.

Delay calculation

Steps for delay calculation

1. The calculator window appears.

2. From the functions choose delay, this can open the delay knowledge panel.

3. Place the pointer within the text box for Signal1, choose the wave button and choose the input undulation from the undulation window.

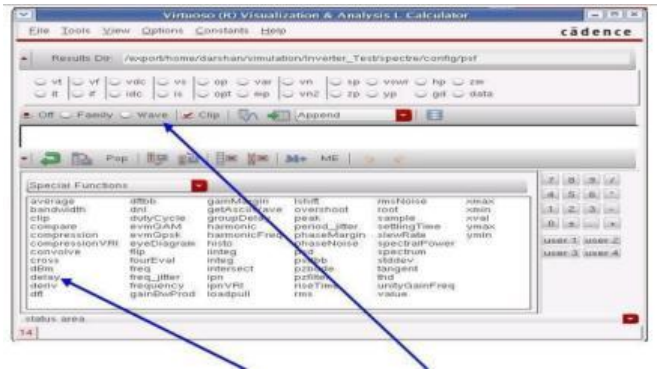
4. Repeat a similar for Signal2, and choose the output undulation.

5. Set the brink worth one and Threshold worth a pair of to zero.9, this directs the calculator to calculate delay at five hundredth i.e.

6. Execute ok and observe the expression created within the calculator buffer.

7. Click on Evaluate the buffer icon to perform the calculation, note down the value returned after execution.

8. Close the calculator window.



RESULT AND DISCUSSION

OUPUT WAVEFORMS:

Waveforms of 180nm technology

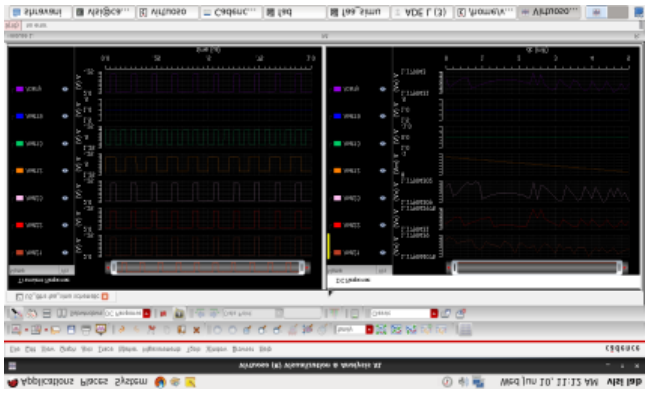


Fig: output waveform of 4-bit parallel adder using 28t

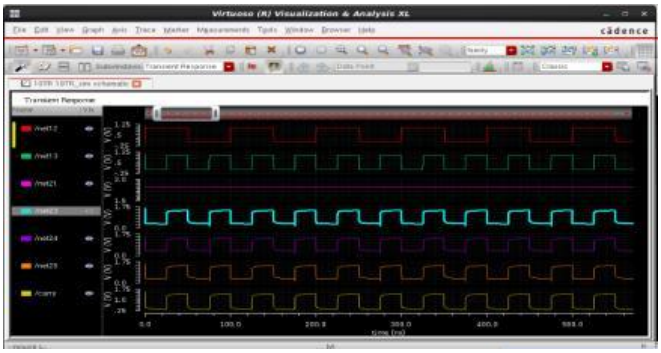


Fig: output waveform of 4-bit parallel adder using 10t

Waveform of 45nm technology

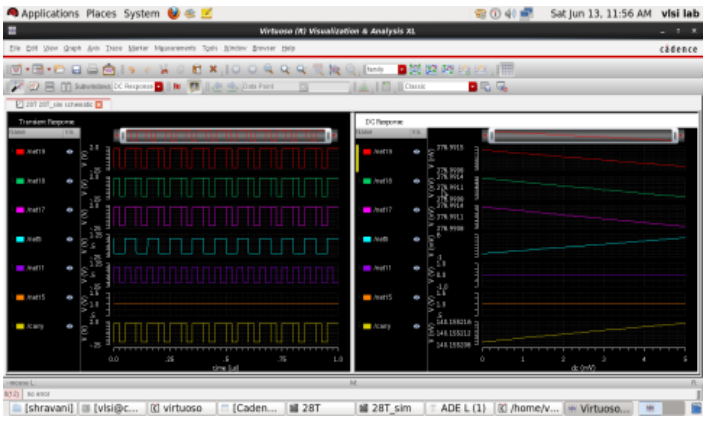


Fig: output waveform of 4-bit parallel adder using 28t

Fig: output waveform of 4-bit parallel adder using 10t

Table: Comparison of 4-bit parallel adder

DESIGN	TRANSISTOR COUNT	DC POWER	DELAY
4-bit parallel adder in 180nm technology	28	3.72uW	5.2ps
	10	2.12uW	3.4ps
4-bit parallel adder in 45nm technology	28	1105nW	22ps
	10	575.5nW	11ps

ADVANTAGES, LIMITATIONS AND APPLICATONS

ADVANTAGES

1. High speed, thanks to the tiny node capacitances.

2. Low power dissipation , as a results of the reduced variety of transistors.

3. Lower interconnection effects thanks to a tiny low space.

LIMITATIONS

1. Design of Parallel adder gets more complicated for more than 4-bits.

2. Each adder has to wait for the carry which is to be generated from the previous adder in chain.

APPLICATONS

1. Parallel adder used in IC design.
2. Digital signal processing.
3. ALU design.
4. Computer memories, CPUs.

CONCLUSION AND FUTURE SCOPE

CONCLUSION:

In VLSI design, the performance of any circuit is limited parameters such as power, delay and area. In 4-bit parallel adder as the transistors count is decreased the power consumption and delay will be less and the area consumed will be reduced. The 4-bit parallel adder is evaluated and compared in both 180nm and 45nm technology based on power and delay factors.

FUTURE SCOPE:

The Parallel adder is designed for 4-bit and results are evaluated and compared with parameters like power and delay. The work can be extended to 8-bits, 16-bits and 32-bits. The new structure can be designed in order to reduce the power and delay of circuits.

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