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IMPLEMENTATION OF HIGH SPEED MULTIPLE CONSTANT MULTIPLICATION TECHNIQUE FOR CONVOLUTION CIRCUIT

[1]MASEED FARHANA, [2]SHAIK NANNU SAHEB

[1]PG Student, Dept. of ECE, Universal College of Engineering & Technology, Dokiparru, Guntur, AP, India
[2]Asst. Professor, Dept. of ECE, Universal College of Engineering & Technology, Dokiparru, Guntur, AP, India

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Abstract - *A variable can be often multiplied by a given set of fixed-point constants employing a multiplier block that consists exclusively arithmetical and logical operations like additives, subtractions and shifts. The generation of a multiplier block from the set of constants is known as the multiple constant multiplication problems. Finding the optimal solution that is the one with the fewest number of additions and subtractions is known to be NP-complete. To propose a replacement heuristic algorithm for the multiple constant multiplication problem, which finds solutions that need less arithmetical and logical operations in a convolution circuit than the solutions found by the simplest previously known algorithm. At the same time, multiple constant multiplication is not limited by the constant bit widths, in contrast to the closest competing algorithm. Designing of a convolution circuit constraints like less silicon area high speed and minimal power consumption. To present this technique by employing a unifying formal framework for the simplest, graph-based multiple constant multiplication algorithms and supply an in-depth runtime analysis and experimental evaluation.*

***Key Words*: Multiple Constant multiplication, Heuristic algorithm.**

1. INTRODUCTION

Digital filters plays major role in DSP, due to its advance performance is one of the key reasons that DSP has become so popular. Filters are used for two process, signal separation and signal restoration. Signal separation is needed when a signal have distorted with interference, noise, or other signals. Signal restoration is used when a signal has been distorted in some way. Digital filters can be implemented in two ways, by convolution (also called finite impulse response or FIR) and by recursion (also called infinite impulse response or IIR).Filters carried out by convolution have good performance than filters used in recursion, but execute much more slowly as the multiplicand has a limited number of values.

From this reason, it is attractive to carry out the multiplication by using shifts and add. The shifts can be realized by using hard-wired shifters and hence they are *essentially free. Furthermore, we can reduce the area of adder by introducing common sub expression elimination CSE techniques. The CSE tackles the multiple constant multiplications (MCM) problem by minimizing the number of additions through extracting common parts among the constants represented in a canonical signed digit (CSD).*

2.*Existing System*

In FIR filter, the multiplication operation is performed between one common variable and many constants (the coefficients) and known as the multiple constant multiplications (MCM). The algorithms that are introduced before is to implement this MCM for an efficient FIR filter design can be categorized in two main groups: 1) graph based algorithms and 2) common sub-expression elimination (CSE)algorithms. Most of these graph based or CSE algorithms presented earlier are used to obtain efficient FIR filter architecture by running the algorithms on a particular set of coefficients for some time on a highly efficient computing platform. We discuss the derivation of MCM units for transpose form block FIR filter, and the design of proposed structure for fixed filters.

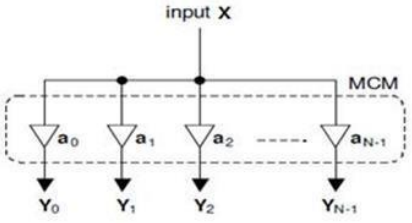

Figure 2.1 Block Diagram of Multiple Constant Multiplications

The multiplications are required to be mapped to the MCM units for a low-complexity realization. In the following, we show that the proposed formulation for MCM-based implementation of block FIR filter makes use of the symmetry in input matrix to perform horizontal and vertical common sub expression elimination and to minimize the number of shift-add operations in the MCM blocks. To illustrate the computation for L = 4 and N = 16. The input matrix contains six-input samples {x(4k), x(4k − 1), x(4k − 2),x(4k −3), x(4k −4), x(4k −5), x(4k −6)}, and multiplied with several constant coefficients, as shown in Table I. As shown in Table I, MCM can

be used for both horizontal and vertical direction of the coefficient matrix. The sample x(4k−3)appears in four rows or four columns of the following whereas x(4k) appears in only one row or one column. Therefore, all the four rows of coefficient matrix are involved in the MCM for the x(4k − 3), whereas only the first row of coefficients are involved in the MCM for x(4k). For larger values of N or the smaller block sizes, the row size of the coefficient matrix is larger that results in larger MCM size across all the samples, which results into larger saving in computational complexity.

Input sample	Coefficient Group
X(4k)	{h(0),h(4),h(8),h(12)}
X(4k-1)	{h(0),h(4),h(8),h(12)} {h(1),h(5),h(9),h(13)}
X(4k-2)	{h(0),h(4),h(8),h(12)} {h(1),h(5),h(9),h(13)} {h(2),h(6),h(10),h(14)}
X(4k-3)	{h(0),h(4),h(8),h(12)} {h(1),h(5),h(9),h(13)} {h(2),h(6),h(10),h(14)} {h(3),h(7),h(11),h(15)}
X(4k-4)	{h(1),h(5),h(9),h(13)} {h(2),h(6),h(10),h(14)} {h(3),h(7),h(11),h(15)}
X(4k-5)	{h(2),h(6),h(10),h(14)} {h(3),h(7),h(11),h(15)}
X(4k-6)	{h(3),h(7),h(11),h(15)}

Table 2.1 Input samples used for multiplication

In MCM-based structure for FIR filters for block size L = 4 is shown in for the purpose of illustration. The MCM-based structure involves six MCM blocks corresponding to six input samples. Each MCM block computes the necessary product terms as shown in Table 2.1. The sub expressions of the MCM blocks are shift computed in the adder network to obtain the inner-product output (rl, m), for 0 ≤ l ≤ L − 1 and 0 ≤ m ≤ (N/L) − 1corresponding to the matrix product of (14). The inner-product values are finally added in the PAU of to obtain a block of filter output.

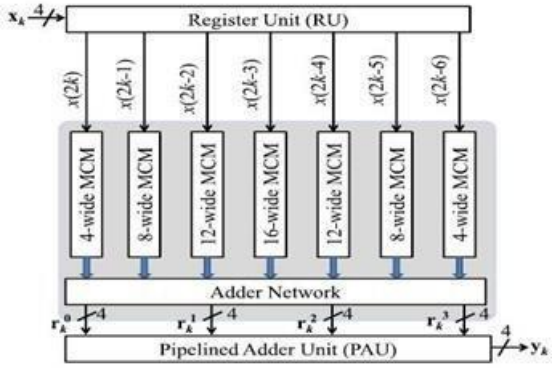

Figure 2.2 Proposed MCM Structure

3.Proposed System

The proposed method has been used for implementing the scheme in that calculates the convolution G ⍰ I between the FP32 kernel vector G and the input vector I of the unsigned integer coded with m bit. The proposed method is used to improve the structure of the k MACs that calculate the product between the generic coefficient of the kernel and the vector of input values.

The resulting architecture is schematized in Once G has been defined, each element of I can be decomposed in n + 1 parts, according to Table I, and stored in an equal number of dual-port read-only memories (ROMs), after they have been pre multiplied by the elements of G. The multipliers are substituted by the n adders in the dashed box of distributed along a log2 (n + 1) depth tree.

In principle, the adders should have FP architecture, but it is possible to adopt a custom coding for partial results, in order to reduce their complexity without altering the accuracy of the multiplication. Starting from the standard IEEE754 FP32 coding [15], all the exponents of the pre multiplied coefficients have been increased to that of the greatest one, while the number of bits of the significant has also been increased accordingly, in order to include the shifted codes and avoid truncations.

Although the proposed method can be employed in conjunction with several kinds of kernels, as a case study it has been used to implement the Gaussian filter with kernel G(x, σ) = Ae−(x2/2σ2) for its large diffusion in image and video elaboration flow Owing to its separability property, for which a 2-D filter can be separated in two consecutive 1-D products [3], [18], the filter implementation in the space–time domain is typically preferred to the frequency conversion. Results from Section II allow partitioning I by using the first n +1= log3 2(28 − 1)+1=6 parts from Table I

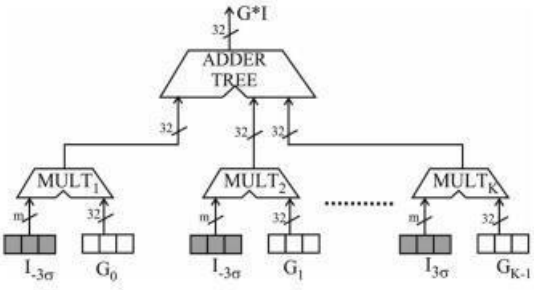

Figure 3.1: Scheme of the Convolution circuit used as case study of proposed decomposition method

In particular, all the n inner products Gjλi are pre computed for each value of I in the range [0;255], for every kernel coefficient, since Gj remains constant once σ and K have been defined. Given that the kernel length can be imposed with K = 6σ + 1 points with good accuracy [3] and that, for the Gaussian symmetry, it is possible to store only 3σ + 1 values, (6) can be implemented by the scheme in Fig. 2. The input I is used to access the ROMs that, in principle, are sharable by all the multipliers. Outputs from the C-ROMs provide the signals to select the inputs to the first adder's row of multipliers.

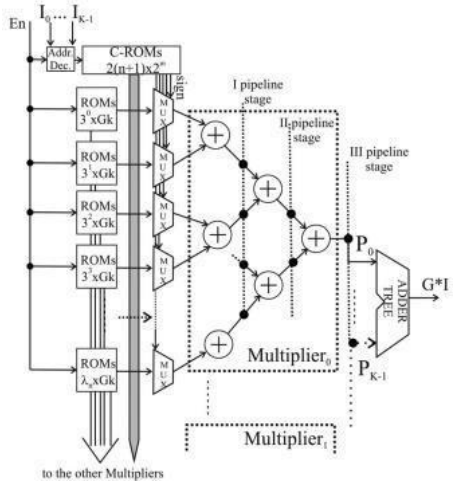

Figure 3.2: Scheme of the proposed multiplier, deployed in a Gaussian convolution

The advantages of the proposed solution become relevant when a large number of multipliers are required. In the implementation reported in the next section, with m= 8 and σ= 4, 25 MACs are required for a full-parallel circuit; thus, using the radix-3 proposed method, it is possible to save 50 adders with respect to the radix-2 DA. Considering also that the memory is sharable between all the MACs, for implementing filters with typical kernel dimensions, the proposed solution proves to be advantageous when compared to a conventional radix-2 DA.

4. RESULTS

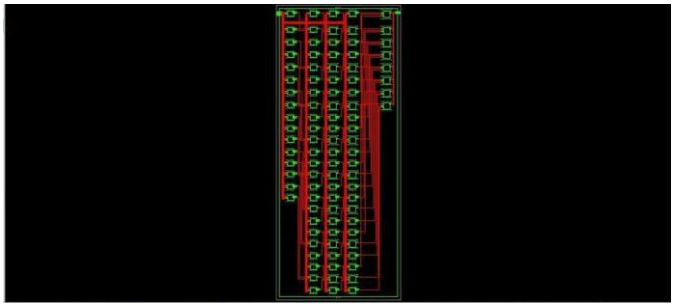

Figure 4.1 RTL of Existing system

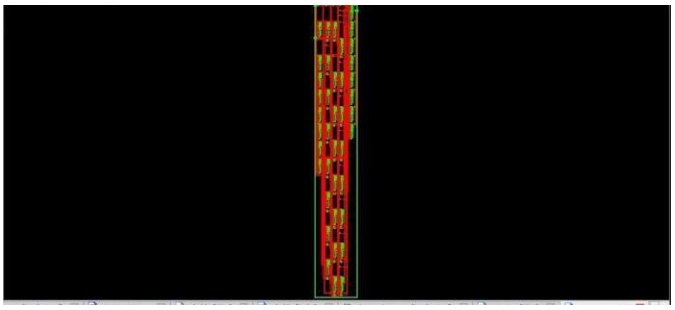

Figure 4.2 Technology Schematic of the existing system

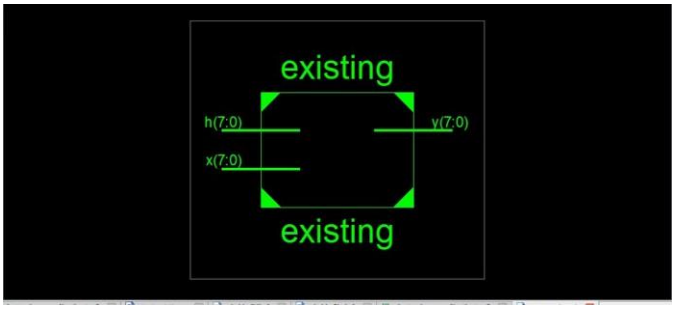

Figure 4.3 Block diagram of existing system

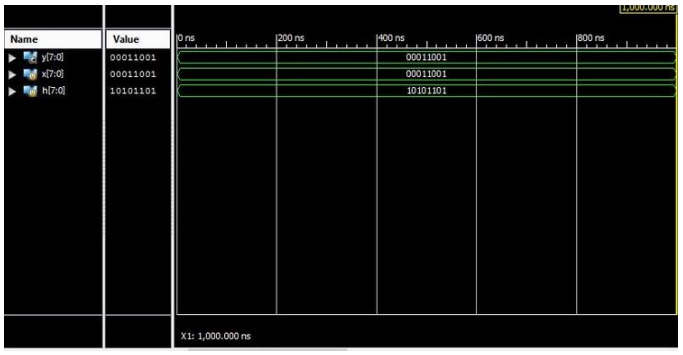

Figure 4.4 Simulation result of the existing system

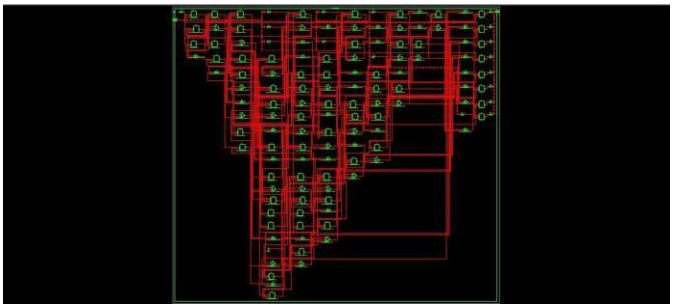

Figure 4.5 RTL of Proposed system

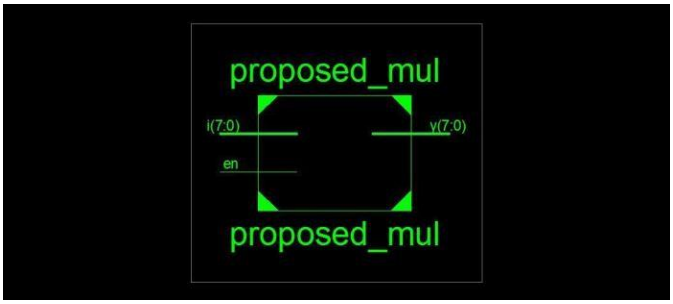

Figure 4.6 Block diagram of proposed system

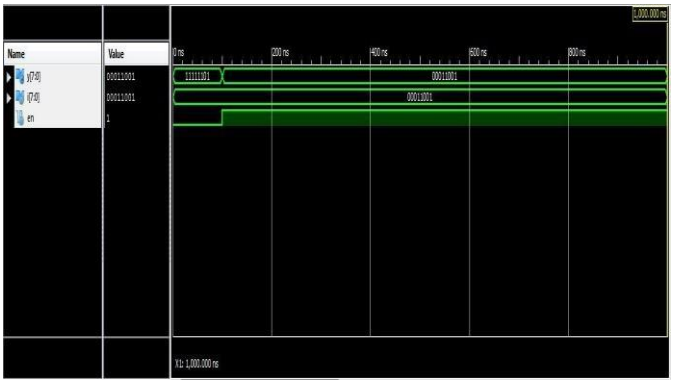

Figure 4.7 Simulation results of proposed system

5. CONCLUSION

In this succinct, an effective term-driving plan has been appeared, that permits executing the hardware for convolution administrators, normally utilized in Filters, without multipliers, encoders. These are completely supplanted by streamlined adders and ROMS for putting away pre-multiplied coefficients. The proposed arrangement gets best in class exhibitions. The outcome is well reasonable for the utilization of multi constant multiplication methods, with a specific end goal to additionally diminish the circuital topology diminish the circuital topology.

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