

# Implementation of Bit Interleavers Used in Flexible Modulation Scheme

Rashmi.S<sup>1</sup>, Ramya.M.S<sup>2</sup>, Haritha.K<sup>3</sup> Students  
Saleem S Tevaramani<sup>4</sup> Assistant professor

<sup>1-4</sup>Dept. of Electronics and Communication Engg., K S Institute of Technology, Bangalore, India

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**Abstract—** In satellite communication, the data transmitted by the satellite must be accurately received by the base station and commands must be sent to the satellite for further data transmission and reception. The major concern is that the satellite is available for the base station to receive and transmit data only for a short duration of time. So, the base station must be able to collect the maximum amount of data in the short interval of time. To collect maximum data at a shorter period the base station must use a higher modulation scheme. This paper presents the implementation of bit interleavers in serial concatenated convolution coding scheme. The modulation scheme is flexible, it can be changed from QPSK, 8PSK, 16APSK, 32APSK till 64APSK. As the input data rate is varied the modulation scheme can be changed to adjust to the input data rate.

**Index Terms—** convolution coding; bit interleaver; puncturing; row-column interleaver; serial concatenated convolution coding

## I. INTRODUCTION

The purpose of this paper is to define an efficient and comprehensive coding modulation solution to support a wide range of spectral efficiency values and data rates. We make use of a set of a large variety of modulation techniques (including QPSK, 8PSK, 16APSK, 32APSK, and 64APSK) and a wide range of coding rates. Presently, the highest modulation scheme used is 32APSK. So, the proposed system uses the 64APSK modulation scheme which provides better and faster data transmission along with reduction of noise in the channel. Also, there is flexibility to change the modulation scheme according to change in the data rate. The modulation scheme can be changed from QPSK to 8PSK, 16APSK, 32APSK and 64APSK where APSK stands for Amplitude and Phase Shift Keying. Amplitude and phase-shift keying or asymmetric phase-shift keying (APSK) is a digital modulation scheme that conveys data by changing, or modulating, both the amplitude and the phase of a reference signal (the carrier wave). In other words, it combines both amplitude-shift keying (ASK) and phase-shift keying (PSK) to increase the symbol set. As the input data rate is varied the modulation scheme can be changed to adjust to the input data rate. A lower modulation scheme can be used if there is disturbance in the channel because if a higher modulation scheme is used during disturbance in the channel, then there is loss of data bits. The bandwidth and power

restrictions in the previous modulation schemes is overcome by using a higher modulation scheme such as 64APSK. Here, we make use convolution encoder for encoding of the input data. The input data is passed to the encoder whose output is 2 bits for every 1 bit input. This encoded data is passed through puncturing system to remove some of the parity bits. These parity bits are removed to achieve the required data rate. Later, the data is passed through the bit interleaver. Interleaving is done to reduce the effect of errors. Finally, the data is stored in row-column interleaver which is used as a buffer. In this way, the bit interleaver used in flexible modulation scheme is implemented. The number of different modulation schemes available, combined with a properly selected coding rate, allows the overall system to make efficient use of the available bandwidth, adapting itself to the variable conditions of the link. The outputs of the binary encoders are mapped to the considered modulation scheme, after being interleaved. In other words, a bit interleaved coded modulation scheme is proposed. This architecture simplifies the synchronization procedure, thus further allowing fast and efficient acquisition at very high rates for the receiver.

## II. PRINCIPLE

Giri S. D et al. [1] presents the design of the structure of Convolutional code to reduce the influence from multi path and channel noise is proposed. The main aim is to focus on the performance analysis of convolution encoder based on FPGA. Such a system can do flexibility relevancy ever-changing information rates, increasing vary, and increasing diversity, whereas giving economical resource utilization. This design is capable of transmitting data, in air errors and noise are tried to be minimized by using channel coding technique. The data speed can be increased by using different combinations of encoding and modulation techniques.

Hu Y., Fonseka J et al. [2] proposes the constrained interleaving based on a row/column structure to improve concatenated codes by maintaining a high MHD and a high interleaver gain. Constrained interleavers are used in constrained turbo product codes (CTPCs) and constrained turbo block convolutional (CTBC) codes. The constrained interleaver delivers an interleaver gain close to uniform interleaving while also increasing the minimum Hamming distance (MHD).

Shou-Sheu Lin et al. [3] proposes a performance enhancement interleaver design method for the generic interleaver. Using distance spectrum as the BER performance prediction tool, these methods provide a systematic way to generate finite interleaver sequences candidates so that the design complexity is reduced dramatically. Performance improvements are also obtained for all the considered interleavers.

Vidya Sawant et al. [4], presents a novel method of Encrypted Structured Random Interleaver (ESRI) provides encryption in addition to shuffling. The conventional interleavers of Turbo Code (TC) provides the required permutation to the information bits and achieves a near Shannon limit Bit Error Rate (BER) performance. The secret key of ESRI determines the shuffling pattern and allows only the authorized users to recover the correct information. Conventional interleavers provide a tradeoff between spread factor and dispersion. The objective of the proposed ESRI is to simultaneously provide a spreading factor larger than the random interleaver and dispersion larger than a deterministic interleaver required for better Bit Error Rate (BER) of TC. The results depict a superior performance of ESRI amongst various interleavers under investigation.

Jyoti Sharma et al. [5], presents the analysis of the interleaver types and a comparative analysis of the principal types of interleaver is done for better bit error rate (BER) performance in linear turbo equalizer using Maximum A-Posteriori (MAP) algorithm. Through the simulation, it is verified that for high SNR, and hence for low bit error (BER), Block interleaver attains better performance than other interleavers for frame size of 1024 bits, and constraint length,  $K=320$ , when using puncturing. The interleaver plays a vital role in the performance improvement of turbo codes used for linear turbo equalizer. In this paper, bit error performance (BER) comparison of various types of interleaver using Maximum A-Posteriori (MAP) algorithm is presented, which shows Block interleaver gives better performance in comparison to other interleavers for 1024 bits frame size and constraint length,  $K=320$ , using puncturing.

Shin Jihwan et al. [6] proposes the performance improvement in concatenating coding scheme compared to not concatenating coding scheme in the correlated Rayleigh fading channel. The paper presents the consideration of a concatenated coding scheme which consists of the tail-biting convolutional code as an inner code and the hamming code as an outer code. They are separated by a block interleaver. The size of the row of the block interleaver is fixed to the length of the codeword of the hamming code. The interleaving depth, the size of the column of a block interleaver is selected based on the burst error statistics of the outer convolutional code. It is assumed that the channel is correlated discrete Rayleigh fading channel which is modeled by using FSMC (Finite-State Markov Chain). The simulation results show that the

BER (Bit Error Rate) performance improvement of the convolutional code with the Hamming code.

Yunlong Zhao et al. [7], presents a class of convolutional error-correction codes (ECCs), spatially coupled protograph low-density parity-check (SC-PLDPC) codes with a sufficiently large coupling length can approach the channel capacity under belief propagation (BP) decoding. However, such codes suffer from poor performance in the case of small coupling lengths. To address the above weakness, the optimization and analysis of SC-PLDPC-coded bit-interleaved coded modulation (BICM) systems over Rayleigh fading channels is performed. Specially, inspired by the unequal-error-protection (UEP) mechanism of M-ary phase-shift keying/ quadrature amplitude modulation (M-PSK/QAM), a novel interleaver design scheme, referred to as spatial position match mapping (SPMM) scheme is proposed. Based on the mutual information (MI) analysis, the proposed interleaver can be used to significantly boost the performance of the SC-PLDPC codes in BICM systems.

S.D. Giri et al. [8], focuses on performance analysis of convolution encoder based on FPGA. With the big quantity of applications now a days, that use digital communication to store and retrieve data, this information should sent and received with smallest errors. Forward Error Correction (FEC) schemes unit a necessary an area of wireless communication systems. There square measure several styles of cryptography techniques accustomed correct utterly totally different error. Convolution secret writing methodology, an honest technique used for correcting errors that occur throughout data transmission.

Youssef Ould-Cheikh-Mouhamedou [9], presents a simple and efficient method for lowering the error floors of turbo codes. This method identifies a set of parity bits that will be forced to take zero bit values when encoding, and exploits these known zero bit parities when decoding.

Francisco J. Escribano et al. [10], presents the well-known property that turbo-like systems owe their success to the principle of reducing error event multiplicities rather than just minimizing related error distances. The increasing need of robust wireless communications, over an already crowded air interface, together with the improvements in hardware and signal processing architectures, is opening the way to the exploitation of new coding and modulation techniques.

Ronald Garzon Bohorquez et al. [11], a method to design channel interleavers based on span properties and mutual information is presented. Resulting interleavers enjoy better burst error control and c mitigate the effect of regular error patterns. For channel interleaving, structures are generated, resulting from a joint optimization of the interleaver span properties in the time and frequency domains. A significant improvement can be observed in

severe channel conditions, especially over time and frequency selective channels with erasures.

Charbel Abdel Nour et al. [12], it is presented that three of the most common interleaver for turbo codes (TCs) are dithered relative prime (DRP) interleavers, quadratic permutation polynomial (QPP) interleavers, and almost relative permutation (ARP) interleavers. In this paper, it is shown that DRP and QPP interleavers can be expressed in the ARP interleaver function. Furthermore, QPP interleavers can be seen a particular case of ARP interleavers, in which values of the periodic shifts follow the quadrant term of the QPP interleaver function.

Yuta Hori et al. [13], it is presented that bit-interleaved coded modulation (BICM), together with orthogonal frequency-division multiplexing (OFDM) signaling, has found its application in many recent wireless standards. BICM-OFDM systems are able to simplify the design of coding and modulation with various information rates for link adaptation.

Manish Yadav et al. [14], it is presented that one of the most popular and effective method adopted for the burst error control is to perform the interleaving operation before the transmission of data over a communication channel. In order to distribute the burst errors, interleaver shuffles the sequence of original message bits. At the receiving end, the received message bits are re-shuffled to recover the message bits in its original sequence. Thus, the selection and designing of appropriate interleavers for an advanced multiple-access technique such as interleaved-division multiple-access (IDMA) is always a key challenge.

Palle Prasanth Kumar et al. [15] provides the design of a Turbo Encoder, which is parallel concatenation of Recursive Systematic Convolutional (RSC) encoders and interleaver to reduce delay. The Turbo Encoder is designed by Verilog-HDL and Synthesized by Xilinx ISE. Further its performance is analyzed through evaluation of metrics such as area and delay. The Turbo Encoder is designed using Verilog-HDL and simulated using Xilinx ISE 14.7, by considering 8-bit input stream and 16-bit input stream. It is observed through the simulation results that the Turbo Encoder with 16-bit input stream has utilized more logic and acquired more delay compared to that of Turbo encoder with 8-bit input stream. Further the work can be extended by incorporating Turbo Decoder for various input streams.

### III. BLOCK DIAGRAM

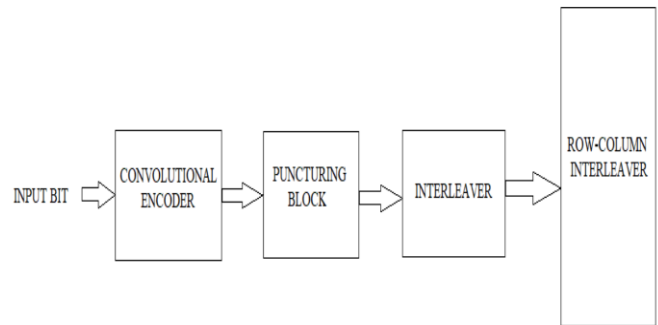


Fig 1: Basic block diagram

The basic block diagram is as shown in fig. 1. The input bit is given to the first block which is the convolutional encoder. The encoder encodes the input bit and produces an output of 2 bits for every input bit. The block diagram of encoder is as shown in fig. 2. These 2 bits are not passed to the puncturing block immediately. After 2 clock cycles, 4 output bits are obtained from the convolutional encoder, that is 2 bits per cycle and then these 4 bits are together passed as input to the puncturing block.

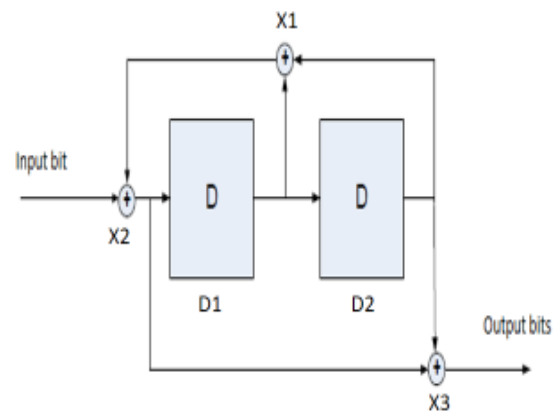


Fig 2: Encoder block diagram

The function of the puncturing block is to remove the parity bits or the redundant bits from the data stream. Puncturing is performed to obtain the required code length and also there is no loss of useful data as some of the redundant bits are only removed. There is a wait for 2 clock cycles to pass the input to the puncturing block as the puncturing block is designed to remove 1 bit for every 4 bits of input data. The output of the channel encoder is subject to puncturing using a puncturing algorithm.

After puncturing 1 bit, the output of 3 bits of the puncturing block are given as input to the interleaver block. The functionality of the interleaver block is to change the position of the bits of the data stream in a predefined order. This operation is performed on the input bits, because the data received from the satellite at the



earth station is not in the order as it was transmitted by the satellite. So, interleaving is a major operation in obtaining the correct form of information at the base station.

Interleaving is the reordering of data that is to be transmitted so that consecutive bits of data are distributed over a larger sequence of data to reduce the effect of errors. Interleaving is a process or methodology to make a system more efficient, fast and reliable by arranging data in a noncontiguous manner. It helps in storage and error correction. The use of interleaving greatly increases the ability of error protection codes to correct for errors.

The data bits are now in the correct order as it was transmitted by the satellite after passing through the interleaver block which is basically a bit interleaver. Then, these data bits are passed to the row-column interleaver which is used as a buffer for storage of the data bits.

The row-column interleaver is used to pseudo randomize the selection of bits. The data is serially written column-wise and serially read row-wise in a row-column interleaver as shown in Fig 3.

Finally, after storing the data in the row-column interleaver the entire block diagram is implemented at the hardware level by using the Spartan fpga kit. Test bench modules are written to test the functionality and working of each of the blocks.

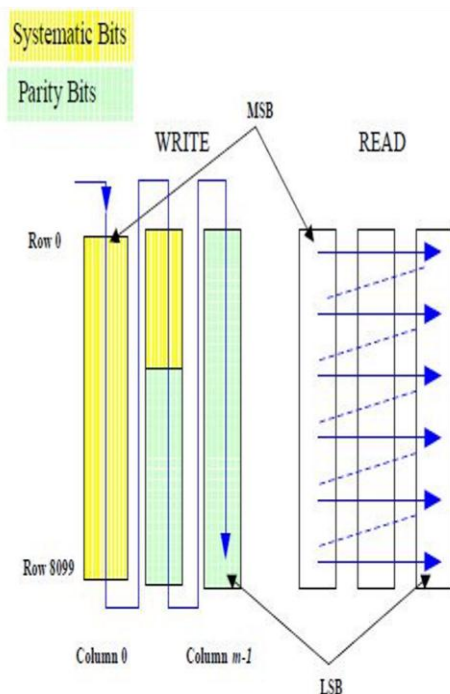


Fig 3: Row-column interleaver

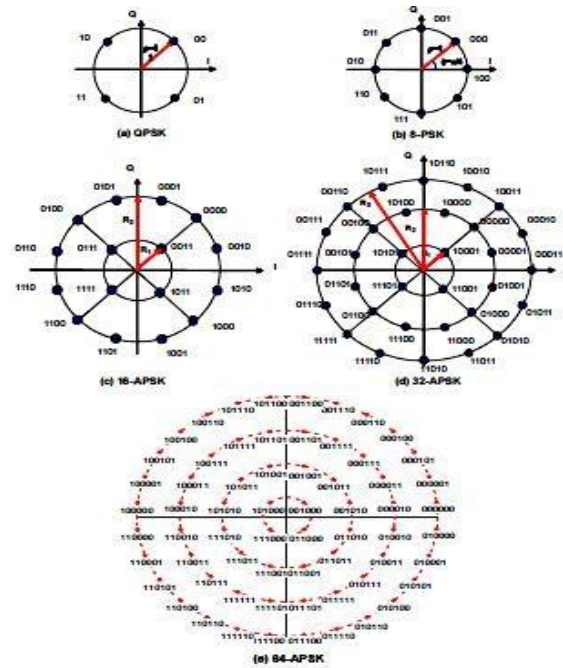


Fig 4: Constellation mapping

In the constellation mapping diagram shown in Fig 4, the 16APSK scheme uses the constellation composed of 2 concentric circumferences, whose number of points shall be set to  $N1 = 4$  and  $N2 = 12$ .

In 32APSK scheme, the constellation is composed of 3 concentric circumferences whose number of points shall be set to  $N1 = 4$ ,  $N2 = 12$ , and  $N3 = 16$ .

In 64APSK scheme, the constellation shall be composed of 4 concentric circumferences, whose number of points shall be set to  $N1 = 4$ ,  $N2 = 12$ ,  $N3 = 20$ , and  $N4 = 28$

#### IV. RESULT

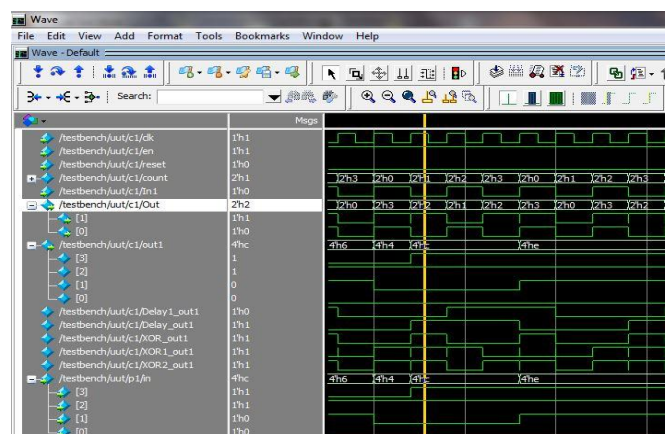


Fig 5: Output of convolutional encoder

The fig 5 shows the output of the convolutional encoder. The output in the first cycle and the output in the second

cycle are together obtained as the final output of the convolutional encoder in the third clock cycle.

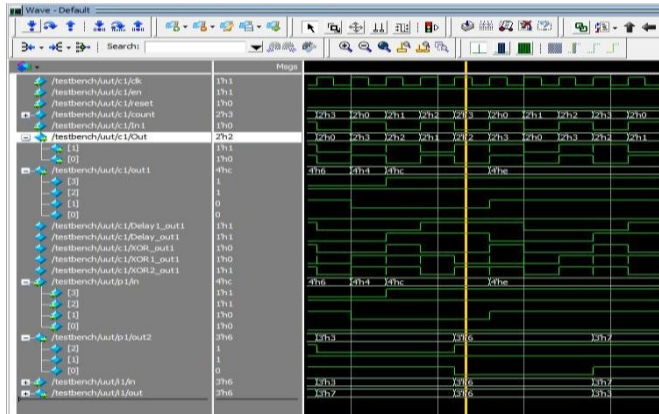


Fig 6: Output of puncturing block

The output of the puncturing block is as shown in fig 6. The input from the convolutional encoder is given as input to the puncturing block. The puncturing block removes the fourth bit for every four bits of input. The fourth bit is the redundant bit or the parity bit. So, even if this bit is removed no useful data is lost from the data stream. Also, by performing the operation of puncturing the desired code length is achieved as some of the parity bits are removed from the data stream.

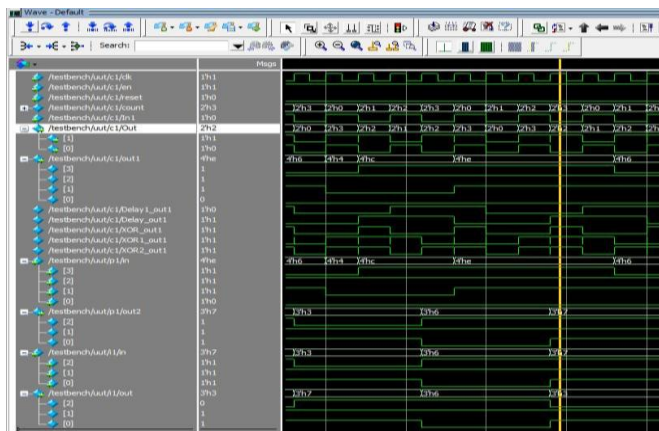


Fig 7: Output of interleaver block

The fig 7 shows the output of the interleaver block. The output of the puncturing block is passed as input to the interleaver block. The interleaver block changes the position of the bits of the data stream so as to obtain the data bits in the correct order.

Bit interleaver used in flexible modulation scheme has been designed. For verification purpose, test data has been generated for all interleaving block sizes using MATLAB. Then, the test data has been applied to the Verilog models and the outputs have been compared to the MATLAB results. Finally, for verification of hardware output, the code will be implemented in the FPGA kit.

**V. CONCLUSION**

By literature review, we have found that the previously used modulation techniques QPSK, 8PSK, 16APSK and 32APSK had bandwidth and power restrictions. So, to overcome the above disadvantage and to get higher modulation, we go for 64APSK. By using 64APSK modulation technique, the error correcting capability can be increased.

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