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Comparative Investigation of 7-level Cascaded Multilevel Inverter using Multicarrier Level Shifted PWM Techniques

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Abstract - This manuscript presents the achieved efforts on 1-ϕ 7-level cascaded H-bridge multilevel inverter. To cheer the quality of 7-level CHBMLI output parameters primarily THD and switching losses, multicarrier level shifted technique is consider for controlling the gate pulse of 7level CHBMLI and the complete analysis of THD for 7-level is done. This work is performed and results are validated using MATLAB/SIMULINK.

Keywords: Multilevel Inverter (MLI), Cascaded H-Bridge (CHBMLI), Multicarrier pulse width modulation technique (MCPWM).

MULTILEVEL INVERTER:

An inverter is a tool that transfers DC to AC, with the use of transformers the rehabilitated AC can be used at any necessary voltages and frequencies. The inverters which have no moving parts are static inverters and are employed in various applications. Industries are now demanding equipments with high powers, of the ranges of megawatt level. Nowadays, it is tough to fix a sole power semiconductor switch directly to medium voltage grids (2.3, 3.3, 4.16, or 6.9 kV). So for higher level of voltage, a new family of MLI has materialized as the way out for functioning. MLI comprise an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. Fig.1 shows a schematic diagram of one phase leg of inverters with different numbers of levels.[12, 13, 15]

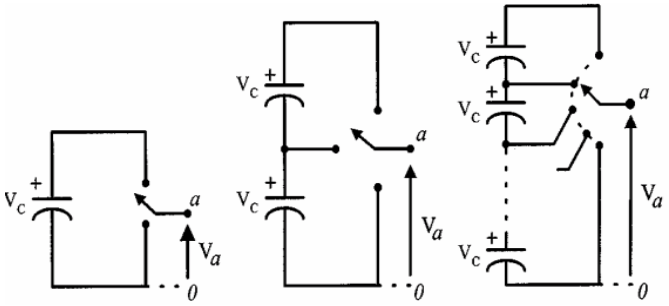

Fig 1: One leg inverters (a) 1-level (b) 2-level (c) n-level

Classification of Multilevel Inverter:

(a) Diode clamped multilevel inverter (DC MLI)

A 3-phase 6-level DCMLI is given away in Fig 2 Each of the three phases of the inverter shares a common DC bus, which has been subdivided by five capacitors into six levels. The voltage across each capacitor is V_{dc}, and the voltage stress across each switching device is limited to V_{dc} through the clamping diodes. This engages the (n-1) main DC link capacitors and also Σ($2n$-2) clamping diodes, where, n is the number of levels [9, 11].

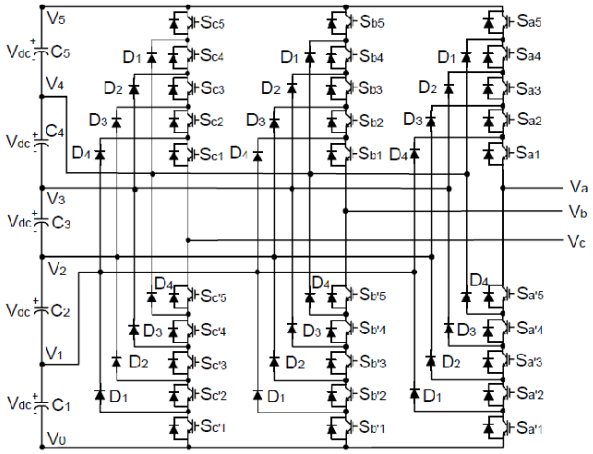

Fig 2: Structure of Three Phase Six Level DCMLI

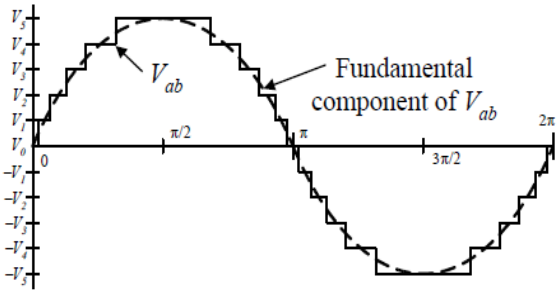

Fig 3: Line Voltage Waveform of Six-Level DCMLI

Advantages and Disadvantages of DCMLI.

(1) **Advantages:**

- All of the phases share a common dc bus, which minimizes the capacitance requirements of the converter.
- The capacitors can be pre charged as a group.
- Effectiveness is elevated for elementary switching of frequency.

(2) **Disadvantages:**

- Real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control.
- The number of clamping diodes required is quadratically related to the number of levels which can be cumbersome for units with a high number of levels.

(b) FLYING CAPACITOR BASED MULTILEVEL INVERTER(FCMLI)

The FCMLI necessitate a big number of capacitors to clamp the device voltage to one capacitor voltage level provided all the capacitors are equal value. An *n*-level inverter will necessitate a total number of (*n*-1)*(n-2)/2 clamping capacitors per phase. Fig 4 demonstrates the 3- phase 6-level FCMLI [10].

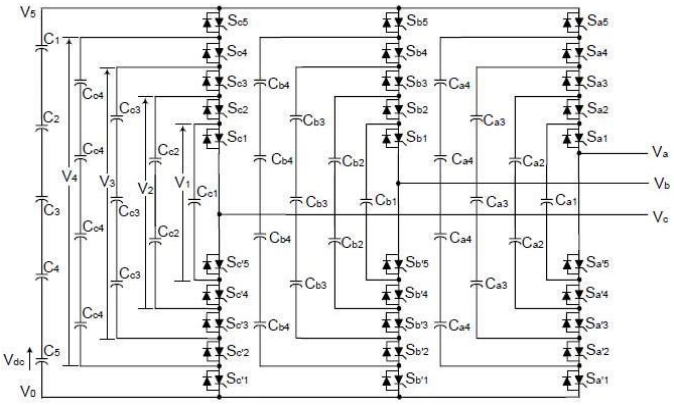

Fig 4: Structure of Three Phase Six-Level Flying Capacitor Inverter.

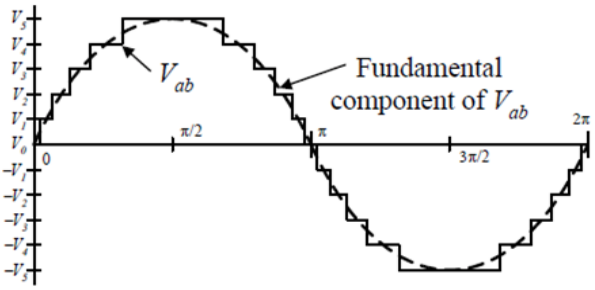

Fig 5: Line Voltage Waveform of FCMLI Based.

Advantages and Disadvantages of FCMLI

(1) Advantages:

- Additional clamping diodes are not required.
- It has switching idleness inside the phase, which can be used to balance the flying capacitors so that only one DC source is desirable.
- The requisite number of level of voltage can be attained with no use of the transformer. This aid in dropping the charge of the inverter and yet again diminish loss of power.

(2) Disadvantages

- Inverter initialization i.e., previous to the converter can be adapted by any modulation method the capacitors ought to be arranged with the obligatory voltage level as the preliminary charge. This makes difficult the modulation procedure and turn out to be an obstacle to the procedure of the converter.
- Organizing is difficult to footpath the level of voltage for every capacitor.
- Pre charging every capacitor to identical level of voltage and bring into being is difficult.

(c) CASCADED MULTILEVEL INVERTER(CHBMLI)

Fig. 6 deprived the basic layout of CHBMLI for single phase. Every splitting voltage source (V_{dc1}, V_{dc2}, V_{dc3}) associated in cascade through additional supply via a unique H-bridge circuit linked through it. Every circuit contains four switches that can create the voltage output source in positive or negative polarity; or it can be simply zero volts depending on the switching condition of the switches in the circuit [1, 2]. The level of output can be given by

$$N_{level} = 2S + 1 \qquad (1)$$

Where, S is the H-bridge

The voltage at every phase can be calculated by

$V_{si} = 1V_{dc} (i = 1,2,3 \ldots)$ (2)

The number of switches used in this topology is given by the equation,

$N_{switch} = 4S$ (3)

The rewards of the CHBMLI are series H-bridges for modularized outline and wrapping. The Fig 7 demonstrates the waveform of voltage output for a 7-level CHBMLI [7, 8].

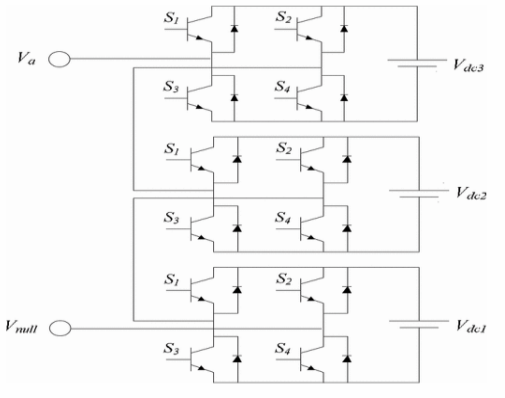

Fig 6: Topology for CHBMLI

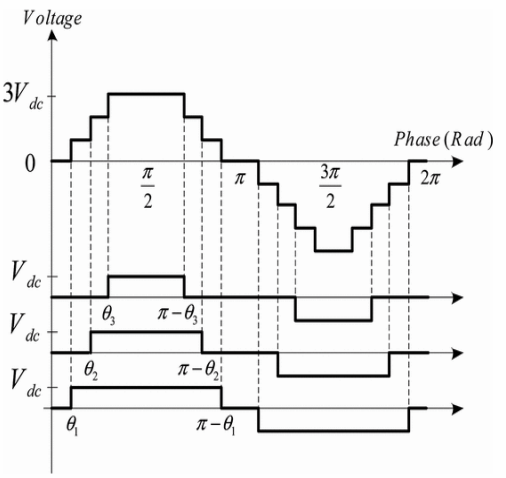

Fig 7: Typical Output Waveform for CHBMLI

Advantages and Disadvantages of CHBMLI.

(1) Advantages

- Very simple to regulate DC busses.
- Modularity of control can be achieved.
- Involve the slightest number of apparatus amongst all MLI to attain the similar number of levels.
- Flexible switching can be used in this arrangement to keep away from hefty and lossy resistor capacitor diode snubbers.

(2) Disadvantages

- Communication between the bridges is essential to accomplish the harmonization of reference and the carrier waveforms.
- Requires splited DC sources for real power conversions, and therefore its purposes are a bit inadequate.

MODULATION TECHNIQUES: Modulation Technique is Low and High switching Frequency fort high switching frequency is considered above 1 KHz [13].

Multicarrier PWM: Multicarrier Pulse Width Modulation Technique is used in three level or more than three levels. These are classified into two types: - Level Shift, Phase Shift.

Level / Vertically Shifted PWM: Level shifted technique is the reasonable addition of sine triangle PWM for MLI, in which *n*-1 carriers are required for *n*-level inverter. They are approved in vertical shifts in constant bands defined by the levels of the inverter [8]. 3(*n*-1) carriers are requisite for 3-phases. Based on managed degrees of liberty grouping, the level shifted PWM is divided into PD, APOD and POD PWM techniques [3, 5, 6].

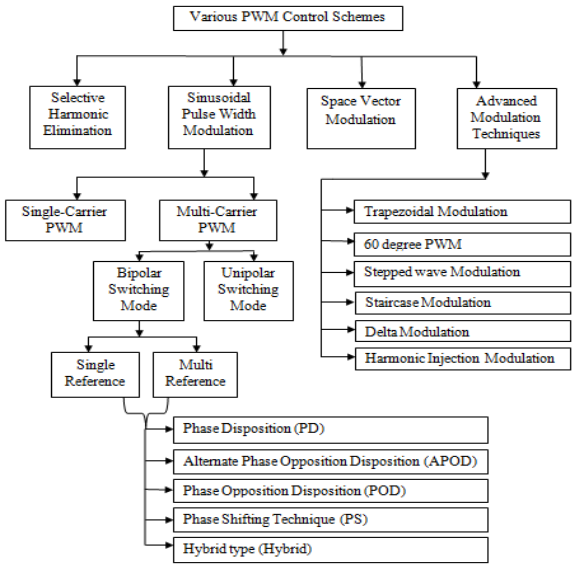

Fig 8: Types of PWM control techniques

Phase Disposition Pulse Width Modulation (PD PWM): The PDPWM with single reference is based on the evaluation of a sinusoidal reference signal with *n*-1 carriers which are vertically shifted. From Fig 11 it can be known that the carriers that have the similar frequency f_c and amplitude A_c are in phase. The modulating signal has a frequency of f_r and an amplitude A_r.

Alternate Phase Opposition Disposition Pulse Width Modulation (APOD PWM): In APODPWM, the contiguous carriers with identical frequency and amplitude are positioned and overlapped and are phase displaced by 180° in a mode as exposed in Fig 13. These carriers are evaluated with single sinusoidal reference wave for the appropriate procedure of CHBMLI.

Phase Opposition Disposition Pulse Width Modulation (POD PWM): The carrier signal with similar amplitude and frequency are in phase over and under the zero reference value. However, as exposed in Fig 15, there is 180° phase

shift flanked by the ones over and under the zero reference. These carriers are overlay with single reference signal to produce the pulses for calculating the switches of MLI.

3. SIMULATION AND RESULTS:

Simulation of Seven Level CHBMLI: 7-level inverter is simulated similar to that of the 5-level inverter. The difference here is the number of carrier signals. Here six carrier signals are employed. Three of them are applied across the positive half cycle of the modulating signal [14]. Remaining three of them are applied across the negative half cycle of the modulating signal. From these signals twelve PWM signals are generated and then given to the eight switches of a leg. Pulses are generated for remaining phases. Here the pulses were generated using various level shifting techniques like PDPWM, PODPWM, APODPWM.

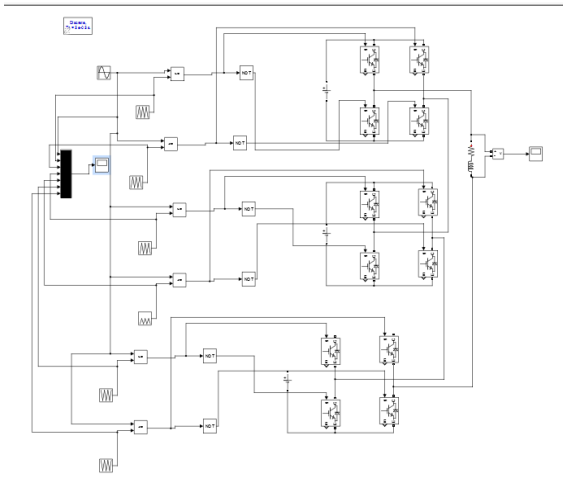

Fig. 9: Simulation for 7-level CHBMLI with PWM technique.

5.3.1 Simulation Results:

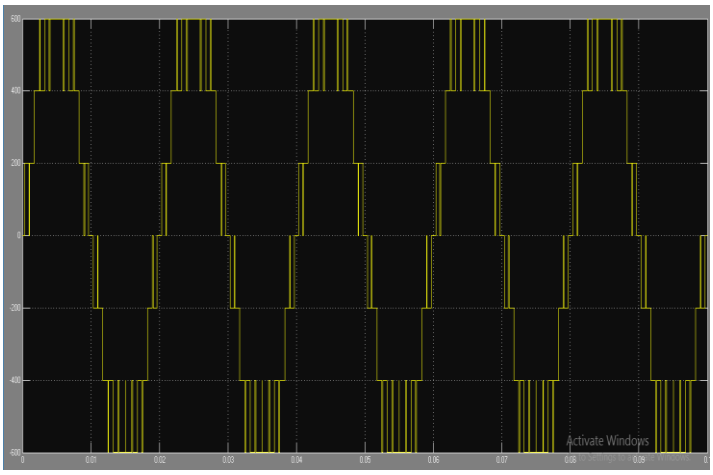

Fig. 10 Output waveform for 7-level CHBMLI.

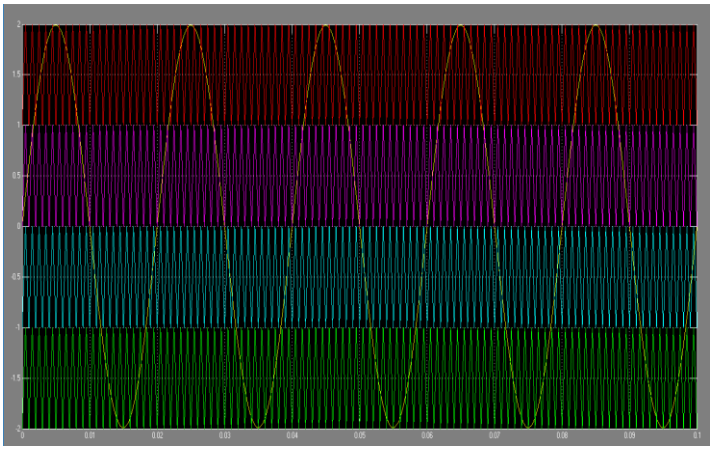

Fig. 11 Carrier arrangements for PD PWM

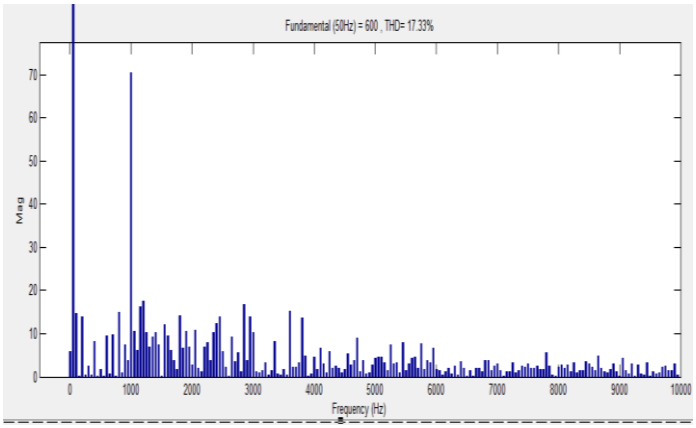

Fig.12 THD for PDPWM technique.

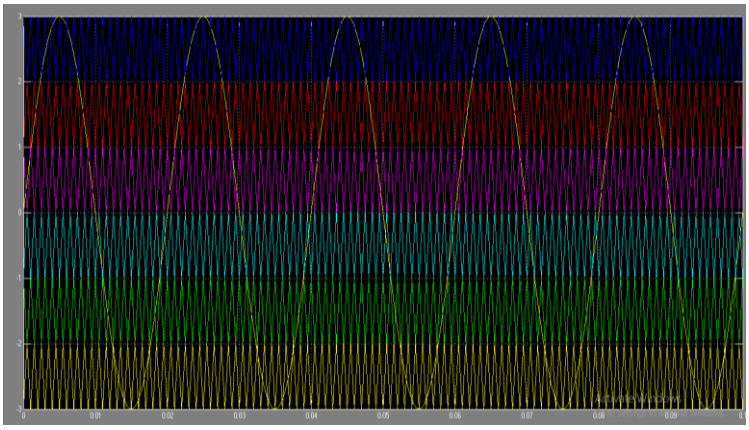

Fig. 13 Carrier arrangements for APOD PWM

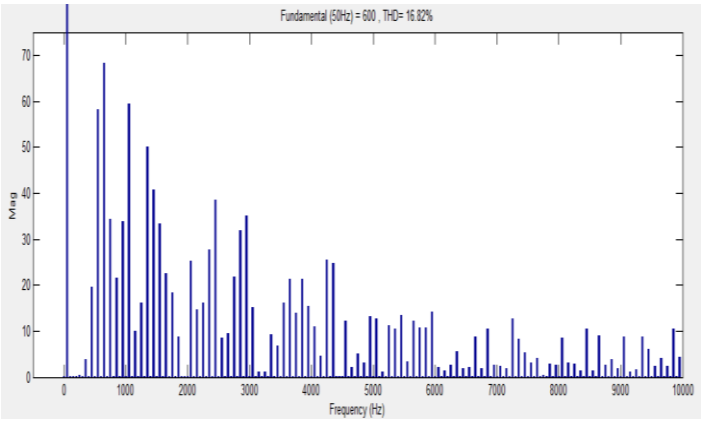

Fig. 14 THD for APODPWM tech.

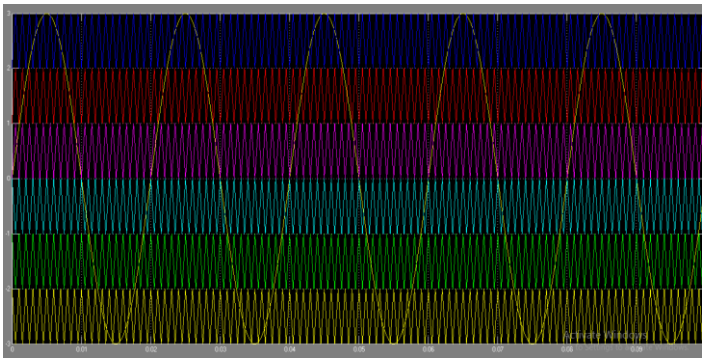

Fig. 15 Carrier arrangements for APOD PWM tech.

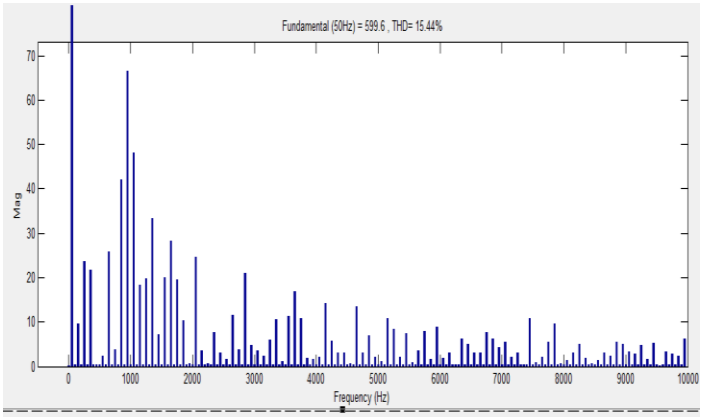

Fig. 16 THD FOR PODPWM

Table 1. THD Comparisons of PWM Technique

S. No.	No. of Levels with technique	%THD
1	7-level PD PWM technique	17.33%
2	7-level POD PWM technique	15.44%
3	7-level APOD PWM technique	16.82%

CONCLUSION:

In this paper has been Discuss the Cascade H-Bridge Topology using Phase Disposition, Phase opposition Disposition, and Alternate Phase opposition Disposition are compared. The three techniques it can conclude that the Phase Disposition Topology is better among the three topologies.

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