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A Review on the Hysteretic Effects on Thin Film Transistors

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Abstract -*A TFT is a special type of MOSFET made by depositing thin films of an active semiconductor layer as well as the dielectric layer and metallic contacts over a supporting (but non-conducting) substrate. Various investigations have shown that hysteresis (a concept of physics where the ferromagnetic substances lag the magnetization behind the magnetic field) effects the current-voltage characteristics of organic TFTs as well as polycrystalline silicon TFT. This paper reviews the origin and consequences of hysteresis on polycrystalline silicon TFT*

***Key Words*: Thin Film Transistors, Hysteresis, Multi Electrode Arrays, Crystallization, Forward Sweep, Reverse Sweep, Threshold, Field Effect Mobilities**

1. INTRODUCTION TO THIN FILM TRANSISTORS

TFTs are basically MOSFET transistors. Their fabrication technology has a history almost as long as that of CMOS technology, but it took several decades before it was mature enough to reach the production level.1) Actually the improvement and development of TFT technology has three aspects: the improvement of the semiconductor layer, the stability of the process for large scale fabrication, and the development of process equipment to produce increasingly large devices. Initially it was mainly the first aspect that limited the rate of the development of this technology. Thin film transistor (TFT) technology is a well-known technology widely used in flat panel displays, computers, smart phones, video game systems and personal digital assistants. This technology has revolutionized video systems, allowing flat panels with increasingly larger dimensions to be obtained: 164 in. is the diagonal dimension of the substrates used nowadays for TFT liquid crystal display (TFT-LCD) fabrication. [1]

The improvement and development of TFT technology has three aspects: the improvement of the semiconductor layer, the stability of the process for large scale fabrication, and the development of process equipment to produce increasingly large devices. Initially it was mainly the first aspect that limited the rate of the development of this technology. This technology was applied from the beginning to TFTLCDs. However, other applications have been investigated in the last 20 years, in areas as diverse as X-ray detection, microelectronic devices (memory), chemical sensing and bio-chemical sensing. In the last field, organic thin film transistors (OTFTs) have played an important role. It is believed that the structure of TFT array substrates fabricated by this technology might make them extremely useful as electroactive substrates for electrical manipulation as well for electrical sensing on biological cells. It is also believed that such substrates might have a wider range of applications than multi electrode arrays (MEAs) realized by more standard microfabrication techniques or by CMOS processing.[1].

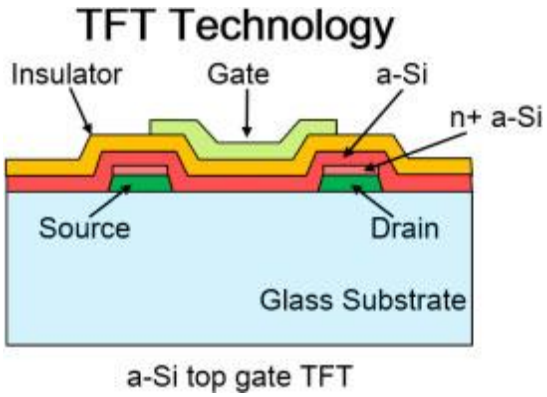


Fig -1: Amorphous silicon top-gate TFT.[1]

2. INTRODUCTION TO HYSTERESIS

One of the most intriguing phenomena examined during studies on energy conversion is hysteresis. The word has a Greek origin, which when translated literally means "to lag behind". It was coined around 1890 by Sir James Alfred Ewing to describe the behavior of magnetic materials. **Hysteresis** is the dependence of the state of a system on its history. For example, a magnet may have more than one possible magnetic moment in a given magnetic field, depending on how the field changed in the past. Plots of a single component of the moment often form a loop or hysteresis curve, where there are different values of one variable depending on the direction of change of another variable.

Hysteresis can be a dynamic lag between an input and an output that disappears if the input is varied more slowly; this is known as rate-dependent hysteresis. However, phenomena such as the magnetic hysteresis loops are mainly rate-independent, which makes a durable memory possible. [2].

The lag between the input and the output signals manifests itself in the occurrence of the so-called hysteresis curve.

Figure 2 describes the hysteresis curve for a soft ferromagnetic material, whose analytical description by itself is a challenging and interesting task both for physicists and engineers. The scientists asked about the most distinctive fingerprint of ferromagnetism might indicate either the existence of the Curie point (the transition from ferro- to paramagnetic regime, important in particular for physicists), or the occurrence of hysteresis loop (interesting for engineers, who design magnetic circuits of electrical machines and devices)[2].

Systems that exhibit hysteresis fall into two categories:

- Systems with **rate-dependent hysteresis** have a memory of recent inputs that fades with time - if the input stops changing and we wait long enough, the output will eventually reach the same value for that particular input.
- Systems with **rate-independent hysteresis** retain a permanent memory of certain input patterns, and even the steady state value of the output depends on the nature of the input history.

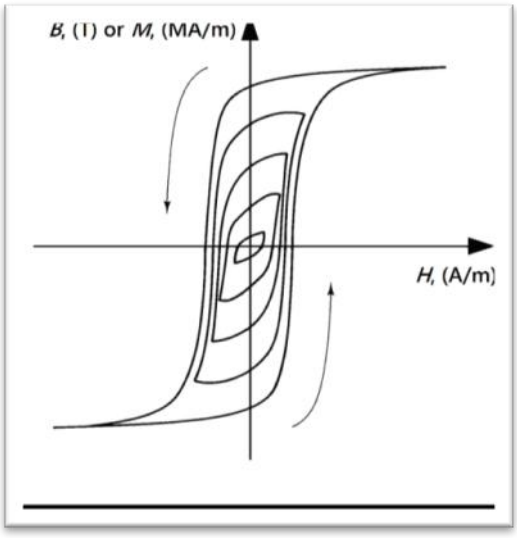


Fig -2: A family of hysteresis loops for a soft ferromagnetic material. The largest loop, exhibiting saturation, is referred to as the major loop.[2]

3. FABRICATION

There are a handful of fabrication techniques for manufacturing of thin film transistors. Let us consider the various processes in fabrication of a poly-Si TFT. These include ion doping technique, fabricating with self-aligned silicide Schottky barrier source/drain (SSD) and low temperature (below 200° C) laser crystallization of Si film. The thickness of poly-Si ranges between 30 to 100 nm. Usually, Si channel is an amorphous layer that is coated at low pressure using the principle of chemical vapor deposition. After n+ poly-Si formation, the source and drain are placed using ion implantation. Such TFTs are top coplanar structures and they are deposited on a glass substrate. Masking approach is used to establish contact cuts and other n+/ p+ diffusion.

Annealing is a common undertaking in metallurgy. It is a heat treatment that is carried out to change the physical and sometimes chemical properties of a material to improves its ductility and to reduce the material's hardness. This method is used after a normal procedure to form metal pads. It is cited that ion shower doping technique makes it easy to synthesise polycrystalline Si TFTs with a CMOS structure using a non-complex apparatus. It is also possible to fabricate large areas easily. Poly-Si find large applications in the market and hence, they are fabricated in mass production.[3]

4. HYSTERESIS EFFECTS

Figure 3. shows the measurement results of transfer characteristics of a-Si:H TFT and poly-Si TFT respectively. The threshold voltage of a-Si:H TFT was altered according to the gate voltage sweep direction. When a gate voltage was increased (forward sweep direction), the threshold voltage was 2.14V while it was 2.55V when a gate voltage was decreased (reverse sweep direction) due to hysteresis of a-Si:H TFT. In this measurement the gate voltage was increased from -10V to 20V with forward sweep direction and it went down from 20 V to -10 V with reverse sweep direction. The hysteresis effect on the current variation of poly-Si TFT was less than that of a-Si:H TFT. Figure 3 (b) shows the hysteresis phenomenon of poly-Si TFT. When a desired gate-source voltage is applied from both high current and low current, the drain current can be varied with a gate voltage sweep direction, such as reverse or forward direction. The threshold voltage of poly-Si TFT with reverse sweep was -1.28 V where that of forward sweep was -1.49V. The threshold voltage was altered by 0.21V due to the hysteresis of poly-Si TFT. The difference of threshold voltage of poly-Si TFT is smaller than that of a-Si:H TFT due to the better quality of the gate insulator in the poly-Si TFT than that of a-Si:H TFT. Reverse gate voltage sweep is from V_{GS}=-20V to 15V, whereas forward is from V_{GS}=15V to -20V, respectively.[4]

The transfer characteristics of TFT were altered according to the direction of gate voltage sweep due to the difference of initial interface trapped charges with sweep direction. Figure 4 shows the difference of initial trapped charges according to gate sweep direction. In a-Si:H TFT the hole charges were trapped in the gate insulator initially with forward sweep direction due to the negative gate voltage, while the electron charges were trapped in the gate insulator with reverse sweep direction due to the positive gate voltage. Because the mobility of electrons is higher than that of holes, electron can escape from the gate insulator faster in reverse sweep direction than holes in forward one. It requires smaller gate voltage to make channel in reverse sweep direction than

gate voltage required in forward sweep direction due to the fast escaping of electron with reverse one. Therefore the threshold voltage with reverse sweep is smaller than that of the forward sweep direction.[4]

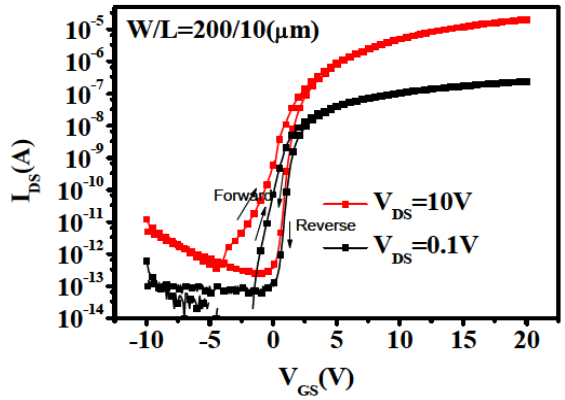


Fig -3a: Hystersis effect on the drain current of TFT. (a) a-Si:H TFT. W/L = 200/10

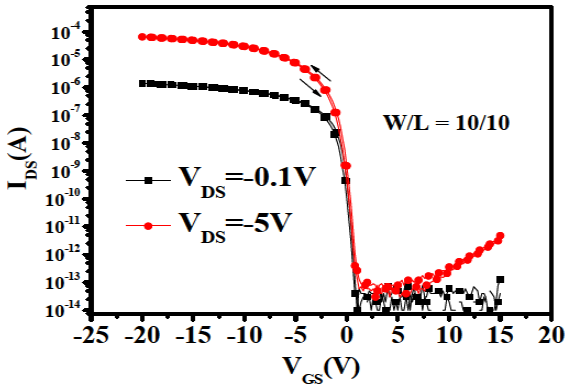
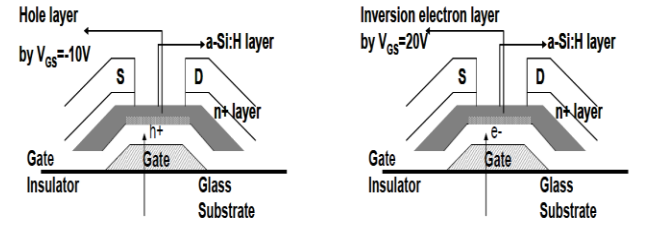


Fig -3b: Hystersis effect on the drain current of TFT. (b) poly-SI TFT. W/L = 10/10[4]



The initial trapped charge in a SiNx gate insulator at forward sweep direction

The initial trapped charge in a SiNx gate insulator at reverse sweep direction

(a) (b)

Fig -4: The interface trapped charge by starting gate voltage, resulting in the threshold voltage variation of TFT. (a) The hole charges are trapped initial with forward sweep direction. (b) The electron charges are trapped initial with reverse sweep direction.[4]

Hysteresis phenomenon can be also explained by the charge balance equation. The charge balance equation can be expressed as $(Q_G + Q_I + Q_S) = 0$, where Q_G is the gate charge, Q_I is an insulator charge, and Q_S is the silicon charge. Q_I includes the interface trap charges between silicon and insulator layer, so that $Q_I = Q_f + Q_{it}$, where Q_f represents fixed insulator charges and Q_{it} represents interface charges. Fixed oxide charges are located in the deep states of the insulator; thus, these do not relate with the hysteresis, which is a short-time effect. The Q_{it} contribution to Q_I is the cause of the hysteresis phenomenon. The mobile charge drift is influenced by temperature and bias duration. [4]

Temperatures up to 150 °C with long bias duration are high enough to ensure that the available sodium ions drift completely across the oxide. However, we made measurements at room temperature and for a short period (several sec), so that the mobile charge drift might not occur. Thus, we can conclude that the Q_{it} (interface trapped charges) contribution to Q_i is the cause of hysteresis phenomena. Hysteresis effects on current of poly-Si TFT was smaller than that of a-Si:H TFT due to the better quality of gate insulator in poly-Si TFT than that of a-Si:H TFT. In a-Si:H TFT, a SiNx gate insulator was used while the SiO_2 was applied in the poly-Si TFT. While the quality of SiNx was poorer than SiO_2, it was used in a-Si:H TFT because when the inverted staggered structure of a-Si:H TFT was fabricated, SiNx, a-Si:H and n+ a-Si:H could be deposited at once.[4]

$$Q=C_V,\Delta Q_{it}=C\Delta V_{TH} \qquad [1]$$

We evaluated the variation initial trapped charge density (ΔQ_{IT}) in the gate insulator according to gate voltage sweep direction from the delta threshold voltage (ΔV_{TH}) by applying equation [1]. It was found to be $3.31X10^{21}$ (C/cm^2) in poly-Si TFT while $1.10X10^{22}$ (C/cm^2) in a-Si:H TFT respectively. The ΔQ_{IT} in poly-Si TFT was less than in a-Si:H TFT because gate insulator of SiO_2 in the poly-Si TFT showed the better quality than that of SiNx in a-Si:H TFT.[4]

5. EFFECT OF HYSTERESIS ON P AND N CHANNEL TYPE POLY-Si TFTs

Figure 5. and Table I show the representative transfer curves of the accumulation mode p- and n-channel LTPS TFTs (W/L = 3.5/16.7 μm), of which the channel is intrinsic or B-doped with a dose of 2×10^{12} B/cm^2, respectively.[5]

Table -1: Extracted Electrical Parameters Of LTPS TFTs With Various Types Of Channels[5]

Channel Type	V_{th} (V)	SS (V/dec)	μ_{FE} (cm^2/Vs)	ΔV_{th} (V)
Intrinsic *p* -ch.	-3.5	0.46	92.7	0.38
B doped *p* -ch.	-2.2	0.51	90.0	0.24
Intrinsic *n* -ch.	1.2	0.58	162.1	0.04
B doped *n* -ch.	2.3	0.50	152.1	0.10

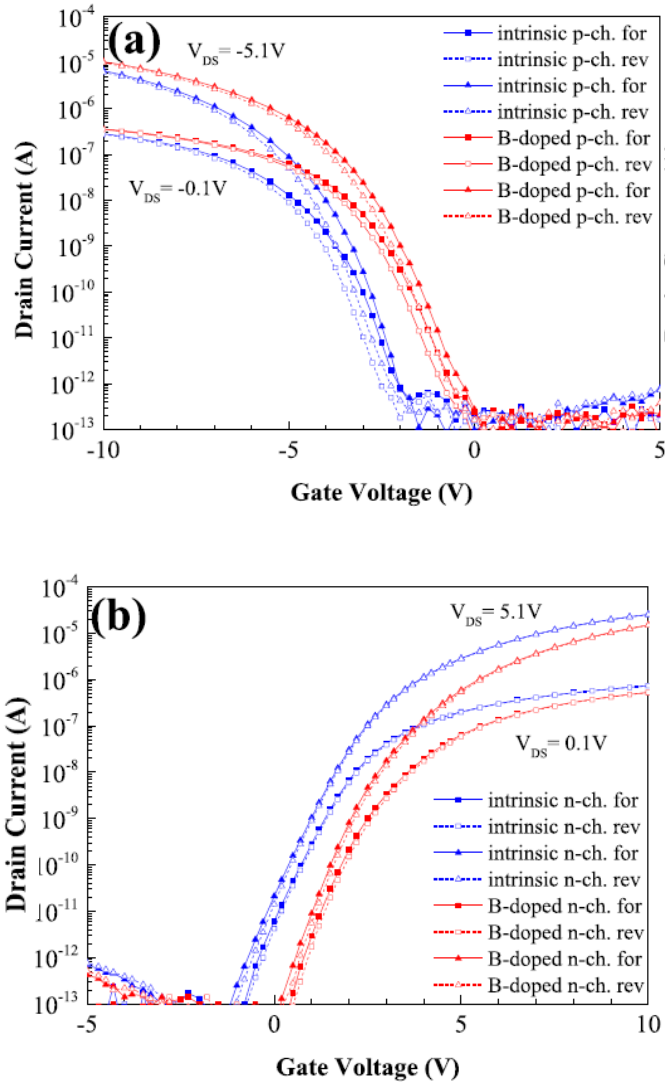


Fig -5: Hysteresis in the I_D–V_{GS} characteristics of LTPS TFTs with various types of channels. Intrinsic or B-doped (a) p-channel and (b) n-channel TFTs.[5]

The threshold voltage (V_{TH}), which induces a drain current (I_D) of 10 nA × W/L at drain voltage VD = −5.1 V, shifted positively from −3.5 V to −2.2 V for p-channel TFTs and from 1.2 to 2.3 V for n-channel TFTs when the channel was B-doped. The electrical performance deteriorated with the B-doped channel. The field-effect mobilities (μ_{FE}) were 92.7 and 90.0 cm2/V · s for intrinsic and B-doped p-channel TFTs, respectively, and 162.1 and 152.1 cm2/V · s for intrinsic and B-doped n-channel TFTs. As the channel was doped, the SS increased from 0.46 to 0.51 V/decade for p-channel TFTs, whereas the SS decreased from 0.58 to 0.50 V/decade for n-channel TFTs. This indicates that the number of defects at the channel and/or the interface between the channel and the gate dielectrics increases for p-channel TFTs but decreases for n-channel TFTs as the channel is doped. In addition, Figure 5 and Table I show the hysteresis behaviour with the forward and the subsequent reverse gate voltage sweeps performed from 15 to −15 V for p-channel TFTs and from −15 to 15 V for n-channel TFTs, respectively. For the p-channel, the hysteresis effect (V_{TH}) was greater than that of the n-channel and was suppressed as the channel was doped, resulting in a reduction from 0.38 to 0.24 V. In contrast, for the n-channel, the hysteresis effect was smaller than that of the p-channel and increased from 0.04 to 0.10 V as the channel was doped. The compiled quantity statistics shown in Figure 6 clearly illustrate that the hysteresis effect is greater in the p-channel TFTs than the n-channel TFTs and decreases in the p-channel TFTs but increases in the n-channel TFTs as the channel is doped with B.[5]

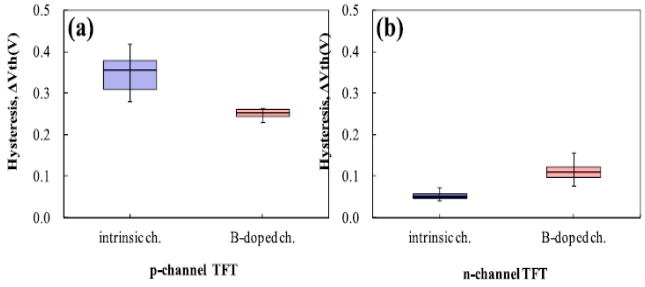


Fig -6: Compiled quantity statistics of the hysteresis in the I_D–V_G characteristics of LTPS TFTs with various types of channels. Intrinsic or B-doped (a) p-channel and (b) n-channel TFTs[5]

5. Variation of Trapped Charge (considering OTFTs)

Hysteresis in the output (I_D – V_D) and transfer (I_D – V_G) curves of OTFTs have been observed in Figure 8. In case no contact effects are present (V_C = 0, V_{GS} = V_G, V_{DS} = V_D, see Figure 7), the variation of trapped charge can be determined by measuring the difference in drain current between forward-sweep (FS) and backward-sweep (BS) curves, at certain values of the drain and gate voltages ΔI_D (V_{DS}, V_{GS}) = ΔI_D (V_D, V_G), where an injection of holes occurs in forward-sweep (FS) current and the extraction of holes occurs in the backward-sweep (BS) current. The relation between the variation of the trapped-charge surface-density $Q_{\Delta p}$ in the intrinsic channel of a transistor and the current displacement ΔI_D (V_{DS}, V_{GS}) is given by

$$q\Delta P = \frac{\Delta I_D(V_{DS}, V_{GS}) \times L}{w \times V_{DS} \times \mu},$$

where q is the elementary charge, μ is the charge carrier mobility, L and w are the channel length and width of the transistor's organic material, respectively.[6]

Figure 8 represents schematically the process of separation of experimental I_D - V_D curves with hysteresis at a constant V_G into I_D - V_S and I_D - V_{DS} curves. This process is repeated at different values of V_G, so that finally, ΔI_D (V_{DS}, V_{GS}) can be evaluated at different values of V_{GS} and V_{DS}.[6]

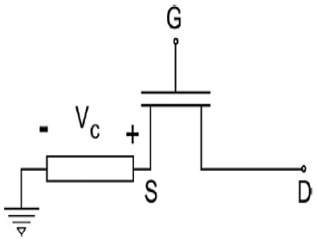


Fig -7: Proposed equivalent circuit of a TFT including a voltage drop at the source contact

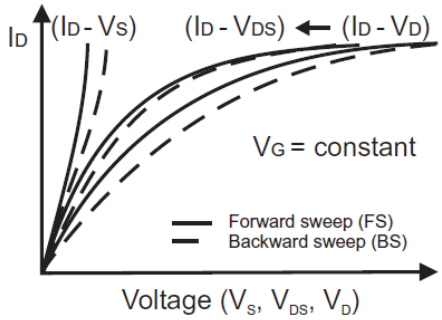


Fig -8: Scheme of current–voltage curves of the intrinsic channel of an OTFT (Id–Vds) and of the contact (Id - Vs) extracted from a Id - Vd curve measured at the device terminals at Vg

6. CONCLUSIONS

The dependence of hysteresis characteristics of driving TFTs on V_{GS} or V_{DS} was investigated.

Due to the changes in effective fixed oxide charge concentration induced by the trapping and detrapping of carrier charges the hysteresis for forward and reverse gate voltage sweep was caused. The hysteresis level was found to increase as the sweep range of V_{GS} increased. However, it was also found that the hysteresis level is independent of the applied V_{DS} values. This means that the recoverable residual image problem can be resolved by adopting the pixel structures that can compensate the dependence of threshold voltage on V_{GS} bias.[7]

REFERENCES

[1] Horng-Chih Lin, Cheng-Hsiung Hung, Wei-Chen Chen, Zer-Ming Lin, Hsing-Hui Hsu, and Tiao-Yuang Hunag; "Origin of hysteresis in current-voltage characteristics of polycrystalline silicon thin-film transistors"; AIP Journal of Applied Physics; DOI: 10.1063/1.3086271.

[2] Roman Gozdur, Piotr Gebara and Krzysztof Chwastek; "A Study of Temperature-Dependent Hysteresis"; Energies 2020,13, 1491,DOI: 10.3390/en13061491

[3] Hoon-Ju Chung, Dae-Hwan Kim & Byeong-Koo Kim (2005) "Hysteresis characteristics in low temperature poly-Si thin film transistors", Journal of Information Display, 6:4, 6-10, DOI: 10.1080/15980316.2005.9651984

[4] Sang-Geun Park, Jae-Hoon Lee, Hee-Sun Shin, Sung-Hwan Choi, and Min-Koo Han, "The hysteresis phenomenon in a-Si:H TFT and poly-Si TFT in AMOLED", ECS Transactions, 8 (1) 77-82 (2007) 10.1149/1.2767290 © The Electrochemical Society

[5] Jaeseob Lee and Byoungdeog Cho; "Effects of Channel Type and Doping on Hysteresis in Low-Temperature Poly-Si Thin-Film Transistors", IEEE Transactions On Electron Devices, Vol. 65, No. 3, March 2018.

[6] K.M.Awawdeh, J.A.Jiménez Tejada, P.López Varo, J.A.López, Villanueva, M.J.Deen, "Characterization of organic thin film transistors with hysteresis", Organic Electronics, ELSEVIER, Volume 14,Issue 12, December 2103

[7] Jae-Hoon Lee, Kwang-Sub Shin, Joong-Hyun Park and Min-Koo Han, "Experimental Study of the Hysteresis in Hydrogenated Amorphous Silicon Thin-Film Transistors for an Active Matrix Organic Light-Emitting Diode", Journal of the Korean Physical Society, Vol. 48, January 2006, pp. S76~S79