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Review on Fractional-N Frequency Synthesizers

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Abstract— Modern wireless transmission systems have increasing demands for frequency synthesizers. In this paper, a survey on designing an efficient Frequency synthesizer to suit a wide range of potential applications is researched. Various technologies existing currently and their parent technologies have been analyzed and the best results are extracted in the current research to suite a better design. In this review various parameters such as wide frequency coverage, fast switching speed, small step size and adequate spectral purity, low cost, compact size are analyzed. Even with the increasing demand for VLSI technology, a huge gap is identified in designing the synthesizers for PLL using VLSI technology.

Keywords: Frequency synthesizer, Phase locked loops, Voltage controlled Oscillators

I. INTRODUCTION

There is a constant pressure on the RF/microwave industry to deliver high functionality, small-size, high performance, low power consumption and low cost frequency synthesizers. Although all synthesizers differ in their applications, they share basic fundamental design objectives. The ideal synthesizer should be broadband with fine frequency resolution so that it supports a large number of potential applications. Aside from bandwidth and resolution, phase noise and spurs are the critical parameters that hinder the system's ability to resolve small amplitude signals. Another important parameter which impacts the overall system performance is frequency switching speed that in turn affect the time duration between switching which does not account for the data processing time [1,2] . Requirements such as wide frequency coverage, fast switching speed, small step size and adequate spectral purity, low cost, compact size—are the prime drivers in the development of modern frequency synthesizers. Various techniques used in designing and developing frequency synthesizers are reviewed in this paper, giving more importance to the fractional frequency synthesizers that has proven to be more efficient and durable when compared to the contemporary integer frequency synthesizers. The review constitutes various styles of VLSI techniques used to design the subject under consideration.

II. LITERATURE REVIEW

A. Programmable PLL

Kevin. W Glass came up with a programmable Fractional N Phase locked loop that uses a fractional divider when compared to the existing integer divider in the year 2006 [1]. This phase locked loop was made programmable using a Digital signal Processor (DSP) which allowed programs to be modified according to the needs, thereby supporting various applications. The output signal of the fractional N is phase locked to a reference signal and has a frequency 'f' which is a non-integral multiple of the reference signal fit. In a dual modulus implementation, the multi-modulus prescaler may switch between two different divisor values (e.g., N and N-1) during operation. When N is being used as the divisor by multi-modulus prescaler, the PLL's output frequency 'f' , will be equal to product of the reference frequency f and N. Likewise, when a divisor of N+1 is being used, the PLL's output frequency 'F' will be equal to the product of N+1 and the reference frequency f. By Switching between these two different divisors, a fractional divisor can be achieved, that is between N and N--1. Which means, an output frequency 'f' may be achieved which is a product of N+F and the reference frequency, where F is a fraction of value less than 1. The multi-modulus prescaler receives the output of the VCO [Voltage Controlled Oscillator] and frequency divides the signal to achieve a comparison signal having a frequency loop. The comparison signal is given as input to the phase comparator where phase of the signal is compared to that of the reference signal. The output signal of the phase comparator will be an indication of the phase difference. Thus programmable Fractional PLL could generate a wide range of reference frequencies. However this model does not provide for noise control or power consumption reduction. Also the area occupied is a huge drawback given the size of an average DSP. Therefore, the idea was developed subsequently making use of more software based approaches later on. Delta sigma modulator is a technique for encoding analog signals. Prescaler helps in switching fractional number between N and N+1.

Author [2] presents HK-MASHIII (Multi-Stage Noise Shaping Architecture) digital delta sigma modulator design and also a programmable prescaler divider circuit. The divider circuit operates with a maximum operating frequency of 10GHz and it may be utilized for noise cancellation. By these two circuits phase noise in decreased and power is optimized, simply by reducing bias current and the width of the transistor. A similar study has been done by, the authors [3] where they have discussed MASHIII delta signal modulator and here the author discusses a Delta sigma modulator. NTF zero-pole fist was compared with MASH III and proposed DSM (Delta Sigma Modulator) is depicted, in which both have 3 poles and 3 zeroes where all the poles are restricted to unit circuit. The system was found to be stable for MASH III DSM where all zeros are equal to 1 while for proposed DSM one zero is equal to 1 and for other complex conjugate pair with such distribution of zeros and poles, it filters M-band quantization noise characteristic below the loop bandwidth.

B. FPGA(Field Programmable Gate Array)

A paper proposed by the authors [9] about real-time FPGA implementation of I/Q modulation indicates that the basic synthesizer can be synthesized digitally with the very low frequency and the very approachable I/Q which is used for tuning radio frequencies. Few authors [10] presented a simplified QDDFS Architecture which provided optimization in terms of time, complexity and space. It had advantages of using very low amount of memory that is, only two 32 registers, fine frequency and phase resolution by reducing the use of device, as the architecture ultimately made use of only two registers, two multipliers, two multiplexers, and two adders. The authors also demonstrated that, using the Optimized QDDFS that could rapidly hop between the fractional frequencies, would lead to the design of an efficient SDR (Software Defined Radio). The authors had programmed using Verilog HDL codes and later implemented on Field Programmable Gate Array (FPGA) using Xilinx Tool. SDR is a Transceiver Architecture that comprised both transmitter and receiver. The Input to the transmitter part was a digital data and the data was retrieved back in digital form at the receiver. In transmitter, the text was encoded using the 16-QAM modulator which is followed by 8-point IFFT that converted the digital data into time domain. Same DDFS architecture was used at both the transmitter and receiver. The receiver basically performed the inverse of the transmitter. The FFT converted the digital data into data of frequency.

C. Injection-Locked Frequency Divider

Few authors [11] proposed a completely integrable phase locked loop which uses a frequency synthesizer that deals with 5 GHZ range and was developed using CMOS technology. This paper ages back to 2000 however, they have proposed a unique technique to reduce the power utilization. The synthesizer is usually a mixture of high frequency as well as low frequency blocks where the higher frequency blocks contains first stage frequency dividers along with voltage controlled oscillator. And such blocks are power consuming blocks. However, this problem could be solved according to the authors [12] by making the first frequency divider, an injection tracked frequency divider and reducing power consumption by means of on-chip spiral inductors. The PLL has bandwidth and phase noise of 280 KHz and the spurious side bands are less than 54 dBc. So SDR are designed which are multi-mode, multi-standard and multi-functional radio system.

D. High Frequemcy Cmos Fractional-N Frequency Divider

Author has designed a frequency divider using low power 0.5 micro CMOS technology called CMOSIS5, and it is designed for 900 MHz GSM standard mobile communication application [13]. Input signal is divided by N by this frequency divider. And output frequency must be 1/N times input frequency. Division ration can be N and N+1. So average result is a fractional number. Divider is fed with full adder whose carry output decides the value among N or N+1 as the ratio of division. And the divider consists of 2 counters (up counters) which generates press ctrl signal. If presc_ctrl is 'low' prescalar works as V and if presc_ctrl is 'high' prescalar works as V+1.

E. Flying Adder Based Digital Frequency Divider

Author [14] has designed flying adder based digital frequency synthesizer. The flying adder is used due to its simplicity and effectiveness. In order to produce a desired frequency it uses set of multiple phase reference signals. This implementation is done in standard 0.18um CMOS technology occupying 0.16 mm^2. The output frequency is between 39.38-226MHz and peak to peak jitter is made less than 130ps. The difference between conventional method and by using flying adder s that PLC should provide multi phased signal to the flying adder. The flying adder architecture is built on time-average frequency concept. The architecture used by the author [15] involves digital phase accumulators and phase-switching

prescalers. They also have incorporated multiphase generator that enables generation of multiple clock signals and also a sigma-delta modulator to enhance the signal purity.

F. Design Of High Accuracy Synthesizer

In this paper [16], the authors present an algorithm which can be used to divide a clock but cannot add to the accuracy of decimal frequency divider. Most of the time, frequency division ratio is not an integer number and will be a fraction. Hence we need fractional divider. Fractional divider uses high circuit resources, sometimes low power clock is required. In such cases, decimal frequency divider is used. We know that delta sigma modulator is the method for encoding analog signals into digital signals and use of fractional-N synthesizer allows high reference frequency, which allows fast dynamics. In PLL circuit, we have low pass filter which filters these high frequency contents thus reducing spurs and phase noise. Considering these aspects, the authors have come up with a Verilog design for the synthesizer [17].

G. Dual VCO[Voltage Controlled Oscillator]

In 2009, some authors [18] have written this paper on the basis of dual VCO PLL, an architecture composed of wide band frequency synthesizer for SDR is present with programmable divider. To achieve 4.3-10 GHz PLL tuning range 45nm technology is used. The below shown diagram is an LC-VCO. The phase locked loop exerts a phase and frequency detector with the help of a lever to avoid distortion. This produce largest oscillation amplitude for a given bias current and adopt power efficient class c NMOS. Synthesizer was fabricated with 45 nm CMOS in plain vanilla occupying 1.02*0.4 mm^2, in which 53% occupied by VCO and 30% by the filter.

H. 90nm CMOS

The frequency synthesizer (PLL based) is most important block of Radio Frequency transceiver. The aim of this method [20] is to ensure accurate output frequency. The phase locked loop have a lot other applications. The first one developed was using an analog component. A phase frequency detector is used here. They are implemented using XOR gate or D- flipflop. Voltage controlled oscillator plays a major role. It is also the heart of the whole design. A proper phase frequency detector architecture must be implemented. And the PFD must have a proper charge pump and loop filter. It is 800 MHz fractional-N PLL. This has centre frequency of VCO which depends upon sizing of transistors. To obtain radio frequencies, phase locked loops are used.

I. 180nm CMOS

In 2019, some authors had proposed a synthesizer [21] with output range of 2.1-2.5 Ghz and resolution of 1MHz and input reference of 50MHz. In this method, the integer-N synthesizer based on PLL and blocks of PFD, CP, VCO and frequency divider is increased in the order of 2.1 GHz, 2.15 GHz.....2.5 GHz very quickly. A second loop consisting the blocks of FVC, VCO and voltage divider is used to get 1 MHz steps in the output. The input frequency is high and is compared to the conventional method. The first loop will be locked very fast and the second loop will quickly move the output to 1MHz. Because of this, channels changing will be very quick. This structure is used because the structure is simple and has a low power consumption and a low output jitter. This is design ender 0.18 um CMOS process. The power consumption is about 36 mW. The channel can be changed by the synthesizer very quickly in less than 56ns. It has a very accurate and a smooth output and the jitter is small. The phase noise at the offset frequency in the carrier is -105 dBc/Hz and the noise performance is very good. This synthesizer is simulated in 0.18um CSMC CMOS process.

J. Power Efficient PLL Frequency Synthesizer

In this paper, the authors [22] discussed about the design of a power efficient PLL that operates on 30 GHz. The synthesizer uses high power amplifier, programmable divider and an LC tank voltage controlled oscillator. They have designed this model using SiGe BICMOS technology. The proposed architecture has an advantage of reduced phase noise with power efficiency. The VCO in the design is upgraded with the use of a single large varactor that can increase the frequency range. Also the quality factor of the overall output was increased by use of resonator and integrated charge pump. Colpitt oscillator was used to increase the varactor gain and coarse tuning the frequency of VCO.

K. 45nm PLL

In 2013, in a paper [19], the authors had written about the application of Bluetooth based on fractional- N Phase locked loop frequency synthesizer that is designed using VLSI technology to be low power consuming. In wireless communication industry, phase locked loop is represented as the dominant method. Loop filters and sigma-delta modulators are prime factors for improving the performance of fractional-N PLL. Operation of dual modulus divider is introduced. Because of this operation, noise is introduced in the phase locked loop. A digital sigma-delta modulator is introduced in the PLL to eliminate this noise. And desired fractional ratio is generated by random integer number. The noise produced at the PFD output side is converted to higher frequency and is removed by the LPF. The main usage of PLL is to reduce power consumption and high stability. The main advantage of this paper is that up to 2009 only 90 nm technology was used. The authors, have proposed a project with 45nm technology instead of 60 nm and 90 nm technology. 45 nm CMOS technology has been implemented for phase detector, loop filter and VCO using microwind 3.1 backbend software of VLSI. Analog circuits were designed using CMOS transistor for individual blocks of PLL and found that power consumption was less. PLL, phase detector and VCO were efficiently designed. Blocks will be cascaded in other parts which will be used for fractional-N-PLL.

L. Various Methods To Reduce Spurs

In a paper about reducing spurious tones in the output signal, the authors [6] discuss about a fully synthesizer that is capable of producing both in-phase and quadrature phase signals. Their VCO is tuned using not one but two parallel charge pumps that is more capable of maintaining constant in-phase noise. By means of shielding the input buffer that acted as a reference buffer, the spurs that were closer to integers could be reduced. Also it was observed that the spurs mainly arose due to two reasons; one being the result of non-linear phase detector and the other being the high gain of VCO. The authors presented their model using the BiCMOS technology in 0.25 micro meter. The two charge pumps shared the same phase detector thereby reducing the non- linearity and the dual loop architecture ensured reduction of the device noise associated with the charge pump. The noises were further reduced by optimization of the currents associated. Adding to this, a unique layout technique which could specifically reduce the VCO induced spurs in fractional-N synthesizers was demonstrated.

Further, the same authors [7] came up with a solution to reduce the spurs even more and analysed the fractional-N phase-locked loops with substrate-related spurious tones which made use of integrated VCOs. The positions of spurs were deduced through calculations and verified through experiments as a function of the division ratios of programmable divider and the prescaler. The spur power levels were measured and compared with mathematically deduced theoretical expectations considering an integrable wideband PLL designed using SiGe BiCMOS technology. Minimization of spurs using a variable reference frequency was demonstrated experimentally and based on the observation, they suggested a programmable integer-N PLL for driving the fractional-N synthesizer which could reduce the worst-case spur level. In this paper, the authors [8] deal with spurs reduction in the fractional division part of a frequency synthesizer. They have reduced the spurs in their model by substituting the fractional divider with a digital phase accumulator and a DAC. This model was proven to be more effective than the sigma delta modulator. It is to be noted that the noise has to be properly quantized. Un-quantized noise can be reduced only by means of passive filtering which in turn increases the power and area consumption. Moreover they have used phase interpolation technique instead of compensating quantisation noise in digital domain by intending the loop bandwidth.

III. CONCLUSION

Modern wireless transmission systems have increasing demands for frequency synthesizers. These requirements sprout from various radio standards that prevailing mobile devices have to support. This multi-standard support results in increased complexity for designing frequency synthesizers that can be used for multi-band operation. This issue can be solved by improvising frequency synthesizer with fractional frequency dividers. With the assistance of these type of dividers, wider frequency range can be used for better frequency resolution that uses high frequency fractional-N divider. Moreover not many synthesizers were made application specific. Designing the synthesizers for a particular application has an advantage of greater efficiency in terms of time, power and area. Though there are a few works under this light, very few synthesizers are able to work in high frequency bands. Hence, the authors have come to a conclusion that designing a frequency synthesizer for the application under consideration, i.e. Software defined radio and making it

operable in high frequency bands with spurs reduction techniques can provide better results. According to our design, we have followed prescaler design algorithm when compared to all other reviews, ours is the simplified and logically mathematic for frequency divider. The exact ratio can be achieved by using prescaler design.

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