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Survey on Post Silicon Validation and Contribution of Scan Chain Technology

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Abstract - *Post Silicon Validation basically refers validating silicon developed for different client segments after the first few chips are available and just before releasing the chip for customer use. It helps in finding out and correcting the bugs in integrated circuit (IC) along with system after producing few chips before the actual mass production. In pre silicon validation it's not the actual chip which will be tested but is just the simulation of the system working which will be tested. Here it is nearly impossible to find out all the defects and bugs due to the complexity of design. This makes it possibility that many of the bugs might escape this stage, these bugs or defects will be caught in the Post Silicon Validation stage. These will be captured during Post Silicon Validation by using very real-life environment debugging tools. Post Silicon is a stage where chip is in its physical format. So, it's almost the user model which will be tested here. Post Silicon Validation is considered as an emerging research field in automation of electronic design. Scan chain technology is also one of the vital debug tools in the Post Silicon Validation environment. This tool makes use of Design for Testability and Design for Debug concept in which, design of the circuitry is made such that it has a separate component to take the dump or say scan the latest reading of the flipflops. This is a very critical debug tool as it deals with the nightmare situations for any processor engineer such as a crash or hang or a catastrophic error. Here we will be providing a view of the Post Silicon Validation and scan chain technology. We will be seeing through the different scholarly works related to these technologies. We will be analyzing the working, going through the challenges and recent studied related to these technologies.*

***Key Words*:** Post-Silicon, Pre-Silicon, Scan, DFT, Flipflop, Processor, DFD

1. INTRODUCTION

While corporates spend millions creating new processors, it is extremely necessary that the new chip functions are meeting its requirement and are deliverable to the customers within the time frame promised. Even a delay of a few weeks can incur significant loss. Post Silicon Validation is hence one of the most vital stage in product manufacturing to achieve the desired success. The motto of Post Silicon Validation is to guarantee that the silicon design works appropriately under real operating conditions while executing real software, identify and correct the faults and errors that may have bypassed by mistake during Pre silicon Validation.

Validation (Post Silicon) is a method in which the chip which is manufactured is made to undergo tests for all accuracy and correctness with respect to its function in an experimental lab environment. This is done through using the actual silicon chip which is brought together on a test board or a reference board along with all other apparatuses which are part of the system for which, the chip was designed for.

The Need: Post Silicon validation comprises of all that validation effort that is bestowed onto a system after the first few silicon samples are manufactured for the same purpose, but ahead of the actual product release. As Pre-silicon involves only simulation, there is tremendous chances that quite a lot of functional errors/bugs leak into the manufactured silicon, and it is the work of Post Silicon validation to sense, correct them as well so that they do not leak into the final customer system. The bugs in this stage are often system level bugs and erratic corner case conditions concealed profoundly in the design state area, as these snags incorporate many design parts, they are very hard to identify with Pre silicon tools. As these tools have very less scaling capacity and performance metrics. Post Silicon Validation differs from this as it profits from very high raw action, since tests are performed directly on silicon chip which is nothing but what the end user will use.

The main aim of our actions here is to check/validate most of the use cases that a buyer might eventually have in real applications and to meet the expectations of all the use models on a chip. This validation occurs firstly for distinct features and interfaces of the silicon chip and then may/may not include running actual software and applications, that stress tests all the featural specifications of the chip design. This validation habitually consists of both software and hardware efforts. This is because the entire procedure includes validating the silicon chip in a system level setting with actual software running on the hardware.

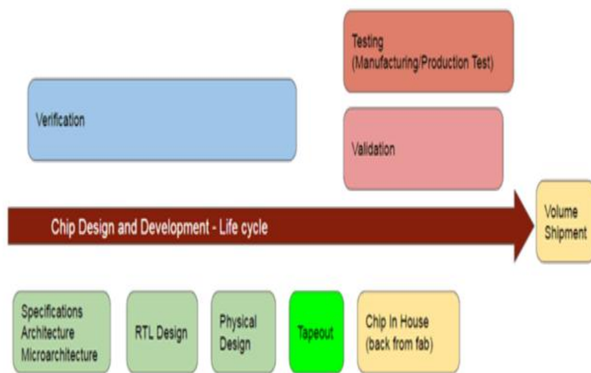

Fig -1: Life Cycle Pre Silicon and Post Silicon Validation

Fig -1 depicts the life cycle of the chip from Pre Silicon to Post Silicon Validation to final product. The main aim of Post Silicon Validation is to make sure that the silicon chip design works efficiently under real operating conditions while executing actual software, identify and correct the errors that may have been bypassed while performing Pre Silicon Validation. The complications in today's SoC design has made design engineers to develop new IP integration methodologies to handle the growing complexity that lies in these embedded systems. In Post Silicon validation usually the test programs are created along with test software to enable functional and stress testing of features, validation with real use case applications also carry out performance validation with industry standard benchmarks.

1.1 Scan Concepts

Scan is one the most important DFT technique. There are different scan techniques. In flipflop based scan we have:

1. Mux based (1973, Stanford)
2. Clock based (1968, NEC)

In Latch based we have LSSD (1977, IBM). The idea of scan is to connect internal flipflops or latches as shift registers, this will help us to control or regulate the internal flipflops or latches in test mode. This feature is life saving for the chip manufacturing industry as this is used to debug when there is catastrophic error or hang or crash. We should know that the circuit will function normally when in normal mode.

The idea was proposed by Stanford University in the year 1970's. Scan remains one of the most important techniques for synchronous digital circuits. The Fig-2 shows the flipflops before and after the scan insertion. On left hand side is the original flipflop before the insertion of scan. The right-hand side shows the flipflop after the insertion of flipflops. After the scan insertion we replace the non-scan flipflops into scan flipflops. We can observe that the yellow flipflops or smaller than the orange flipflops here. The next important step is we stitch the scan flipflops into a chain so that we can scan the whole chain together. This process is known a DFT insertion or DFT synthesis in the design flow.

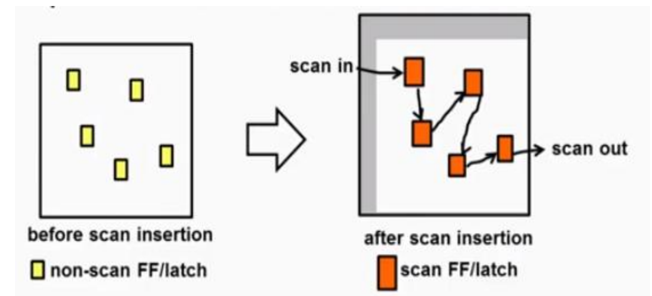

Fig-2: Flipflops before and after the scan insertion

1.2 Scan Flip Flop

The scan flipflop is substitute for normal flipflop when one wants to have a design for testing in the circuit. For scan flipflop we will be having four important pins. They are:

1. Scan chain: Scan input (SI), Scan output (SO):
These two pins are used to connect scan chain as a shift register
2. Logic: Data Input (DI), Data Output (DO)
These two pins are used to connect scan flipflop from and to the logic. Fig-3 depicts a simple scan flipflop. Scan flipflop has two functions to be performed Shift and Capture. The different pins present are Data(D), Scan Input (SI), Scan Enable (SE) and Clock (CLK) pin as depicted in the schematic.

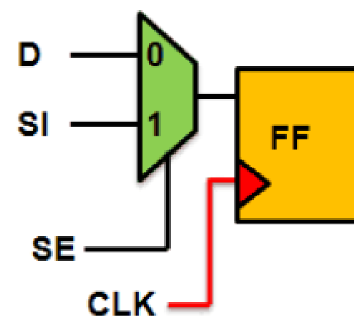

Fig-3: Scan flip flop block

The circuit of the scan flipflops has two operation modes. In the normal mode it performs the capture function. They capture the response from the logic, and they apply the response to the logic, which is exactly same as the original circuit. In Test Mode the scan flipflops are first configured to perform shift operation. So that we can shift in our test pattern and then the scan flipflops are configured to capture the response from the logic for one or few cycles and then the flipflops are configured to do shift out operation so that we can observe the vales of the flipflops for further debug. This is depicted in the Fig-4 and 5 below.

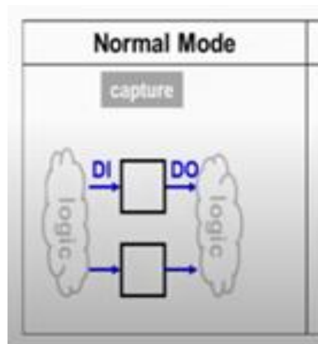

Fig-4: Normal mode of Scan flipflop

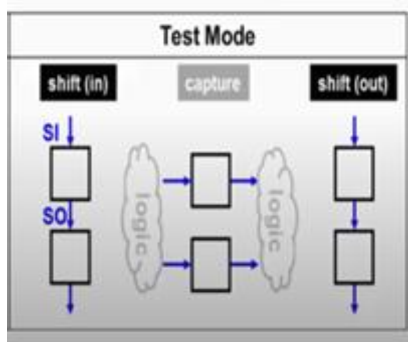

Fig-5: Test Mode of Scan Flipflop

The remaining part of this paper is structured in the following way: Section-2 provides the literature review where we go through the works and proposals of different scholars regarding the post silicon validation and scan chain technology. Section 3 provides us the basic working principle and steps in the scan design flow by explaining the various stages in the same. Section 4 concludes the paper and provides an insight on what can be the future works related to this technology.

2. REVIEW OF LITERATURE

According to S. Mitra et al. [1] Post-silicon validation is used to find and correct errors in integrated circuits (IC) and chip level systems post the manufacturing. As a result of complex designing it is very difficult to find and correct all the defects or bugs before the manufacturing is done. It's nearly impossible to have 100% accuracy here. Post Silicon Validation is most challenging for upcoming processor systems. In present day it is principally understood as an action with a very less methodical solutions or processes. This is the reason why the Post Silicon Validation is an emerging futuristic study topic. It provides various chances for futuristic big inventions in electronic or automation of silicon design fields. They identify four important steps in Post Silicon Validation: Problem detection, confining the problem to specific area, identification of the reason of the failure, and debug the problem if it's in reach or bypass the problem depending on situation. They quote several reasons as to why the validation plays and important role in product delivery. Pre silicon validation is in no place to detect all the bugs, so the Post Silicon Validation becomes essential. Modelling of electrical bugs is a very difficult task in the pre silicon validation stage. Even for the design errors it's the same story. Metrics or techniques of testing are less standard to that of the Post Silicon Validation. That sums up that post silicon is very crucial stage.

According to A. Nahir et al. [2] They observed that Post Silicon Validation is more effort consuming, say approximately 50 percent of design efforts of SoC's overall design efforts put in. Also, as measured cost wise the complexity is going to increase steadily as and when the design becomes smaller and smaller. In Pre-Silicon verification, the process is carried away involving separate zones like functional, electrical, performance and software. This is unlike in Post Silicon Validation. Here they speak about covering the gap in between the Pre Silicon Validation and Post Silicon Validation. One of the suggestions given is a different method to linking the technical space/gap is to be trying and giving silicon chip some of the features of the simulation atmosphere. Requirement of the day is a way to capture post silicon test related with an error/failure in a nonconcrete way that can be verified on a pre-silicon model. They identify two problem here. One is pre silicon environment is very slow compared to Post Silicon Validation environment. Second, wrong assumption in pre silicon that the hardware underlying is covered completely, to mitigate this they suggest a hybrid method between the pre silicon validation and Post Silicon Validation methods.

According to S. Ray et al. [3] Post-silicon validation is important activity as in it plays a goalkeeper role in a SoC designs. One of the vital actions in SoC designs is Post Silicon Validation. It covers the pre-production fabricated chip, on which we run tests and multiple software. The aim here is to check that the chip works fine in actual user conditions. In Post Silicon Validation the test runs at billions of times clocks speed than that of RTL simulation, and at a higher magnitude than that of hardware accelerators, emulators and so on. This provides an opportunity to the validation engineer to explore the design states at a deeper level and run in real environments like different OS and booting environments and so on. This is not possible in pre silicon validation. They say that Post Silicon Validation involves a lot of complexity and thus requires presence of many stake holders. They also elaborate some of the security challenges involved in this process. DFD is the one area which they have concentrated here, which is basically one which provides observable capacity and control over the states which are during functional operation of silicon.

According to K. Balston et al. [4] Pre-silicon validation and Post-silicon validation varies in two fundamental ways: The SoC(System on Chip) runs roughly a billion times faster in Post Silicon Validation environment than full SoC simulation

and can be integrated to the real systems; Second in simulation there will be possibility of internal operations visibility and also there will be controlling mechanisms, this is not possible in Post Silicon Validation environment. This paper addresses the issue and mis interpretations of area coverage. It tries to bridge the gap between what is assumed with respect to the area coverage in conventional mechanisms and actually what is achieved. The paper proposes the following results: The boot Operating system test frequently attains high coverage, analogous to pre-silicon directed tests, but in some blocks the coverage can be low or markedly dissimilar between pre and post-silicon. The area overhead of the coverage monitoring instrumentation more. State-of-the-art software analysis techniques decrease the overhead considerably, but the residual overhead is still inadmissibly high for practical deployment.

According to K. Basu et al. [5]. Distinguishes between the testing after manufacturing and Post Silicon Validation as to say that they have entirely varying objectives. Physical bugs or defects are caught in the manufacturing testing process. Whereas the Post Silicon Validation is designed to catch the functional bugs and bugs due to electrical mismatches or faults.

According to C. Gu et al. [6] Post Silicon validations goal is to make sure that a product meets all the best process steps accurately also ensure that all operating environment requirements are met. At last, Post Silicon Validation, a Product Release Qualification (PRQ) verdict is made rendering to the risk valuation as to how many chip systems may not meet the specified conditions. In a life cycle of a product, the PRQ pronouncement is a key breakthrough, only after which high volume manufacturing is launched.

According to S. Yerramili et al. [7]. Depicts post silicon in what way it can affect the release dates and company's commitment to the delivery of customers expectation. The Post Silicon Validation is one which had to give a pass to the product to be produced in mass scale. Otherwise there would be a lot of delay in mass production of the product. So, the watch keeper to the gate of manufacturing few chips for validation to manufacturing in large scale product for customer consumption is the Post Silicon Validation phase. Thus, if delayed can result in losing the market and reputation. Hence, it is very important to have fast, systematic flow of work in Post Silicon Validation.

According to N. Nicolici et al. [8]. Post Silicon Validation adopts design for debug, as observability and lack of in system control will be present in design of chips. Anticipates that, as the design complication grows, taking and handing out circuit information at gate level will turn out to be more and more difficult. In this work, they recapitulate the known techniques and debate some likely guidelines of study that can use high level circuit descriptions to enlarge the prevailing resolutions. For a person to get as much as possible information from the SoC, to get to know the nature of the errors and faults, DFD is inserted in the design.

According to Y. Huang et al. [9]. Speaks mainly about what are resorts or techniques to follow when the scan chain itself fails. Provides a fair idea of what are the different scan chain failure diagnosis techniques to follow. New directions for the present diagnosis is recommended in this paper like multiple chain failure diagnosis per chain, enhancement of resolution for diagnosis of intermittent failures or faults, need of improving speed on runtime diagnosis for mass quantities of chips, cell based chain fault methods are currently used so diagnosis will be spread in one cell but generally the cell and its connections are spread widely in the silicon chip. Hence improvement of resolution to a specific signal would be more accommodating for physical failure scrutiny.

3. WORKING PRINCIPLE

As shown in Fig-6 the basic working principle in Post Silicon Validation is loading a test which passed in pre silicon validation simulation test on to the actual board and testing if same result as we got in pre silicon validation shows up. If yes, the board is passed for mass production, if not then is the process of debugging a Post Silicon Validation starts. In debug tools we have wide variety of tools for each IP unit on the processor board. One such test we do is the scan chain test which uses the Design for Testing or more specifically Design for Debug principle.

Design for test (DFT) scan concept was developed in 1960s as IC complexity grew. The vision originally was to test the integrated circuits whose complexity was growing gradually in an efficient way, as the old methods mostly were carried out manually by inserting special logic to test the integrated circuits. This was originally owned to test in high volume manufacturing environment in factory where the chips where just checked on the go rather than test a bunch of chips rather quickly and kind of identify the defects, measure the health of silicon not necessarily using it in a functional mode as an end user would or a customer would use. Basically, the aim was to check if silicon is working or what part of silicon is failing in a manufacturer perspective.

The three basic advantages of the use DFT method for debugging of the SoC are: First, the easy adaptation behavior of the DFT architecture to several systems architecture, Second, DFT methods and techniques have been developed well and used over the past few decades, there is partial impact on a design in relation to that of area overhead, testability, and power consumed, therefore the debug and manufacturing cost is less. Lastly, reusability of the design is vital and critical for modern SoC designs to preserve low cost and decrease time-to-market.

Scan design flow explain how the original design will be transformed into Scan design and goes on till extraction of scan chain dump.

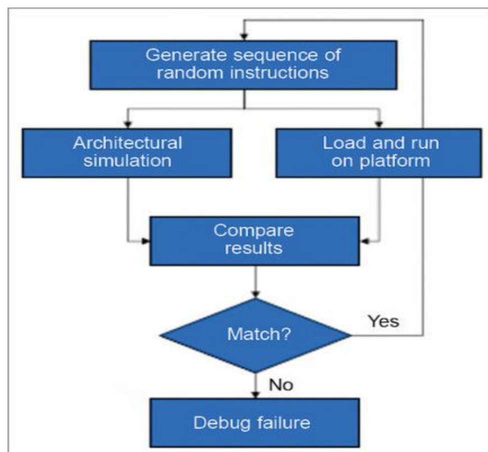

Fig-6: Flow chart for initiation of Post Silicon Validation

As we can see in the design flow there are two phases present in scan chain design flow.

Design phase:

As an initial step we need to check up whether our original design obeys the scan design rule. If not, we need to adjust and repair the design to obey the same. There are many scan designs rules. These scan design rules need to be set to correct states or values before the start of operations. Few examples of these are handling of gated clock, setting of tri state bus and so on. After this step we will have Testable design with us. Then we need to enter the phase of Scan Synthesis. In Scan synthesis there will be four stages where we modify the design so that we can appropriately extract the scan information from the same. During the scan synthesis phase, we also require Layout information and constraint and control information from the designer of the chip. Fig-7 shows the flow of scan design on basic level, steps which depict the scan synthesis are also included in Fig-8.

The four steps of scan synthesis here are:

1. Configuring the scan: The designer can decide the number of scan chains to stay and which not to include. Here the designer decides which Flipflops to include which to exclude.

2. Replacing the scan: This step includes replacing the original normal flipflop with scan enabled equivalent flipflop. Here by the obvious reasons the area required will be more as the flipflops grow in area due to extra scan circuitry.

3. Reordering the scan: Here it involves rearranging or reordering the scan cells to reduce the routing wire required. Here we take the help of layout information given by the design team.

4.Stitching the scan cells: We will connect all the scan cells together to form scan chains.

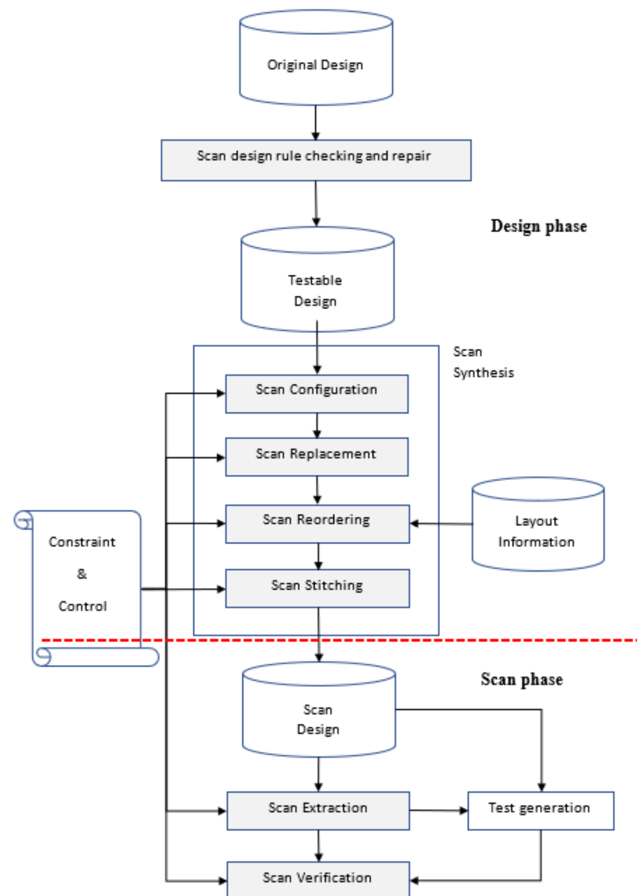

Fig-7: Flow of scan design [20]

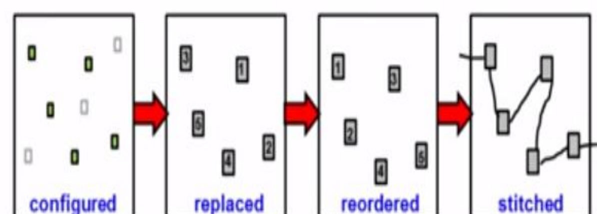

Fig-8: Steps depicting the Scan Synthesis phase

Scan phase:

After all these steps we have scan design which has scan chain inserted into our original design. We can start test generation at this phase. After test generation we can do scan verification to make sure that the test pattern can be correctly applied to our design.

After the scan synthesis we have a scan design which will be ready for scan test pattern generation. But as ATPG is separate from the scan synthesis elements we need to first have extraction of scan information from the scan design for

test generation. After that we need to verify our scan test pattern.

Hence, scan extraction is required to get the correct order of scan cells for ATPG. To also be sure that all chains are correctly connected. Scan verification has two functionalities. One, to have surety that ATPG test patterns correctly applied and both shift and capture functions are correctly done.

Fig-9 shows a structure and components of typical scan chain. We can see that there is a common clock between the scan flipflop which assists in taking the scan of the flipflops by bypassing the combinational logic between the flops.

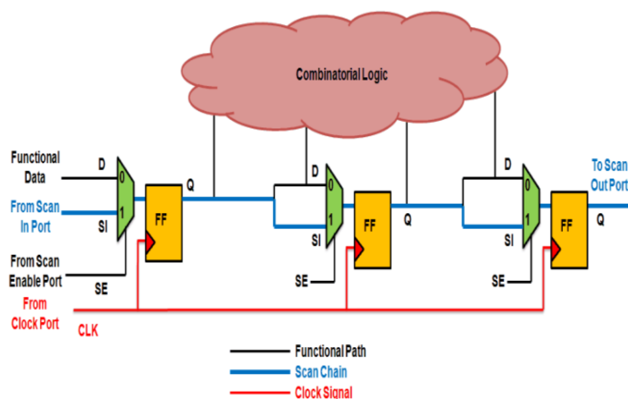

Fig-9: A typical scan-chain

Advantages and disadvantages of scan chain technology:

Advantages of scan:

- It will give us a way to carry out systematic DFT, not an ad hoc way of doing it.
- Easy ATPG is provided which gives faster run time and higher fault coverage is provided.
- Easy way of silicon debugging, or diagnosis is provided by this. After manufacturing if there are any discrepancies, we can shift out the data and observe the values of flipflop which is very useful for diagnosis.
- Unlike earlier ways where it would require extra setup for debugging this provides an inbuilt compact way of debugging.

Disadvantages of scan:

- We need more area i.e., area overhead is present, typically five to ten percent of area overhead is acceptable.
- Routing of scan chains also requires more area than usual area requirements.
- Performance overhead is present as scan flipflop has longer setup time, hold time.
- Pin overhead is present as many extra pins like scan in, scan out, scan enable, scan clocks etc. are inserted here.
- As the area increases even the power overhead is increased.
- Design efforts requirements will increase as we need to have scan insertions, and for scan verification.

4. CONCLUSION AND FUTURE SCOPE

In the paper we have tried to explain what exactly Post Silicon Validation is, how is it different from Pre-Silicon Validation. Debug tools form an integral and important part in Post Silicon Validation. Scan chain technology is one such important tool. This tool helps in know the value of the flipflops or registers which is of great help while debugging failure or defects on system on chip. This paper tries to give the brief explanation of the basic technology behind the scan chain technology, what are the different phases or stages in the scan technology especially what measures are taken in design phase and scan phase is explained briefly.

We have briefly explained the literature of several scholars in the area of Post Silicon Validation and scan chain technology. There is lot of scope for improvement in the Post Silicon Validation as suggested by various scholars and researchers. Especially with respect to decreasing the overhead of area, Pin overhead, performance overhead there is tremendous scope for future researches. Power overhead increases as the area overhead increases which needs further research and development. As the scan flipflop is addition to the normal flipflop design optimization is also an area of concern.

Here we have tried to explain the Post Silicon Validation and scan chain technologies in a bird's eye view. This paper emphasizes on giving the baseline knowledge or introducing of these most important technologies in post validation environment.

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