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Investigation of the Simulation Study of Single Gate Extended Source SOI-Tunnel Field Effect Transistors

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Abstract - *The proposed work presents an extensive simulation study of the various parameters of SOI Single Gate Tunnel field effect transistors with extended source and compare it with standard TFET structure using Sentaurus TCAD. The parameters such as Ion, Ioff, Subthreshold wing and Threshold Voltage are studied for different Source doping, extension width and length variation and for variation width of the body oxide. Finally, an encouraging model with all the optimum parameters is derived for the parameters of interest.*

Key Words*: *TFET ; extended source; BTBT; Sub- threshold Swing; Threshold voltage;Ion; Ioff; TCAD

1. INTRODUCTION

As the scaling down of the transistor is marked as an important event owing to the Moore's law, The Tunnelling Field Effect Transistors comes as a major contender to the MOSFETs as they outperform them in low power usage and with a good subthreshold swing at room temperature [1]. Such sub-threshold swing provides us with very low off-state leakage current and thus can be operated at much lower supply voltage [1][2]. Reduction of energy consumption is the major challenge that the designers face nowadays, and beyond CMOS technology comes as a rescue for the same as the bias supply VDD is reduced. Low subthreshold swing, low Ioff, high Ion and low threshold voltage are considered optimum for low power applications. [3]

Unlike MOSFETs where the carrier transport mechanism of Tunnel FET uses Band to Band Tunneling which would be almost not dependent on temperature. This tunneling may be horizontal tunneling or vertical tunnelling.

This work proposes an extended source structure. The Extended Source tunneling Field Effect Transistor has been reported to give better performance in terms of sub-threshold swing and drive current of the device due to its enhanced tunneling junction area [5]. We use a rectangular extension over the channel region from the source with similar doping configuration. The extended source majorly increases the count of tunneling path from source to drainat the same time enhances the tunneling probability and thus the tunneling current giving a high Ion. [2], [4], [6]. We optimize the structure with variation of length and width of the extension.

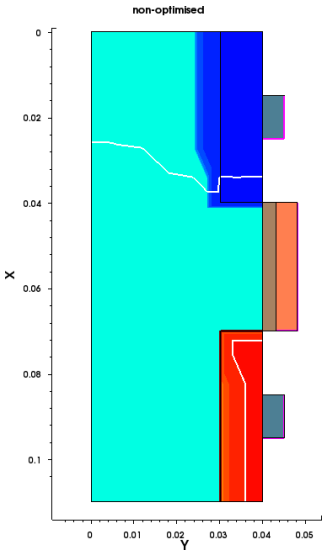


Fig -1: The Non-Optimized TFET

We also vary the doping concentration of source, and the body width with and without the body oxide layer. As a combined effect of these schemes the structure is expected to demonstrate a better performance over the conventional structure. The results of the device parameter studies are used to obtain an optimal structure with consideration of trade-offs among the electrical parameters of interest for this device. The Optimal structure has a sub-threshold swing 37.77 mV/ decade, threshold voltage of 0.8842V and an on-state current of 2.9814nA/ µm with off-state current of nearly 1.473pA /µm at a reduced supply voltage of 0.1 Volt in 30nm channel length.

2. DEVICE STRUCTURE

The structure of TFET is P-I-N structure; source and the drain are very heavily doped while the semiconductor layer is slightly doped. The gate terminal controls the electrostatic potential and the concentration of charge thus increases in the junction between the semiconductor and extrinsic region. TFET also ensures a much lower OFF current due to the reverse biased P-I-N structure.

The device dimensions are having a fixed value of drain doping of 1xe^(19), the oxide thickness being 3nm. And the channel width is fixed to 10nm and the intrinsic channel length of 30nm.

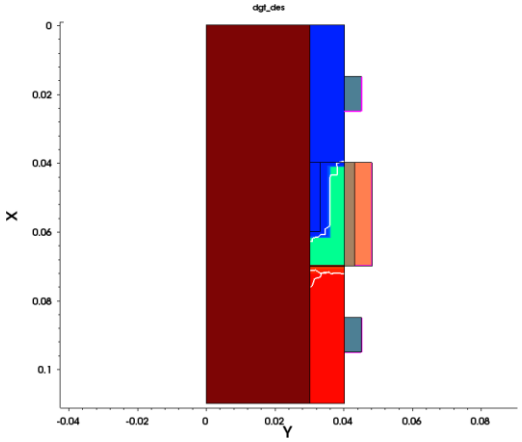


Fig -2:The Device structure

We use HfO_2 a High-K dielectric in the gate oxide and SiO_2, a Low-K dielectric in the body oxide. We use the gate contact of aluminium with an optimum work function.

3. DEVICE PARAMETER STUDY

With the large density of transistors on a chip and faster clock speeds the issue of dynamic and static power is to be addressed. Dynamic power is relation to $CfVDD^2$, where C being the load capacitance and f is the frequency, VDD is the supply voltage. Reducing the supply voltage is the best way to reducing the dynamic power consumption due to its squared dependence. Similarly, the static power consumption, requires optimization in terms of gate leakage currents and the switching characteristics. The Gate leakage is minimized using high-k gate dielectrics which allows for thick films, reducing the tunneling probability via the gate oxide along with the same electrostatic control. To minimize the losses that occur during switching - a low subthreshold swing, S, and a smaller voltage is preferable [4]. The reduction of S and VDD are altogether addressed by using Tunnel field-effect transistor (TFET).

3.1 VARIATION OF SOURCE DOPING

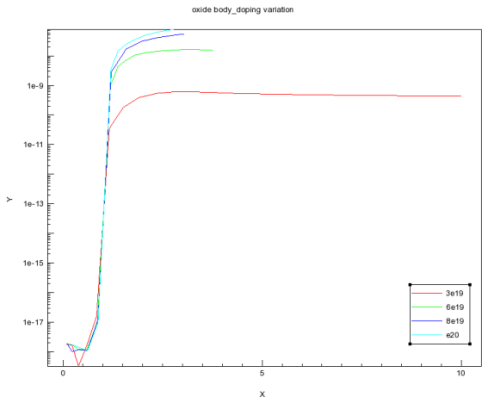
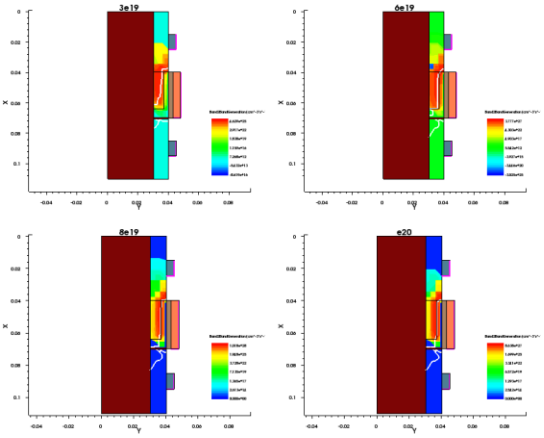
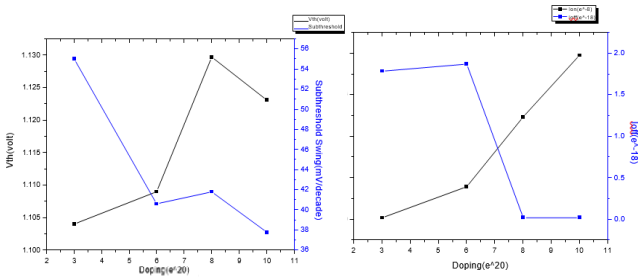


Fig -3: Output characteristics –doping variation

In order to avoid the ambipolarity, we go for asymmetrical doping of the source and the drain and thus make the transportation unipolar. Since the Fermi levels potential, an increase of doping concentration in the drain up-shifts the energy bands leading to a larger overlap and an increased tunnel current. On the drain side, where the NA is kept constant, the tunneling probability at the drain side is unaffected.



(a)



(b) **(c)**

Fig -4: (a)Variation in source doping –tunneling (b)Vth and Subthreshold swing variation(c)Ion and Ioff variation

It is thus demonstrated that employing an asymmetrical doping profile between the source and the drain regions is a simple and efficient way to reduce the ambipolarity.

3.2 VARIATION OF LENGTH AND WIDTH OF SOURCE EXTENTION

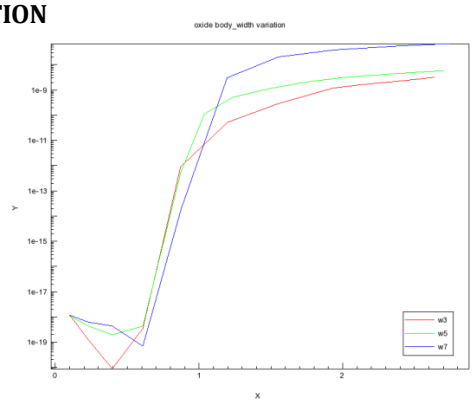
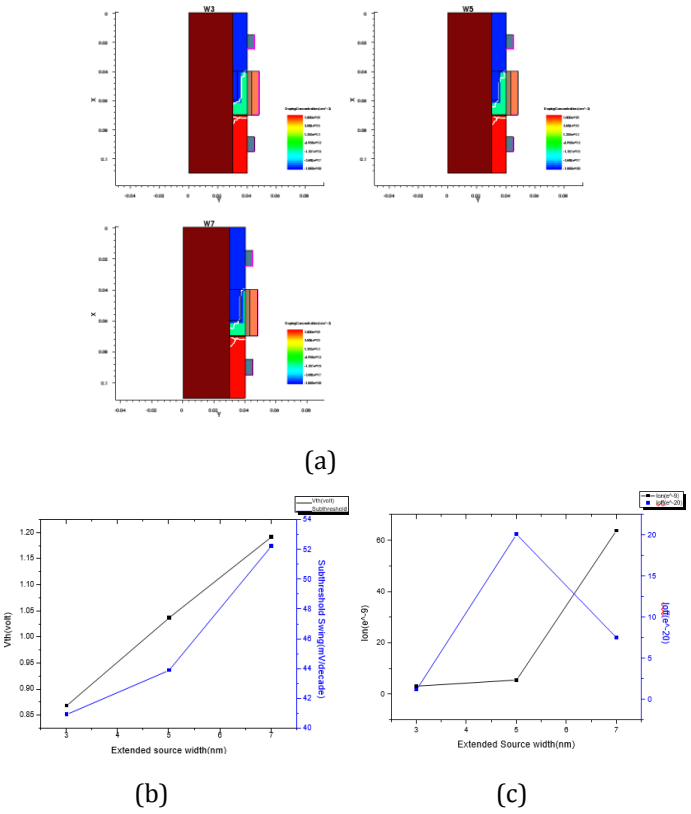


Fig -5: Output characteristics –source ext.width variation

Now optimizing the length and width of the extended source with a better trade-off between the electrical parameters, we obtain the following results. The source extension width is varied for three differentvalues say 3nm, 5nm and 7nm.



(a)

(b) (c)

Fig -6: (a)Variation in source ext. width (b)Vth and Subthreshold swing variation(c)Ion and Ioff variation

Even though the surface area increases when we increase in the width of the extension, for higher widths it ends up transporting using direct band to band tunneling, which makes the I-off much higher. So we select 3nm as optimum width.

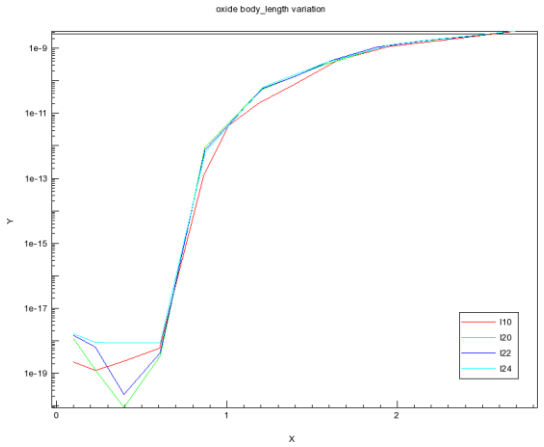
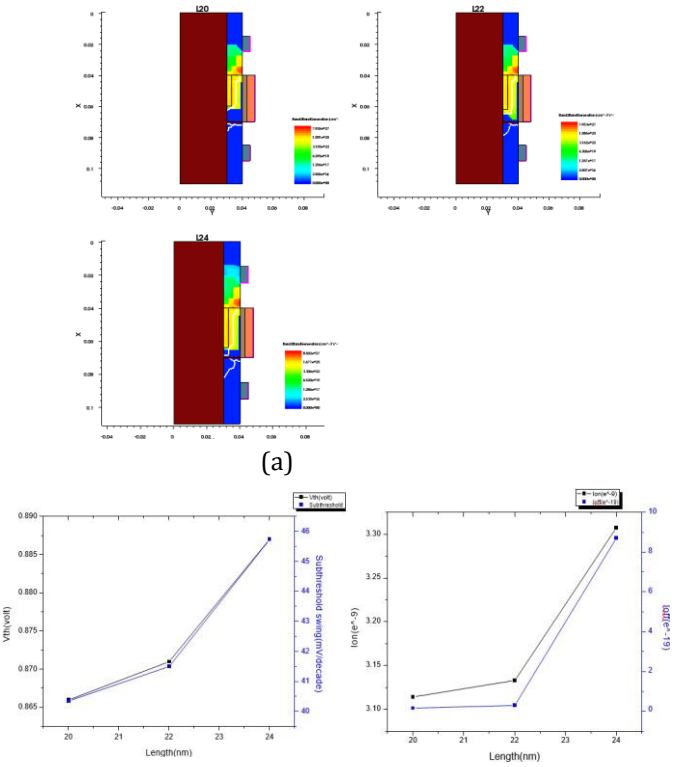


Fig -7: Output characteristics –source ext. length variation

The Length of source extension is varied for four different values such as 10nm,20nm 22nm and 24nm. The gradation is not uniform as the variation was too steep between 20nm and 30nm length. And the following BTBT is observed. The variation of threshold voltage(Vth), the subthreshold swing, Ion and Ioff for various length are plotted as below.



(a)

(b) (c)

Fig -8: (a)Variation in source ext. length (b)Vth and Subthreshold swing variation(c)Ion and Ioff variation

Beyond the length of extension of 20nm the tunneling becomes direct band to band tunneling. so we use the 20nm as our optimum length of extension.

3.3 VARIATION OF BURIED OXIDE THICKNESS

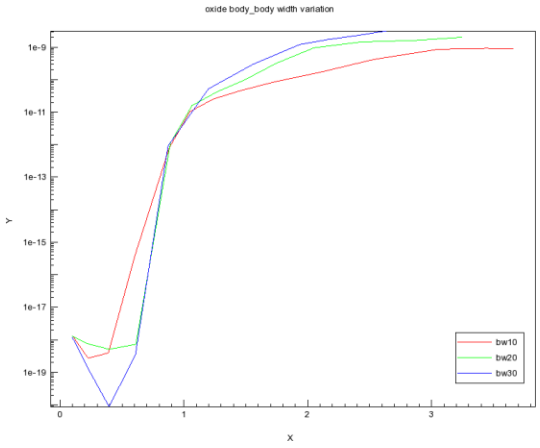
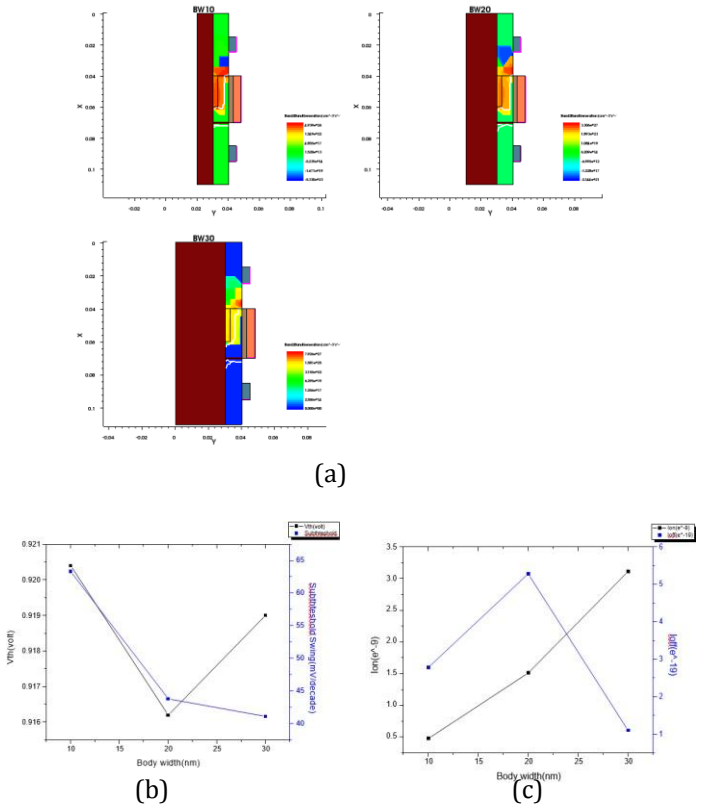


Fig -8: Output characteristics –BOX thickness variation

SOI transistors has an advantage of bulk silicon parasitic elimination and thus contribute to low power consumption and higher speed. Thus for further enhancing our design, we introduce a Buried oxide of SiO^2 which is of low-k unlike the gate oxide which is a high-K dielectric. The comparison is made between three thicknesses 10nm,20nm and 30nm. And the results are as follows.



(a) (b) (c)

Fig -9: (a)Variation in BOX thickness(b)Vth and Subthreshold swing variation(c)Ion and Ioff variation

In order to reduce the geometric scaling, we go for higher body width. Here the body oxide capacitance and the depletion capacitance are series connected topologywhichis in parallel with the gate capacitance. Beyond 20nm, the gate capacitance dominates and thus we see a sudden drop in the Ioff and increase in Vth due to lower geometric scaling.

4. CONCLUSIONS

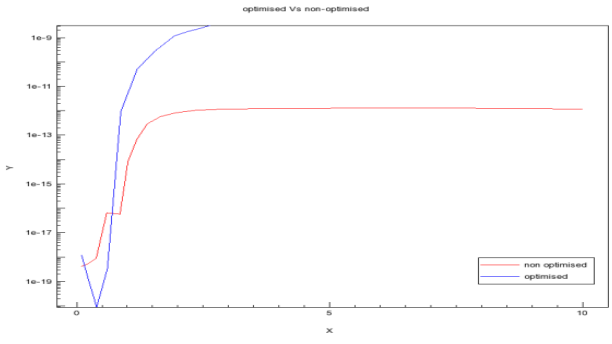


Fig -10: Output characteristics –Bulk and SOI TFET(opti)

The above plot is the output characteristics of both the initial TFET that we considered and the optimized extended SOI-TFET that we designed. It is evident from the plot that the optimized SOI-TFET has much higher Ion and lower Ioff than the non-optimized one.

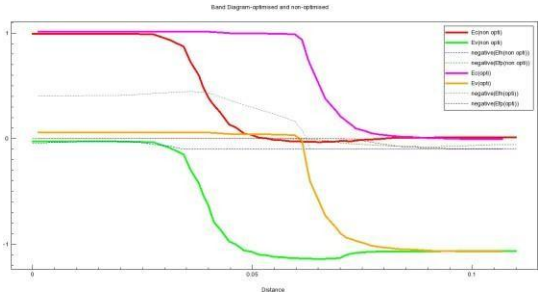
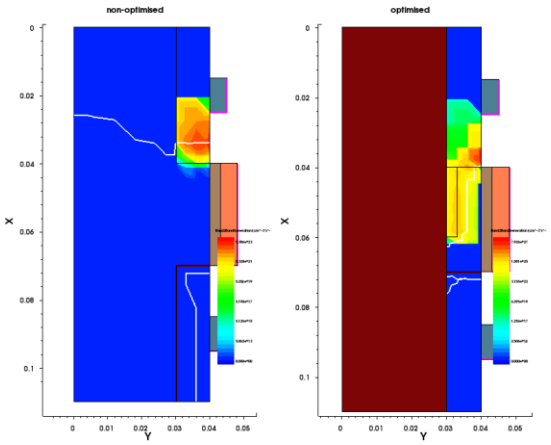


Fig -11: Band diagram of both TFETS

Further, upon investigating the Band diagram of both the TFETS we observe that the SOI-TEFT has lesser band gap, thus enhancing the probability of band-to-band tunneling. The tunneling is clearly visible in the below fig-12.



(a) **(b)**

Fig -12: Band to band tunnelling of (a)Non-optimised TFET (B)Optimise SOI-TFET

The following Table-1 draws an comparison between the two devices with regard to their electrical parameters.

Table -1: Comparison of electrical parameters

Parameters	Optimized Model	Non optimized model
Ion	2.9814*e^-9	1.27*e^-12
Ioff	1.473*e^-20	4.55*e^-19
Vth	0.88442 volt	1.184 volt
Subthreshold swing	37.77 mV/decade	71.89 mV/decade

The following table gives the optimum values of the design parameters for the SOI-TFET structure after careful examination.

Table -1: optimum device design parameters

Ext. length (nm)	Ext. Width (nm)	Body width (nm)	Doping conc.
20nm	3nm	30nm	$1xe^{20}$

Thus we observe an increase in Ion four orders of magnitude. The Ioff is decreased by one order of magnitude. Further we also observe that the threshold voltage has decreasedby 25% from that of the normal single gate TFET and the subthreshold swing is reduced by 47% of the Subthreshold swing of the single gate TFET.

Further improvements can be observed by using multiple gates.

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